



Application Note

The CS5504 Family Characteristics

The CS5504/5/6/7/8/9 are a series of A/D converters all derived from a high performance $\Delta\Sigma$ architecture. The CS5504 family members are based on a core architecture including both an analog modulator and a digital filter, with only subtle differences between the individual products. The digital filter has been optimized to attenuate ac line interference (50/60 Hz and their harmonics) when the devices are operated from a low-cost 32.768kHz crystal.

The use of a low-cost 32.768kHz clock provides 20 samples per second from the family. The CS5505/6/7/8 can achieve up to 100 samples/second with a 163kHz system clock, while the CS5504/9 can achieve up to 200 samples/second when operated from its maximum input clock of 330 kHz. In achieving higher conversion rates, the CS5504 requires slightly higher operating currents than the CS5505/6/7/8. The CS5509 achieves the same high conversion rate as the CS5504 with lower power consumption, but pays a slight penalty in linearity.

Table 1 summarizes the similarities and differences of the CS5504 family.

The CS5504/9 come in smaller packages than the CS5505/6/7/8, however, the CS5505/6/7/8 have more functionality and flexibility. The CS5505/6/7/8 offer a sleep function, an on-chip voltage reference, and multiple serial communication modes.

Table 2 shows the CS5504 family's wide array of power supply options. Note: the CS5509 is single supply, however, the VA+ supply for all devices must always be the most positive operating voltage under all operating conditions, including start-up.

	VA+	VA-	VD+
CS5504/5/6/7/8	+5 to +10V	0V	+5V
	+5V	0 to -5V	+5V
	+5V	0 to -5V	+3.3V
CS5509	+5V	-	+5V
	+5V	-	+3.3V

Table 2. Power Supply Arrangements

	Resolution	#Channels	Max. Speed ³	Linearity ⁴ (Typical)	Sleep	Power	On-chip VREF	Serial Port Modes ⁵	Pin Count
CS5504	20-bits	2 ¹	200	0.0007%	No	4.4 mW	No	SEC	20
CS5505	16-bits	4 ²	100	0.0015%	Yes	3 mW	Yes	SEC, SSC	24
CS5506	20-bits	4 ²	100	0.0007%	Yes	3 mW	Yes	SEC, SSC	24
CS5507	16-bits	1 ¹	100	0.0015%	Yes	3 mW	Yes	SEC, SSC	20
CS5508	20-bits	1 ¹	100	0.0007%	Yes	3 mW	Yes	SEC, SSC	20
CS5509	16-bits	1 ¹	200	0.0015%	No	1.7 mW	No	SEC	16

Table 1. CS5504 Family Characteristics

- Notes:
1. Fully-differential
 2. Pseudo-differential
 3. CS5509 is production tested at 330 kHz (200 samples/second)
All others are production tested at 32.768 kHz for the best 50/60 Hz rejection.
 4. These linearity specifications are based on a 20Hz output rate using a 32.768kHz crystal.
 5. SEC is synchronous external clocking of the data out while SSC is synchronous self-clocking.

