

## Evaluation Board for CS5334/CS5335/CS5360

### Features

- Demonstrates recommended layout and grounding arrangements
- CS8402A Generates AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Buffered Serial Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

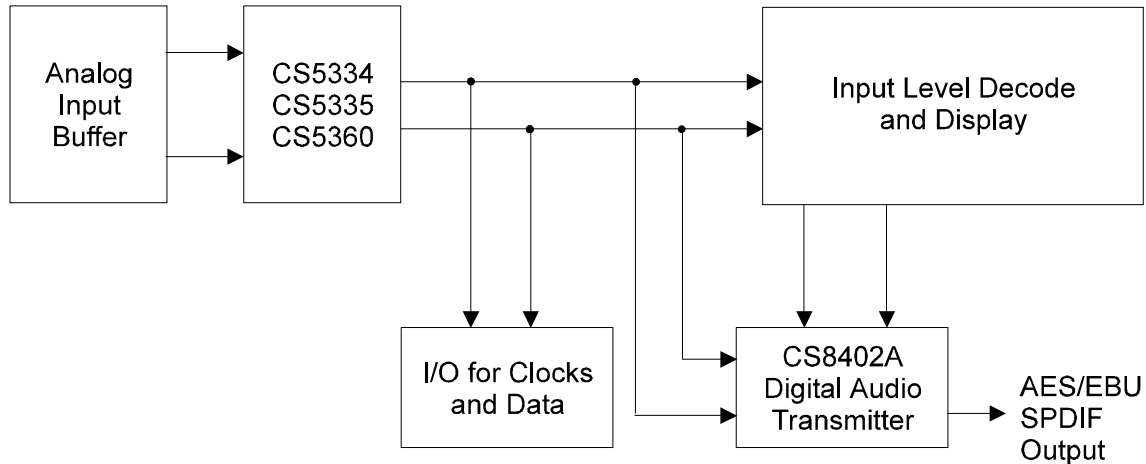
### Description

The CDB5334/35/60 evaluation board is an excellent means for quickly evaluating the CS5334, CS5335, or CS5360 stereo A/D converters. Evaluation requires a digital signal processor, a low distortion analog signal source and a power supply. Analog inputs are provided via XLR connectors for both channels.

Also included is a CS8402A digital audio interface transmitter which generates AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono, and optical connectors.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

**ORDERING INFO**  
CDB5334/35/60



### Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

## **CDB5334/35/60 SYSTEM OVERVIEW**

The CDB5334/35/60 evaluation boards are an excellent means of quickly evaluating the CS5334, CS5335, or CS5360. The CS8402A digital audio interface transmitter provides an easy interface to digital audio signal processors, including the majority of digital audio test equipment. The evaluation board has been designed to accept an analog input, and provide optical and coaxial digital outputs. The evaluation board also allows the user to access clocks and data through a 10-pin header for system development. In addition, the evaluation board supports the input level monitoring function provided by the CS5334, CS5335, and CS5360. The Peak Signal Level bits are displayed on bargraph LEDs or 7 segment displays for both left and right channels.

The CDB5334/35/60 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the connections between the partitioned schematics.

### **Power Supply Circuitry and Grounding**

Power is supplied to the evaluation board by six binding posts as shown in Figure 2. +5VA provides 5 Volt power to the converter and the reset circuitry. The  $\pm 12$  V binding posts provide power to the analog input buffer. C1-C3 and C5-C7 provide general power supply filtering for the analog supplies. Z1-Z3 are transient suppression diodes which also provide protection from incorrectly connected power supply leads. +5VD supplies 5 Volt power to the digital section of the board. C41 and C10 provide general power supply filtering. Z4 is a transient suppressor.

Localized decoupling for the CS5334, CS5335, or CS5360 is provided by C16, C17, C32, and C33, as shown in Figure 4. R10, C16, and C32 form a low pass filter which isolates VA+ from noise on VD+.

The evaluation board uses separate analog and digital ground planes which are joined together underneath resistors R6, R41, and R52-R55. This arrangement isolates the analog circuitry from the digital logic.

### **Reset Circuit and Offset Calibration**

Two methods of placing the CS5334, CS5335, or CS5360 into power-down mode are provided on the evaluation board. The CAL switch, shown in Figure 8, pulls the DIF0 and DIF1 lines high on the CS5334, CS5335, or CS5360, thus placing the ADC into power-down mode. Releasing the CAL switch causes the DIF0 and DIF1 settings to be restored, upon which an initialization sequence begins, as described in the CS5334/CS5335 and CS5360 data sheets.

The reset circuit provided on the evaluation board is shown in Figure 2. Upon power up, this circuit sends a reset to the RST pin of the CS5334, CS5335, or CS5360. Power-down, followed by offset calibration, can also be performed by pressing and then releasing the RST switch. It should be noted that only the RST method of powering down the CS5334, CS5335, or CS5360 will include the decision of master or slave operation.

### **Input Buffer and Protection Circuits**

The differential input circuit shown in Figure 3 is well-suited for the CS5334, CS5335, and CS5360 in professional applications. The circuit will accept a differential or single-ended signal of either polarity and provide a differential signal with the proper DC offset to the CS5334, CS5335, or CS5360. The circuit also incorporates 6 dB of attenuation to scale down professional input levels to the input voltage range of the CS5334, CS5335, or CS5360. A nominal input level of 4 Volts rms to the evaluation board will achieve a full scale digital output from the CS5334, CS5335, or CS5360. The common mode rejection of the system is limited by the passive component matching of the input buffer

circuit. The analog input connector is a standard female XLR with Pin 2 positive, Pin 3 return, and Pin 1 shield.

R1, R5, and C8 form an RC network which provides anti-alias filtering and the optimum source impedance for the CS5334, CS5335, or CS5360 right channel inputs. R2, R3, and C42 duplicate this function for the left channel.

Space has been left on the evaluation board for input protection diodes D1-D4 on the right channel, and D8-D11 on the left channel, shown in Figure 3. These diodes are optional as the CS5334, CS5335, and CS5360 are able to withstand input currents of 100mA maximum, as stated in the CS5334/CS5335 and CS5360 data sheets. The output current from the op-amp used in the analog filter on the evaluation board is not able to deliver a current that exceeds 100mA. Input protection diodes are recommended if there is a possibility that over-range signals could be applied at the ADC inputs which exceed this level. See the application note, "A/D Converter Input Protection Techniques" in the 1994 Crystal Semiconductor Audio Databook.

### **CS5334, CS5335, and CS5360 A/D Converters**

The CS5334, CS5335, and CS5360 A/D converters are shown in Figure 4. A description of these devices are included in the CS5334/CS5335 and CS5360 data sheets.

### **CS8402A Digital Audio Interface**

Figure 5 shows the circuitry for the CS8402A digital audio interface transmitter. The CS8402A can implement AES/EBU, S/PDIF, and EIAJ-340 interface standards. The Digital Interface Format (DIF) for the transmitter is set automatically to match the format chosen for the CS5334, CS5335, or CS5360 (the DIF is selected by the DIF1 and DIF0 switches on SW1, as defined in Table 3). SW2 provides 8 DIP switches to select various

modes and bits for the CS8402A; switch definitions and the default settings for SW2 are listed in Tables 4 and 5. Digital outputs are provided on an RCA connector via isolation transformer and on an optical transmitter. For more detailed information on the CS8402A and the digital audio standards, see the CS8401A/CS8402A data sheet.

### **Serial Output Interface**

A serial output interface is provided on HDR2, as shown in Figure 6. When the SMODE1 and SMODE2 jumpers, defined in Table 2, are set to the MASTER position, MCLK, SCLK, LRCK, SDATA, and FRAME signals are outputs. When the SMODE1 and SMODE2 jumpers are in the SLAVE position, MCLK, SDATA, and FRAME are outputs, while SCLK and LRCK become inputs. Hence, in SLAVE mode, the SCLK and LRCK signals must be externally derived from MCLK to run the ADC. All signals are buffered in order to isolate the converter from external circuitry. Signal buffering is provided by a 74HCT243 transceiver (U10) and a 74HCT541 buffer (U11).

### **ALTERA PLD AND PEAK SIGNAL LEVEL LEDS**

The Altera EPM7128 programmable logic device (PLD), shown in Figure 8, is designed to support three major features on the evaluation board. First, it automatically configures the CS8402A transmitter to accept the Digital Interface Format chosen for the CS5334, CS5335, or CS5360. Second, the PLD provides a 128x Fs master clock for the CS8402A. Third, it decodes and updates the Peak Signal Level (PSL) bits which give information about the amplitude of the input signal.

### **CS8402A Format Configuration**

The CS5334, CS5335, and CS5360 support three Digital Interface Formats for both master and slave configurations. Format 0 has valid data on the rising edge of SCLK. The CS8402A transmitter has no corresponding mode which matches Format 0,

but inverting the SCLK so that data is valid on the falling edge of SCLK will make the Format 0 interface lines match the Format 1 interface lines on the CS8402A. The PLD configures the CS8402A to Format 1 and performs SCLK inversion automatically when the DIF1, DIF0 switches on SW1 are set to 00.

Digital Interface Format 1 on the CS5334, CS5335, and CS5360 has valid data on the falling edge of SCLK. This interface format matches Format 1 on the CS8402A, so no modification is performed on the digital interface lines. The PLD configures the CS8402A to FORMAT 1 and passes the interface lines from the CS5334, CS5335, or CS5360 through to the CS8402A unchanged when the DIF1, DIF0 switches are set to 01.

Digital Interface Format 2 is the I2S compatible mode. It matches Format 4 on the transmitter. The PLD configures the CS8402A to Format 4 and passes the interface lines from the CS5334, CS5335, or CS5360 through to the CS8402A unchanged when the DIF1, DIF0 switches are set to 10.

### **CS8402A MCLK Generation**

When the CDB5334/35/60 is set up for SLAVE mode, the crystal oscillator (U5) can be 256x, 384x, or 512x Fs. The CS8402A requires a master clock frequency of 128x Fs to operate. The PLD can be configured to divide MCLK\_5335 (the oscillator output) by 2, 3, or 4 to generate MCLK\_8402, thus accommodating the various possible frequencies of the oscillator. The switches on SW1 labeled MCLK\_S1 and MCLK\_S0 select the degree of clock division as defined in Table 3.

### **Decoding PSL bits / Driving LEDs**

The PLD decodes and displays the Peak Signal Level bits for both High Resolution and Bargraph

modes (for detailed information on the PSL bits, see the CS5334/CS5335 and CS5360 datasheets). When the TMODE1 and TMODE2 jumpers, defined in Table 2, are set to BARGRAPH, the PLD decodes the PSL bits and drives bargraph LEDs for the left and right channels. When the TMODE1 and TMODE2 jumpers are set to HI RES (High Resolution mode), the PLD drives the 7 segment displays for left and right channels.

The PLD also provides a Peak Update (PU) signal, which adjusts the rate at which the PSL bits are updated. Four settings provide update rates ranging from 42 ms to 2.7 s (for a 48 kHz sample rate). The switches on SW1 labeled PU\_S1 and PU\_S0 select the PU frequency as shown in Table 3.

## **GROUNDING AND POWER SUPPLY DECOUPLING**

The CS5334, CS5335, and CS5360 require careful attention to power supply and grounding arrangements to optimize performance. Figure 4 shows the recommended power arrangements. The CS5334, CS5335, or CS5360 is positioned over the analog ground plane, near the digital/analog ground plane split, to minimize the distance that the clocks travel. The series resistors are present on the clock and data lines to reduce the effects of transient currents when driving a capacitive load in MASTER mode, and to reduce clock overshoot when applying external clocks to the ADC in SLAVE mode.

This layout technique is used to minimize digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the ADC as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5VA	input	+5 Volts for analog section
+5VD	input	+5 Volts for digital section
±12V	input	±12 Volts for analog input
AGND	input	analog ground connection from power source
DGND	input	digital ground connection from power source
AINL	input	left channel differential/single ended analog input
AINR	input	right channel differential/single ended analog input
LRCK, SCLK	input/output	I/O for serial and left/right clocks
MCLK	output	master clock output
SDATA	output	serial data output
FRAME	output	framing signal output for PSL bits
coaxial output	output	CS8420A digital output via transformer
optical output	output	CS8420A digital output via optical transmitter

**Table 1. System Connections**

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
SMODE1, SMODE2	Selects master/slave operation for CS5334, CS5335, and CS5360 and I/O status of HDR2. SMODE1 and SMODE2 should always be set to the same position.	*MASTER SLAVE	Timing generation onboard. External clock generation, derived from MCLK.
TMODE1, TMODE2	Selects the functionality of the PSL bits. TMODE1 and TMODE2 should always be set to the same position.	HI RES *BARGRAPH	PSL bits display the input level PSL bits display the bargraph
HPSEL	Enables or disables the input highpass filter on the CS5334, CS5335, and CS5360	DEFEAT *ENABLE	Defeats highpass filter Enables highpass filter

**Table 2. Jumper Selectable Options**

Switch #	0 = closed, 1 = open	Comment
8, 7	MCLK_S1, MCLK_S0	Divides MCLK_5335 to generate MCLK_8402 for the CS8402A transmitter
	*0 0	Generates a 128x Fs clock when using a 256x Fs oscillator
	0 1	RESERVED
	1 0	Generates a 128x Fs clock when using a 384x Fs oscillator
	1 1	Generates a 128x Fs clock when using a 512x Fs oscillator
6, 5	*0 0	RESERVED
4, 3	DIF1, DIF0	Selects the digital interface format for the CS5334/35/60, and CS8402A
	*0 0	Configures the CS5334/35/60 for Format 0, and the CS8402A for Format 1
	0 1	Configures the CS5334/35/60 for Format 1, and the CS8402A for Format 1
	1 0	Configures the CS5334/35/60 for Format 2 (I <sup>2</sup> S), and the CS8402A for Format 4 (I <sup>2</sup> S)
	1 1	Places the CS5334/35/60 in power down mode
2, 1	PU_S1, PU_S0	Adjusts the frequency of the Peak Update signal for PSL bits
	*0 0	Updates the PSL bits at a frequency of LRCK/2 <sup>11</sup>
	0 1	Updates the PSL bits at a frequency of LRCK/2 <sup>13</sup>
	1 0	Updates the PSL bits at a frequency of LRCK/2 <sup>15</sup>
	1 1	Updates the PSL bits at a frequency of LRCK/2 <sup>17</sup>

**Table 3. Switch Definitions**

Switch #	0 = closed, 1 = open	Comment
6	$\overline{PRO} = 0$	Consumer Mode (C0 = 0)
8, 5	FC1, FC0	C24, C25, C26, C27 - Sample Frequency
	0 0	0000 - 44.1 kHz
	*0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
7	$\overline{C3}$	C3, C4, C5 - Emphasis (1 of 8 bits)
	*1	000 - None
	0	100 - 50/15 $\mu$ s
4	$\overline{C2}$	C2 - Copy/Copyright
	*1	0 - Copy Inhibited /Copyright Asserted
	0	1 - Copy Permitted/Copyright Not Asserted
3	$\overline{C15}$	C15 - Generates Status
	*1	0 - Definition is based on category code
	0	1 - See CS8402A Data Sheet, App. A
1, 2	$\overline{C8}, \overline{C9}$	C8 - C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	*0 0	1100000 - Digital Audio Tape - DAT

\* Default setting from factory

**Table 4. CS8402A Switch Definitions - Consumer Mode**

Switch #	0 = closed, 1 = open	Comment
6	PRO = 1	Professional Mode (C0 = 1)
8	CRE	Local Sample Address Counter and Reliability Flags
	0	Disabled
	1	Internally Generated
7, 4	C6, C7	C6, C7 - Sample Frequency
	0 0	00 - Not Indicated - Default to 48 kHz
	0 1	01 - 48 kHz
	1 0	10 - 44.1 kHz
	1 1	11 - 32 kHz
5	C1	C1 - Audio
	1	0 - Normal Audio
	0	1 - Non-Audio
3	C9	C8, C9, C10, C11 - Channel Mode (1 of 4 bits)
	1	0000 - Not Indicated - Default to 2-channel
	0	0100 - Stereophonic
1, 2	EM1, EM0	C2, C3, C4 - Emphasis (2 of 3 bits)
	1 1	000 - Not Indicated - Default to none
	1 0	100 - No emphasis
	0 1	110 - 50/15 μs
	0 0	111 - CCITTJ.17

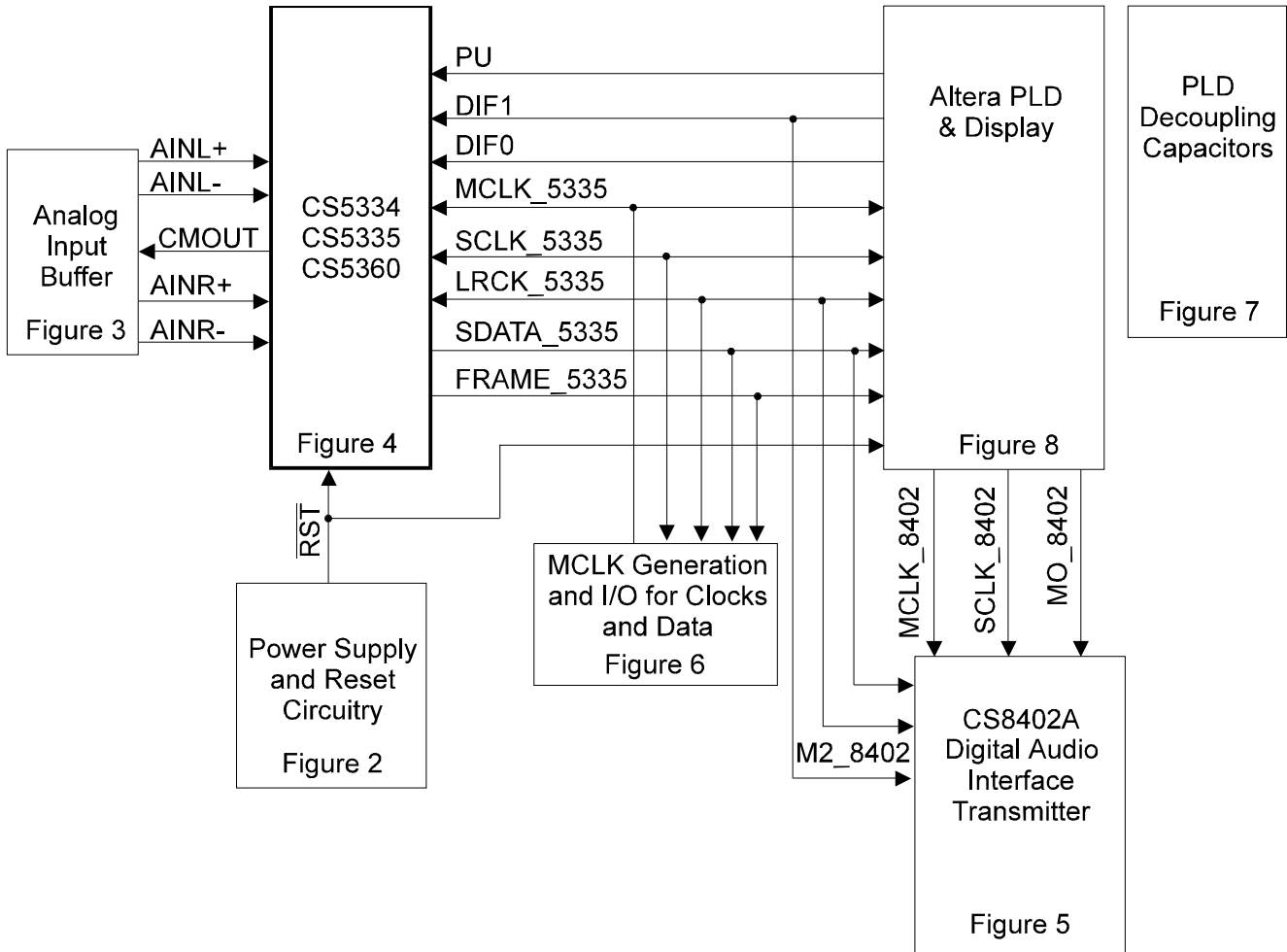
Table 5. CS8402A Switch Definitions - Professional Mode

**Schematic & Layout Review Service**

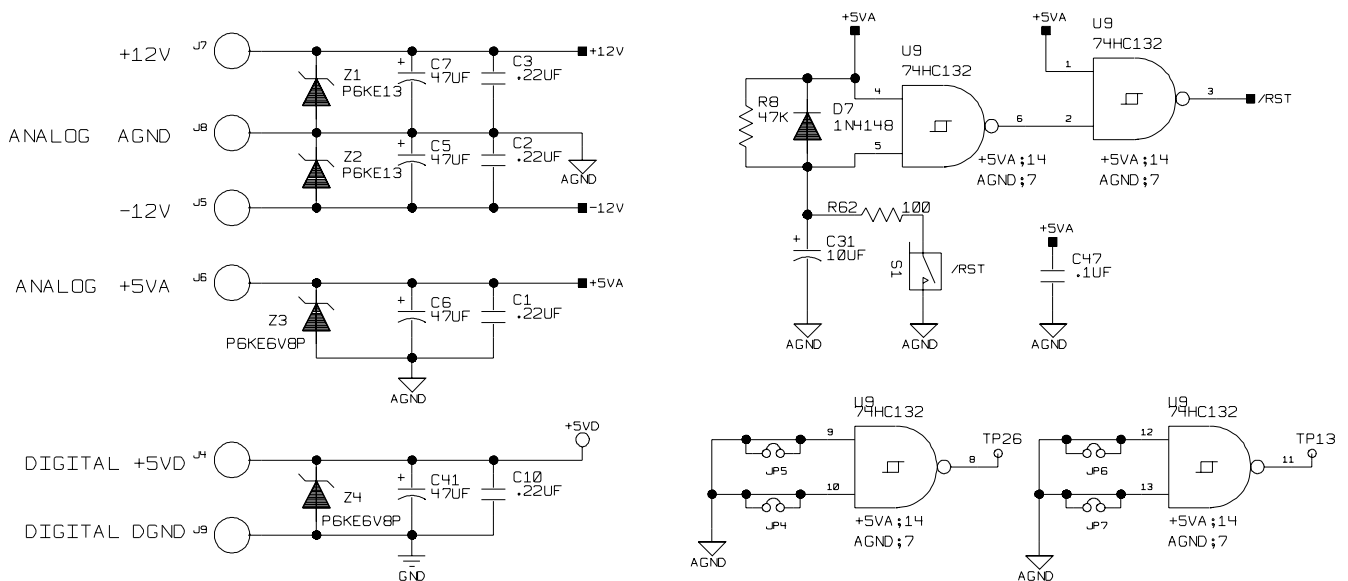
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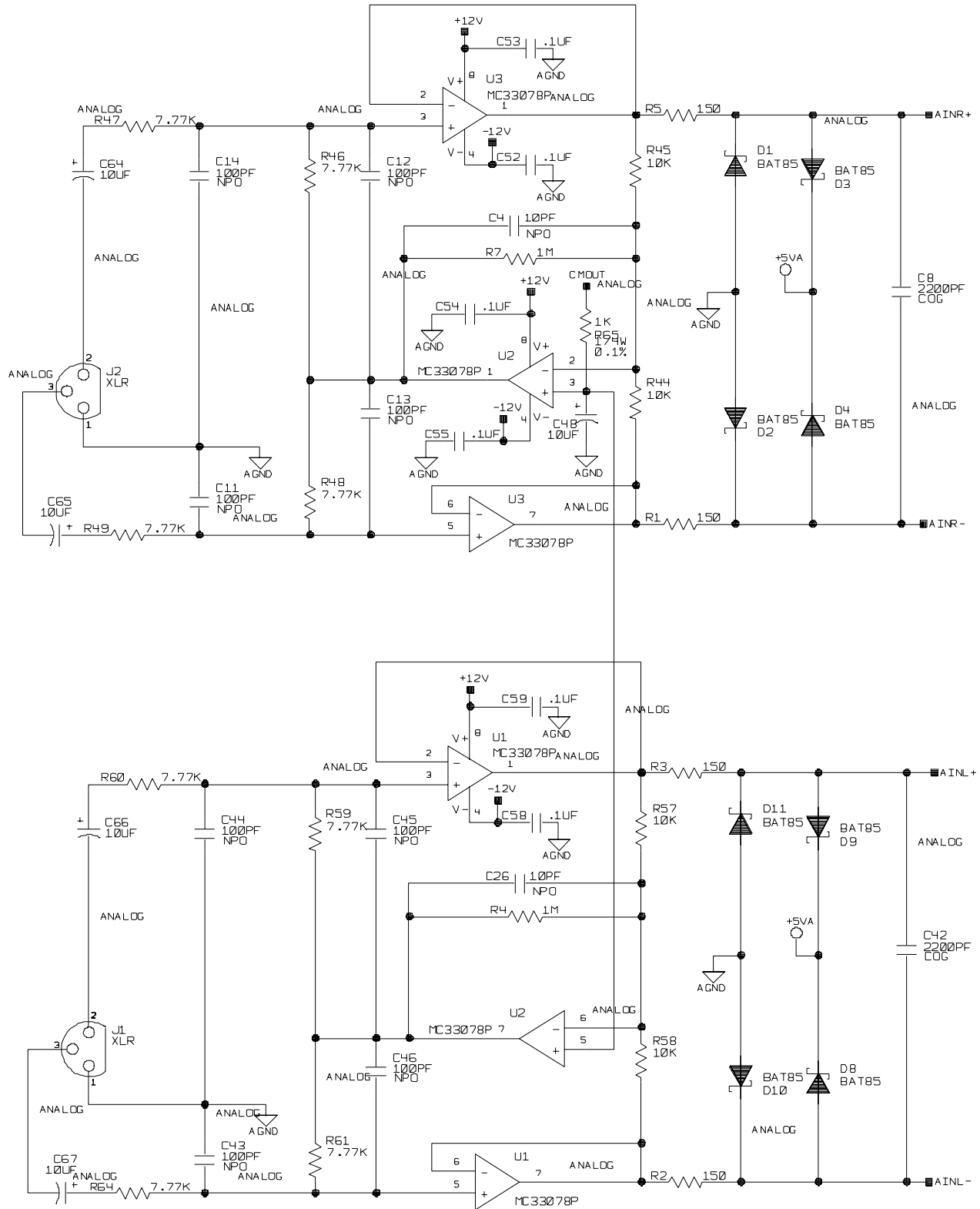


**Figure 1. System Block Diagram and Signal Flow**



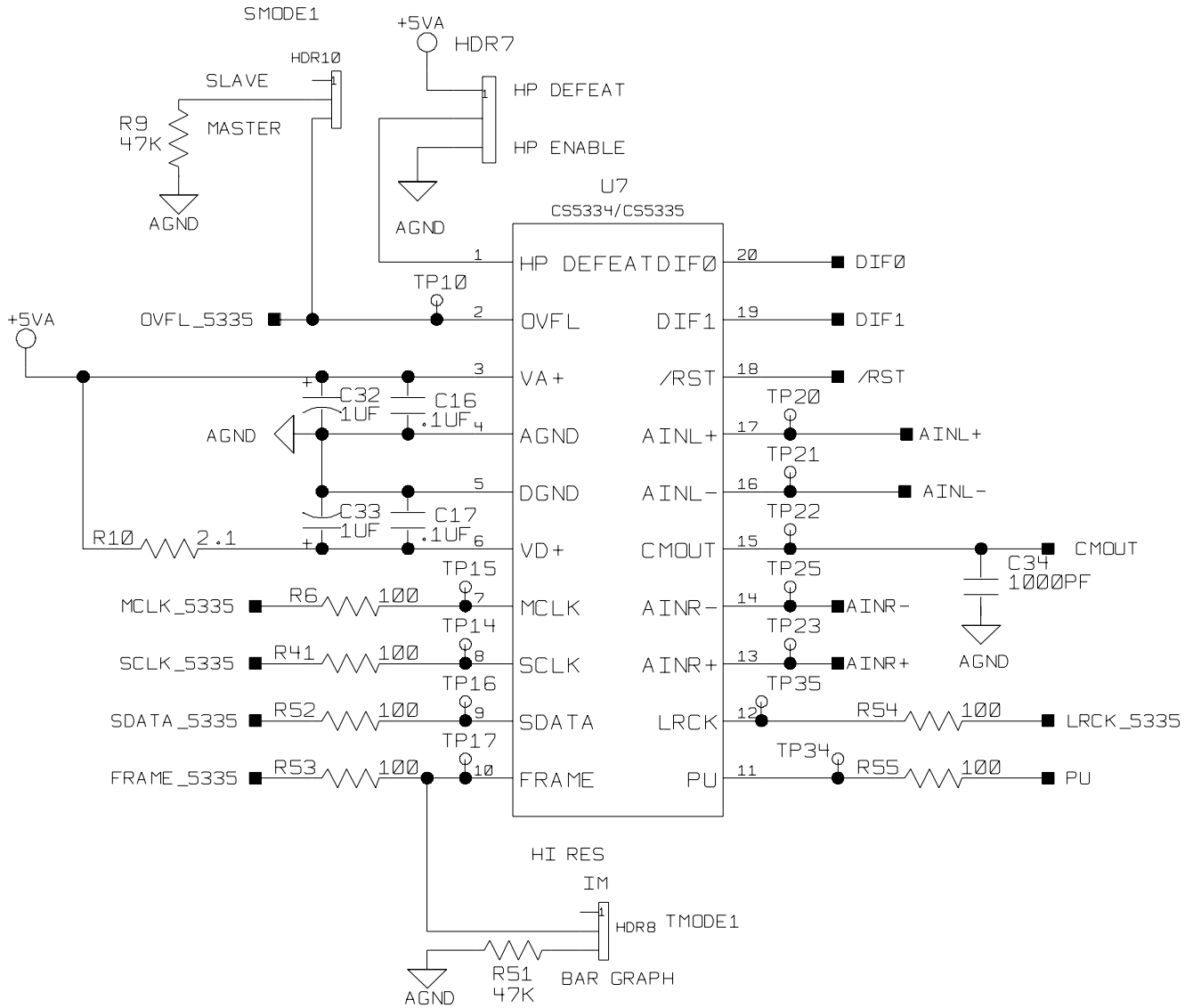
**Figure 2. Power Supply and Reset Circuitry**





NOTE: BAT85 Diodes are not installed on the Evaluation Board (see text)

**Figure 3. Analog Input Buffer**



**Figure 4. CS5334, CS5335, and CS5360 Connections**

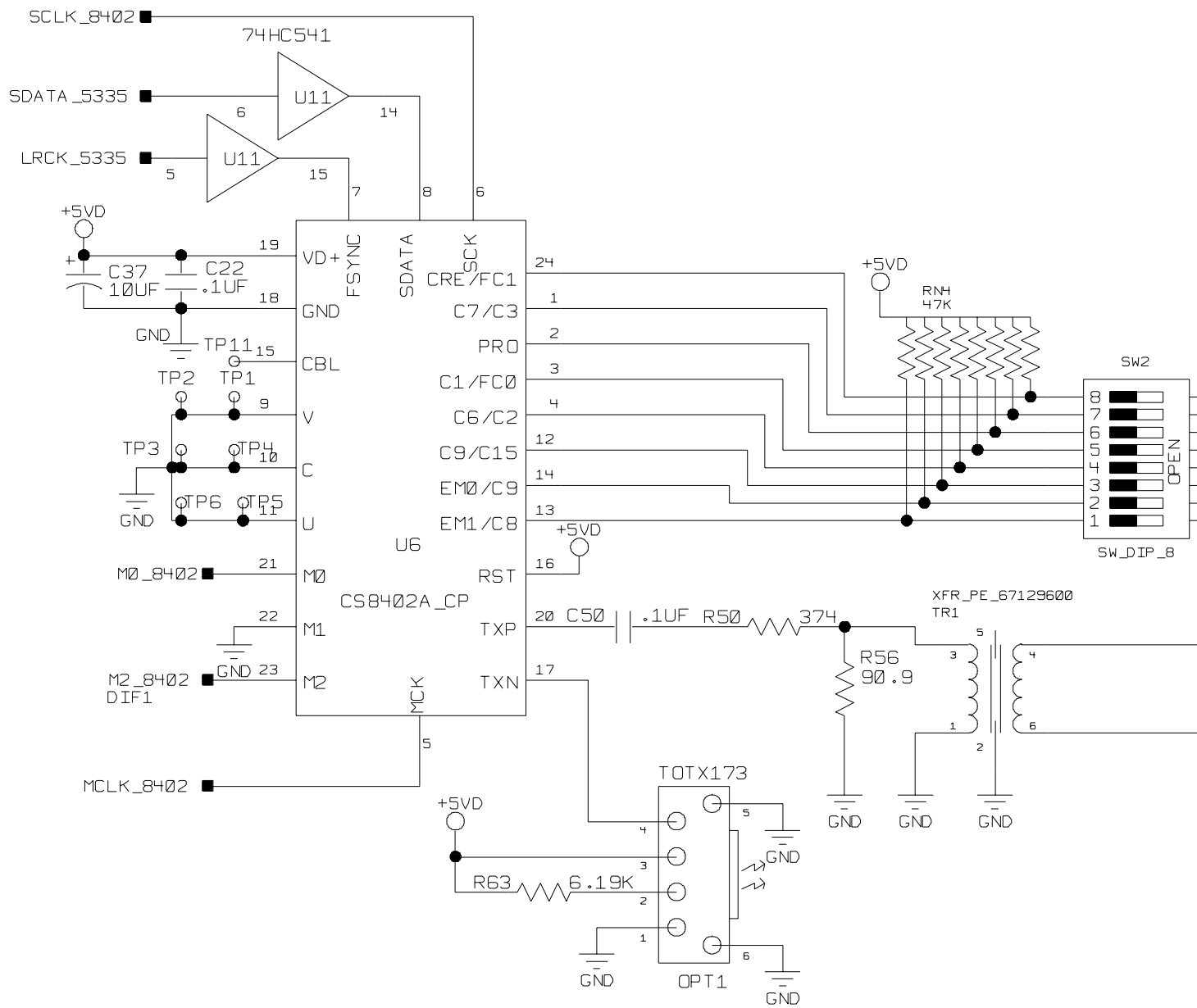
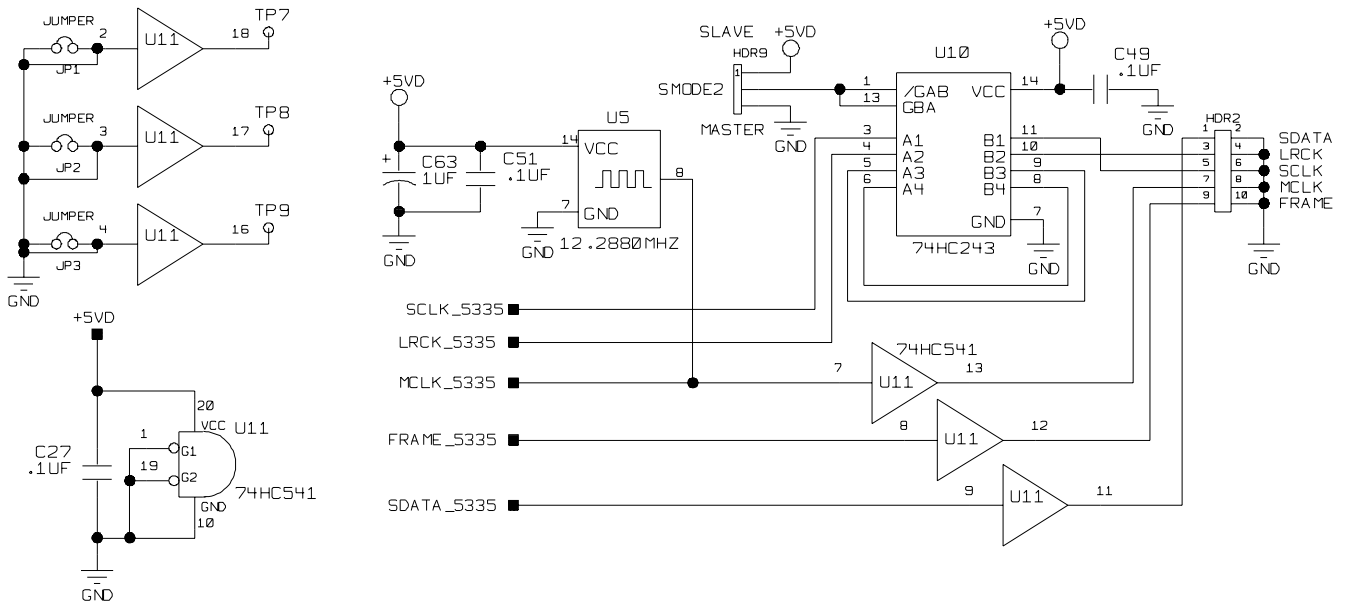
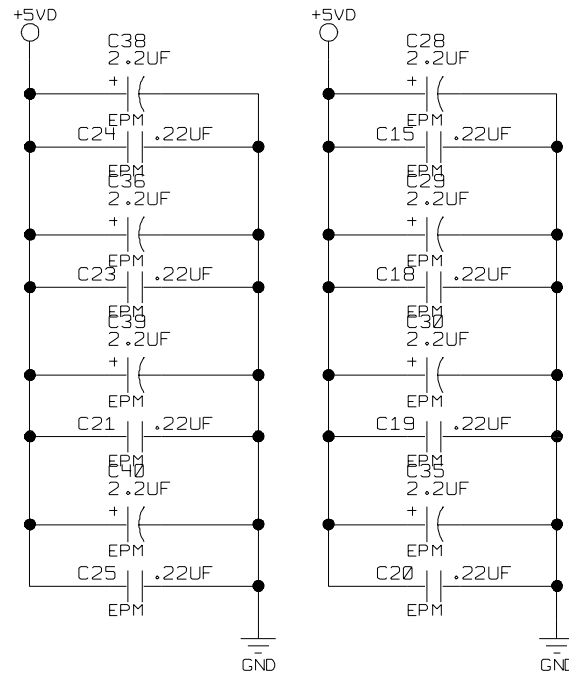


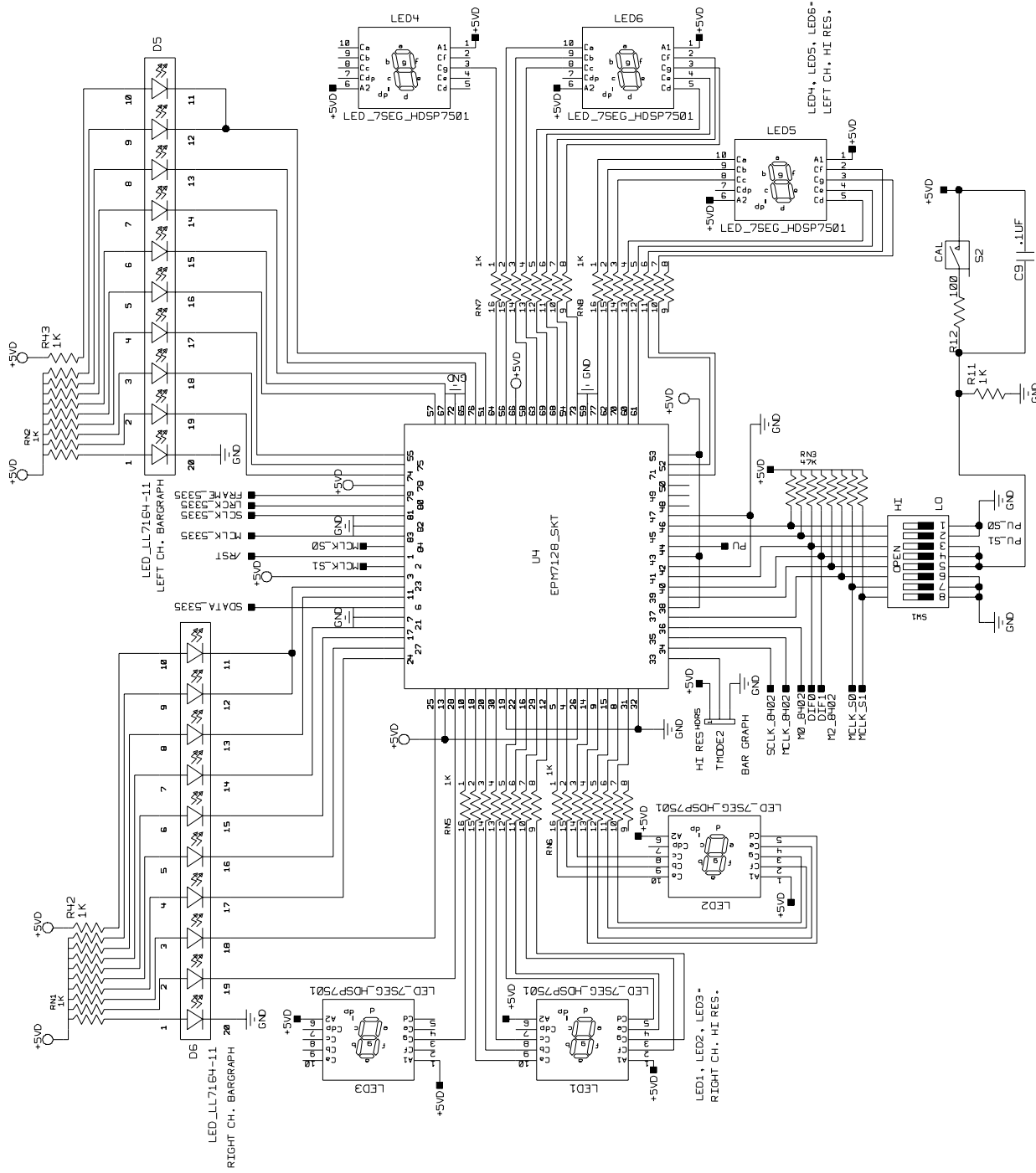
Figure 5. CS8402A Digital Audio Transmitter and Connections



**Figure 6. I/O Interface for Clocks and Data**

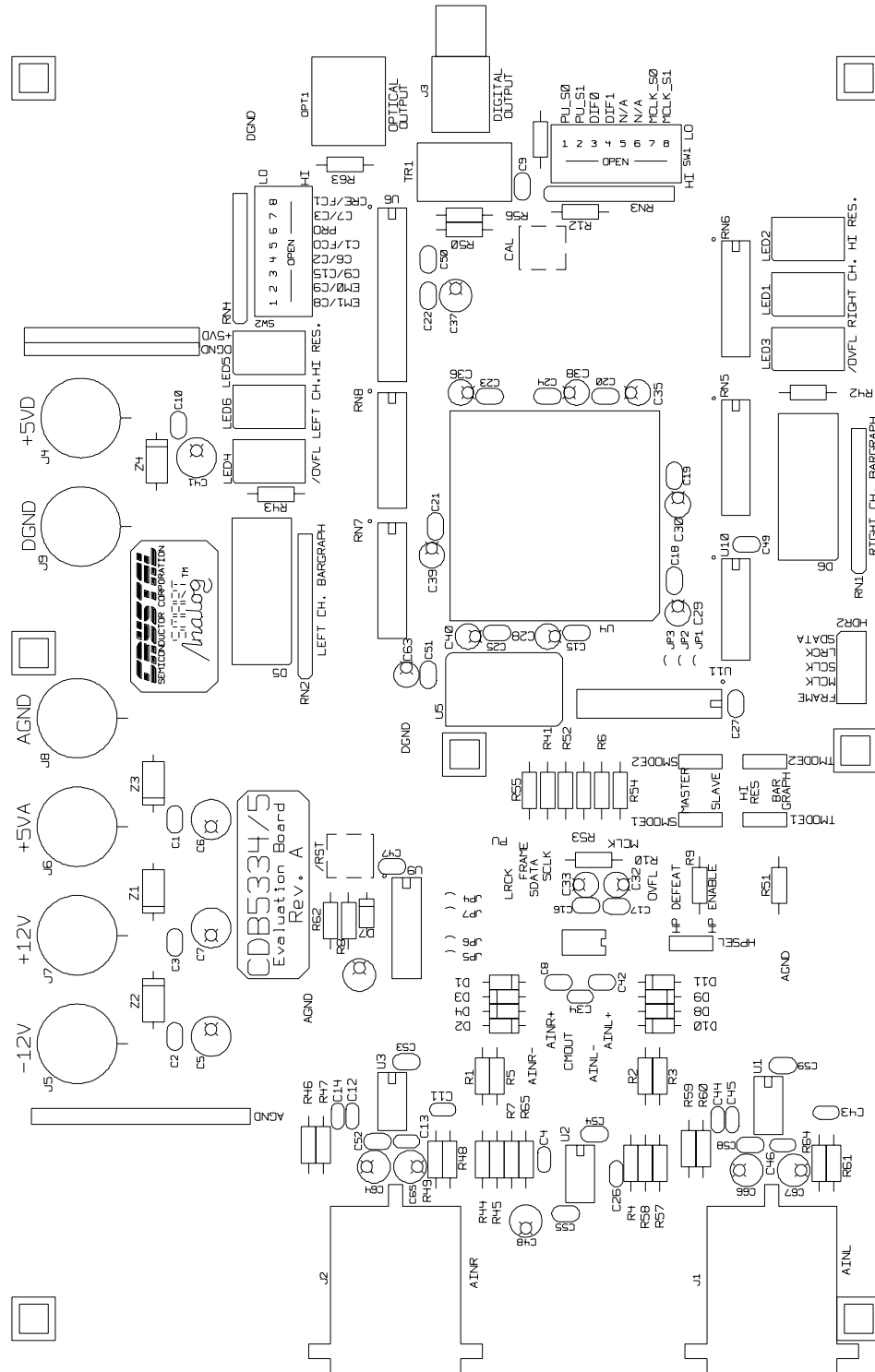


**Figure 7. Decoupling Caps for PLD**



**Figure 8. Altera PLD and Display LEDs**

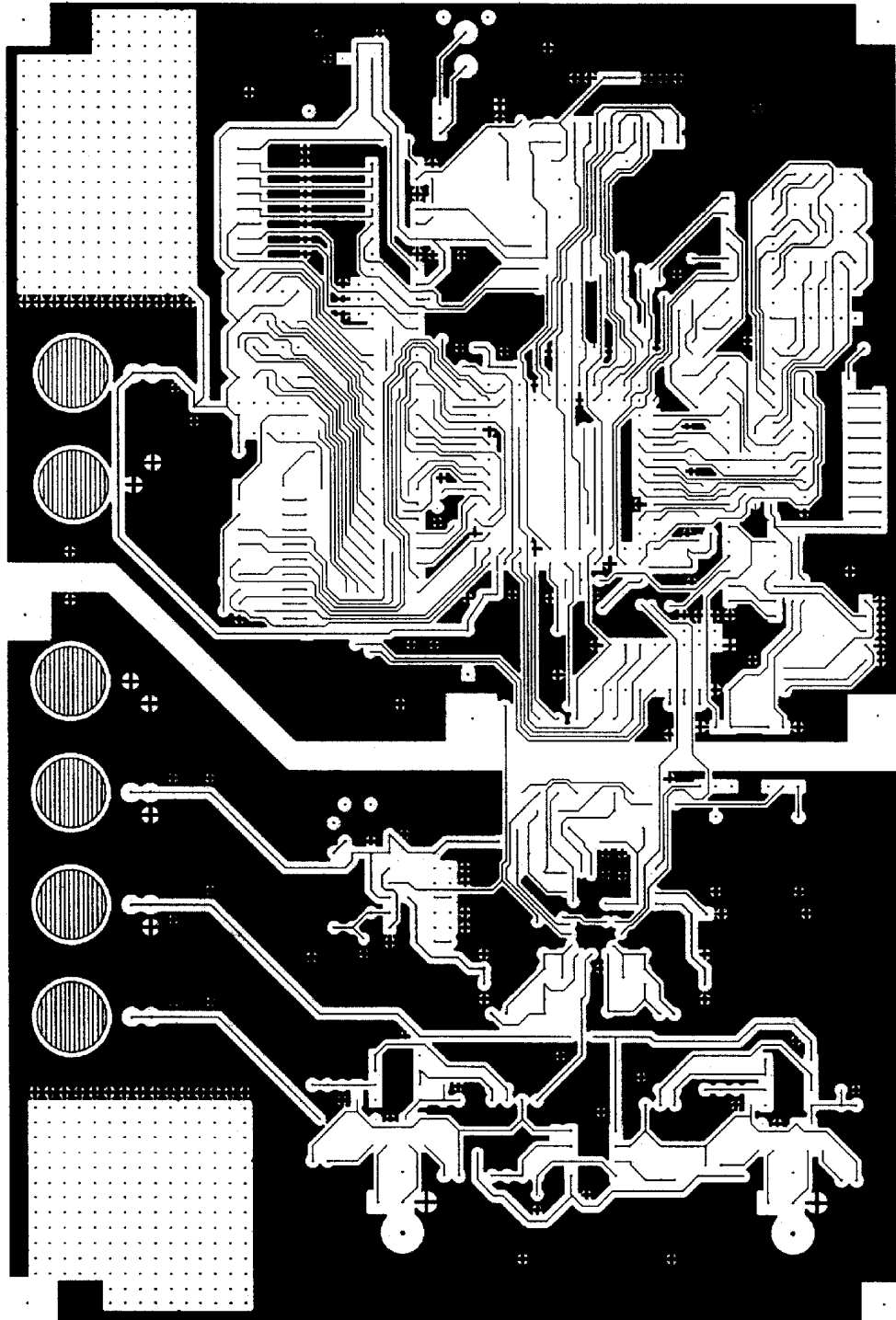
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Component Side Silkscreen

Figure 9. CDB5334/35/60 Component side (top)

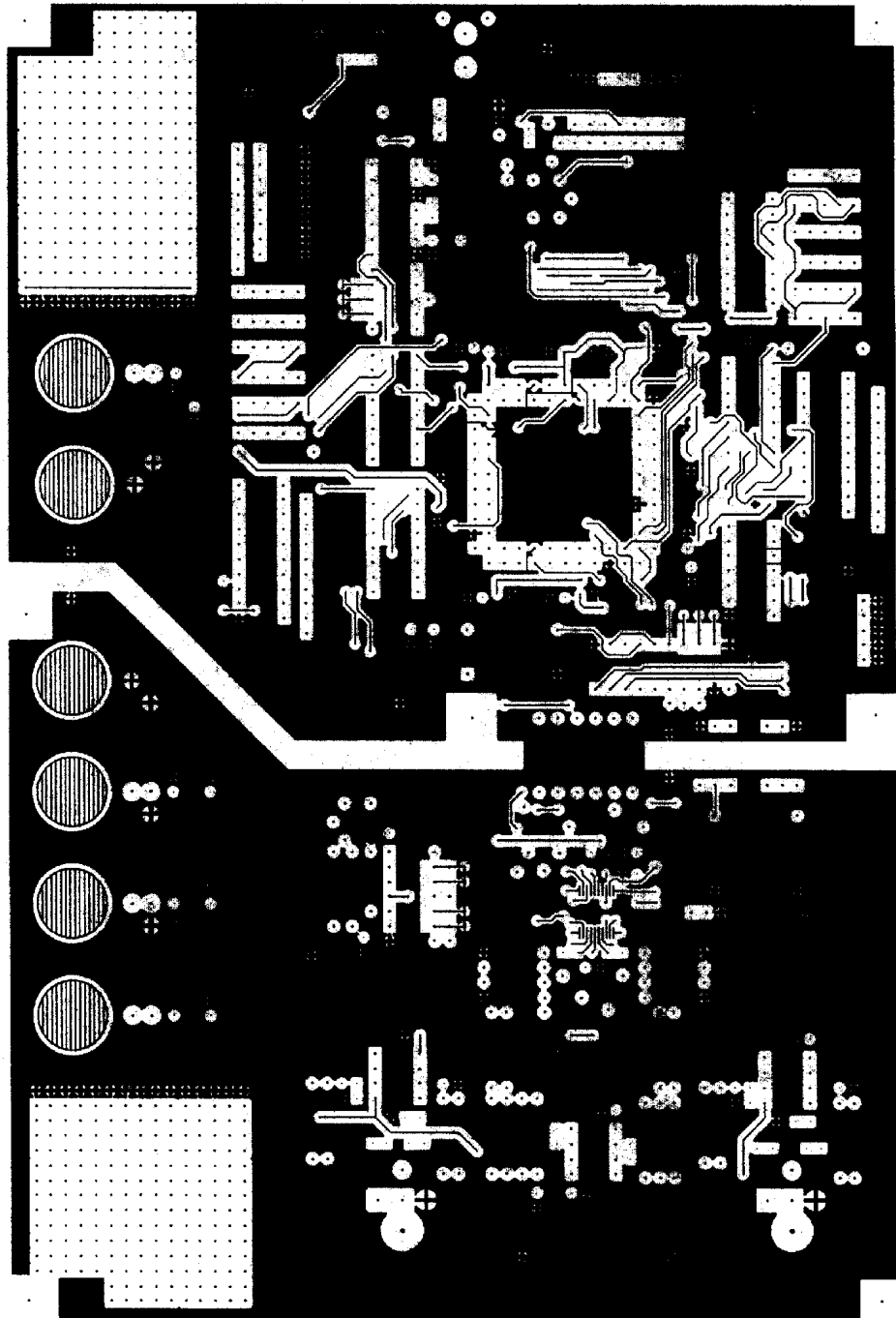
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SOLDER SIDE

Figure 10. CDB5334/35/60 Component side (bottom)

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CDB5334/5 Rev. A



COMPONENT SIDE

Figure 11. CDB5334/35/60 Solder side (bottom)



• **Notes** •

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