CIRRUS LOGIC®

CDB5361

Evaluation Board for CS5361

Features

- Demonstrates recommended layout and grounding arrangements
- CS8405A generates S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system

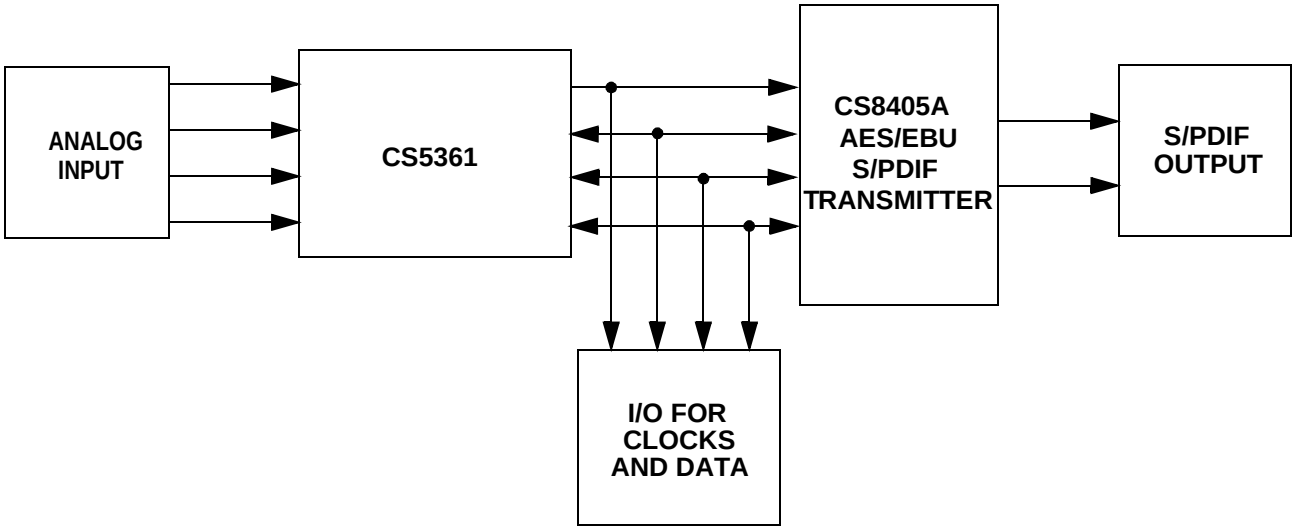
Description

The CDB5361 evaluation board is an excellent means for quickly evaluating the CS5361 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, and a power supply.

Also included is a CS8405A digital audio interface transmitter which generates S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB5361 Evaluation Board



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/

1. CDB5361 SYSTEM OVERVIEW

The CDB5361 evaluation board is an excellent means of quickly evaluating the CS5361. The CS8405A digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB5361 schematic has been partitioned into 9 schematics shown in Figures 2 through 10. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS5361 ANALOG TO DIGITAL CONVERTER

A description of the CS5361 is included in the CS5361 datasheet.

3. CS8405A DIGITAL AUDIO TRANSMITTER

The system generates and encodes standard S/PDIF data using a CS8405A Digital Audio Transmitter, Figure 7. The outputs of the CS8405A are RS422 compatible differential line drivers. The CS8405A supports both Left Justified and I^2S data formats, as determined by the DIP switch, S2. A description of the CS8405A is included in the CS8405A datasheet.

4. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J3. The schematic for the clock/data input/output is shown in Figure 6.

The CDB5361 allows some flexibility as to the generation of the clocks. When the CS5361 and CS8405A are in slave mode, the SCLK and LRCK must be provided via the header, J3. MCLK must be generated from the on board oscillator, Y1. This oscillator is socketed to allow other frequency oscillators to be used.

5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by six binding posts (VEE, VCC, VD, VL, GND, +5 V), see Figure 10. VEE and VCC supply the input amplifiers while the VD input supplies the VD pin of the CS5361. VL supplies power to the VL pin of the CS5361 and to the level shifter circuits. The +5 V input supplies power to the +5 V digital circuitry and the VA pin of the CS5361.

6. GROUNDING AND POWER SUPPLY DECOUPLING

The CS5361 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 4 details the power distribution used on this board. The decoupling capacitors are located as close to the CS5361 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

7. ANALOG INPUT FILTER

The CDB5361 implements a single-ended to differential analog input buffer, as shown in Figures 2 and 3. Note that the first inverting stage attenuates the input by 0.5. This will allow the updated modal dynamics of a 2Vrms signal (single-ended) applied to the board to be 2Vrms (differential) going into the CS5361.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
VEE	Input	-5V to -12V power
VCC	Input	+5V to +12V power
VD	Input	+3.3V to +5V power for the CS5361
VL	Input	+1.8V to +5V power for the CS5361
GND	Input	Ground connection from power supply
+5V	Input	+ 5 Volt power
AINL	Input	Analog input left channel
AINR	Input	Analog input right channel
Optical Output	Output	Digital audio output
Coax Output	Output	Digital audio output

Table 1. System Connections

JUMPER/SWITCH	PURPOSE	POSITION		FUNCTION SELECTED
J3	Input/Output for clocks/data	-		-
S1	Reset for the CDB5361	-		-
S2	CDB5361 Configuration	M1/M0	Open *Closed	Hi *Low
		5361	*Open Closed	CS5361 in Master mode CS5361 in Slave mode
		HPF	Open *Closed	High-pass filter is disabled High-pass filter is enabled
		DIV	Open *Closed	MCLK is divided by two internally by the CS5361 MCLK is not divided internally by the CS5361
		IO_HDR	Open *Closed	Header J3 is an input for clocks Header J3 is an output for clocks and data
		DIF	*Open Closed	Digital interface format set to I^2S Digital interface format set to Left Justified
		8405A	Open *Closed	CS8405A in Master mode CS8405A in Slave mode

Table 2. CDB5361 Jumper and Switch Settings

Notes: * denotes default factory settings

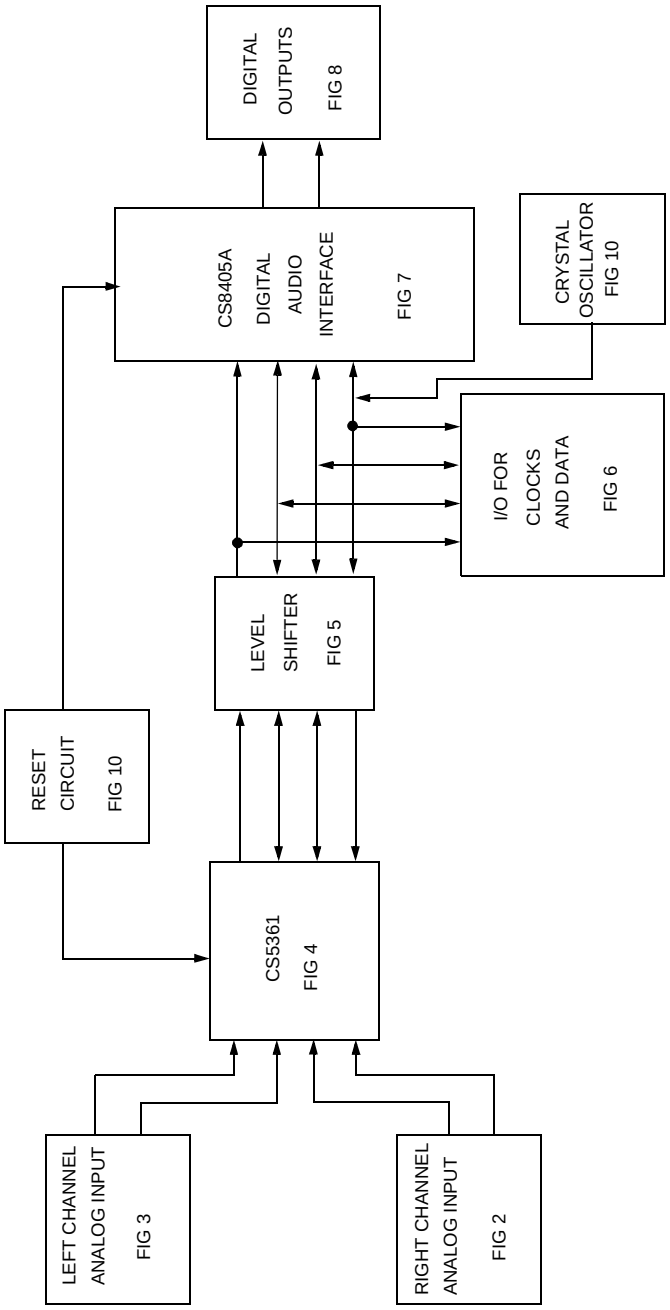

Figure 1. System Block Diagram and Signal Flow

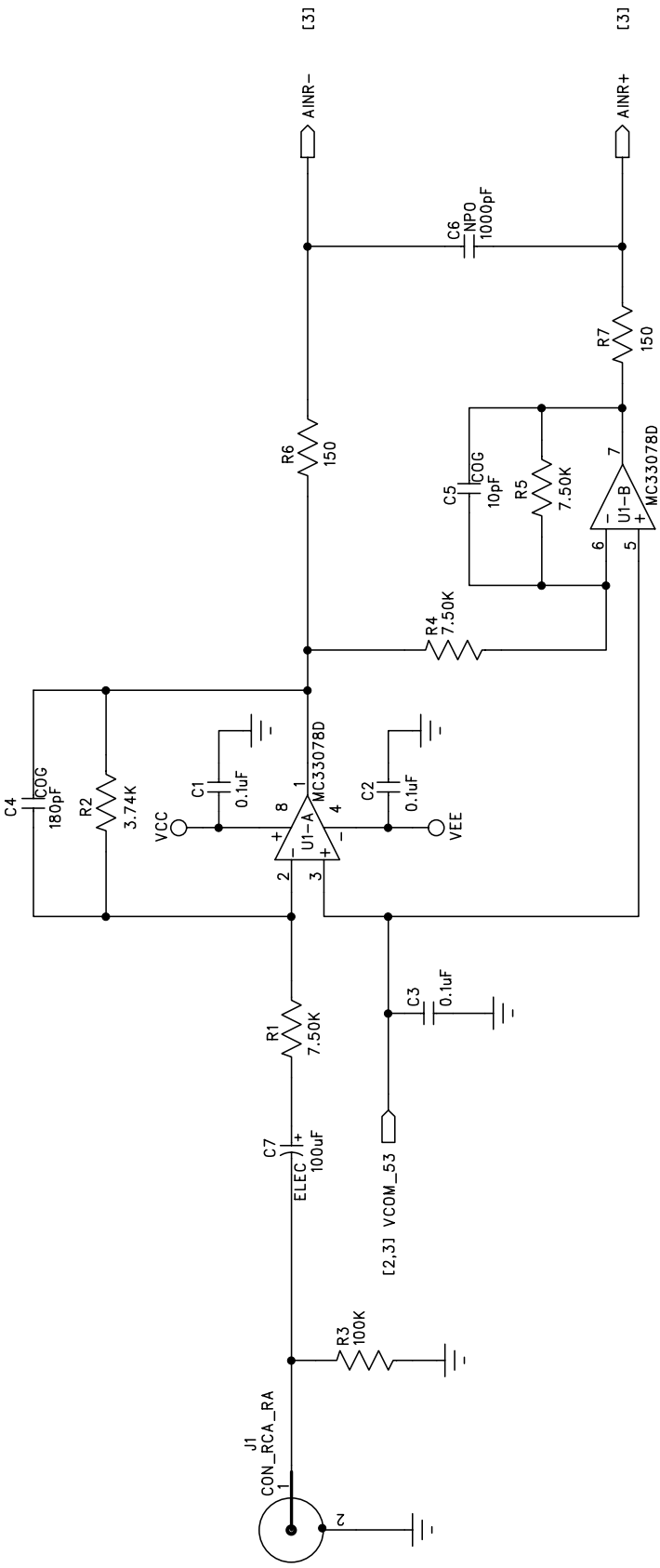

Figure 2. Right Channel Analog Audio Input

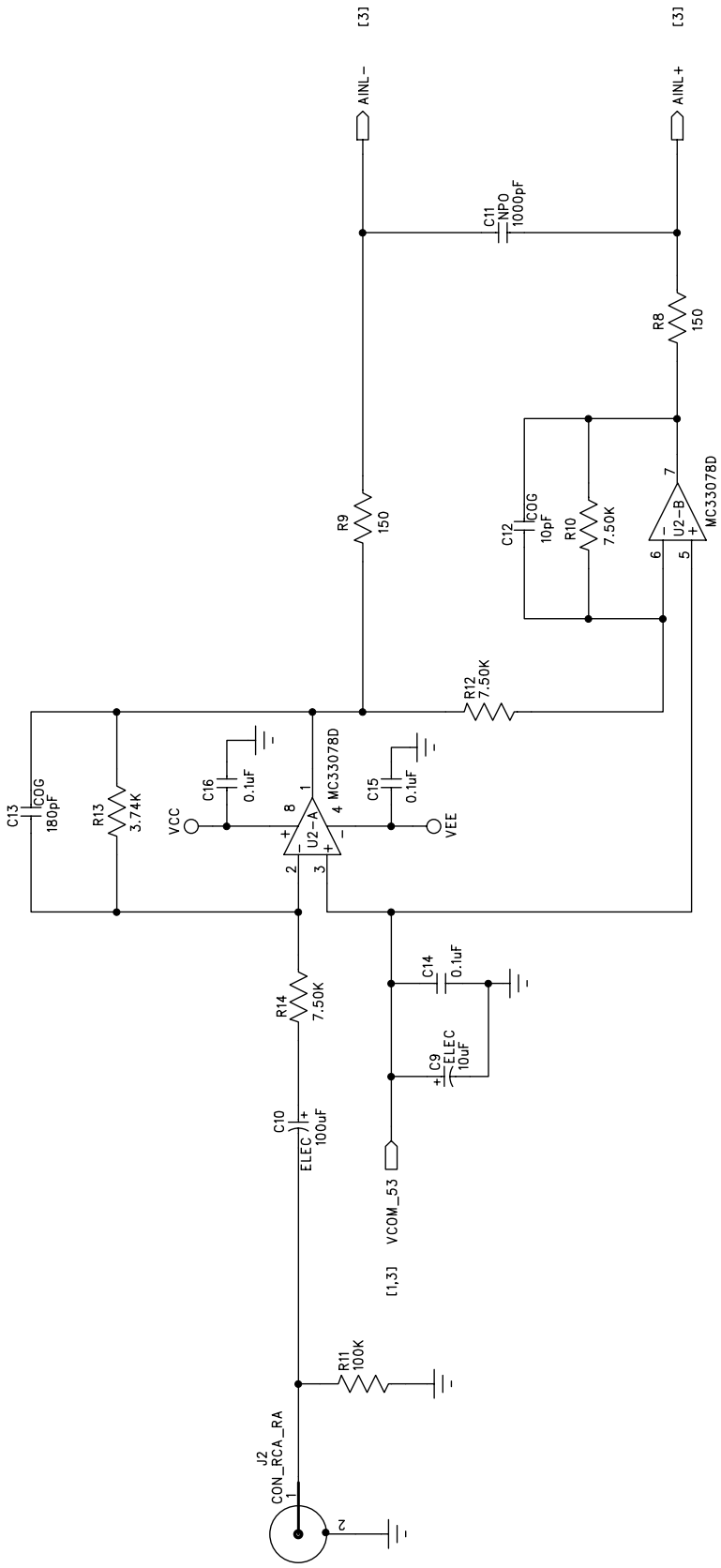

Figure 3. Left Channel Analog Audio Input

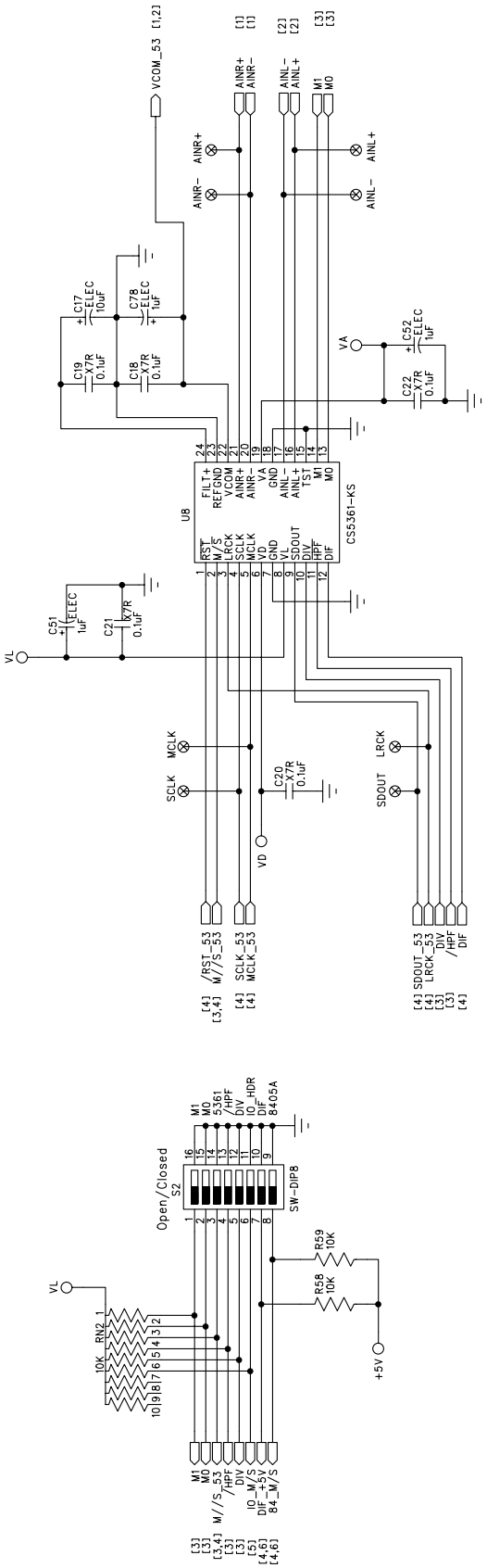

Figure 4. CS5361

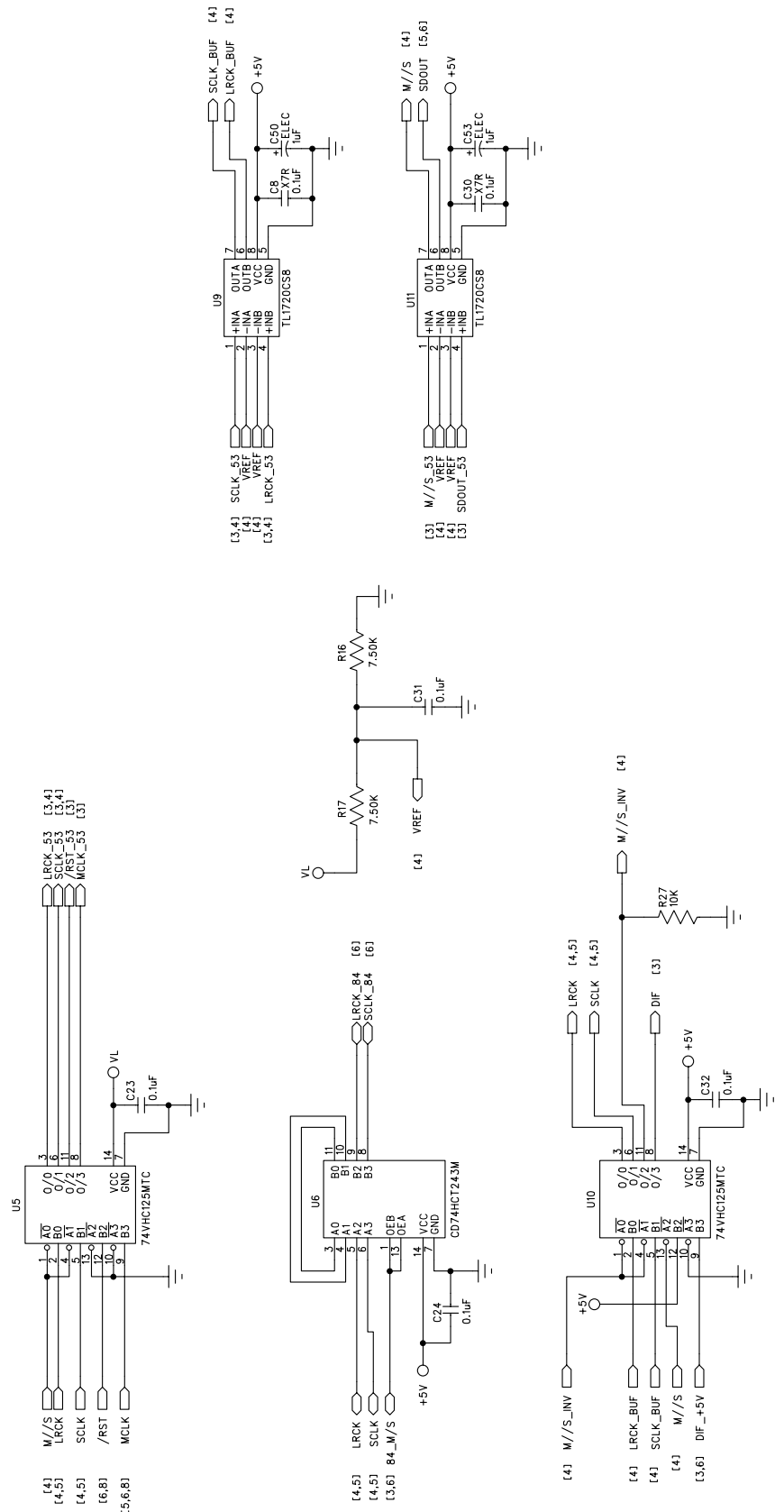

Figure 5. Level Shifters

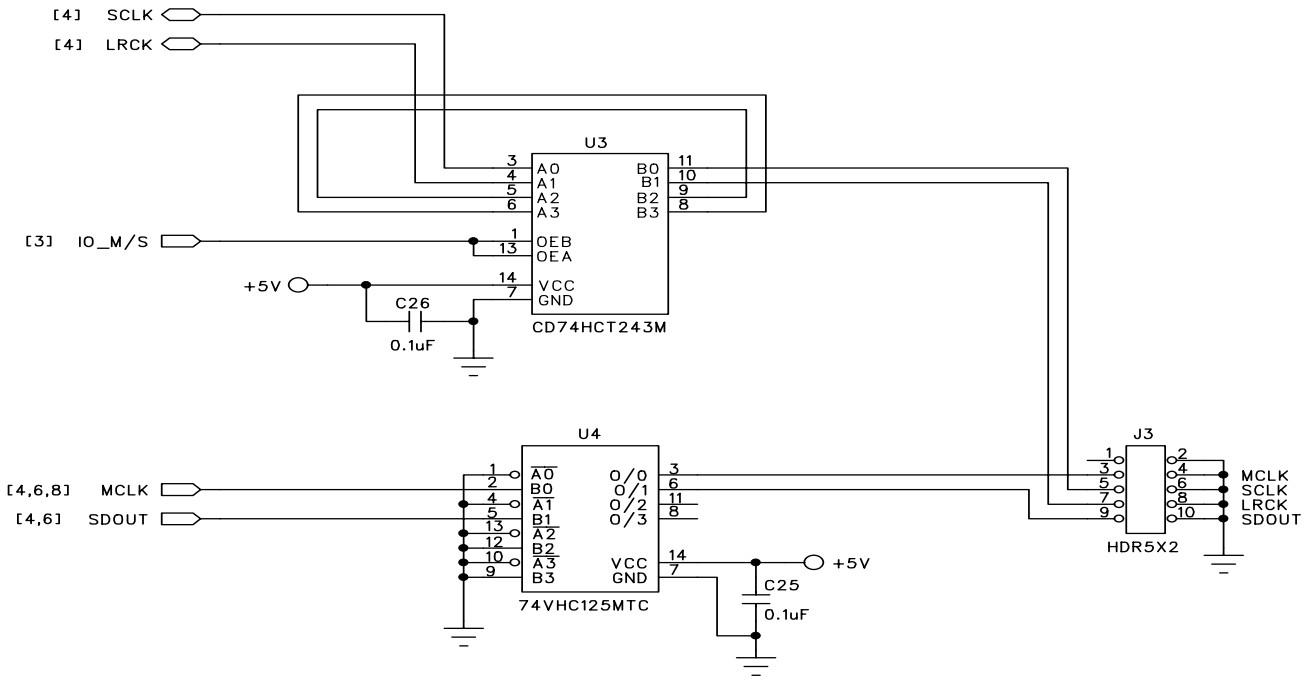

Figure 6. I/O for Clocks/Data

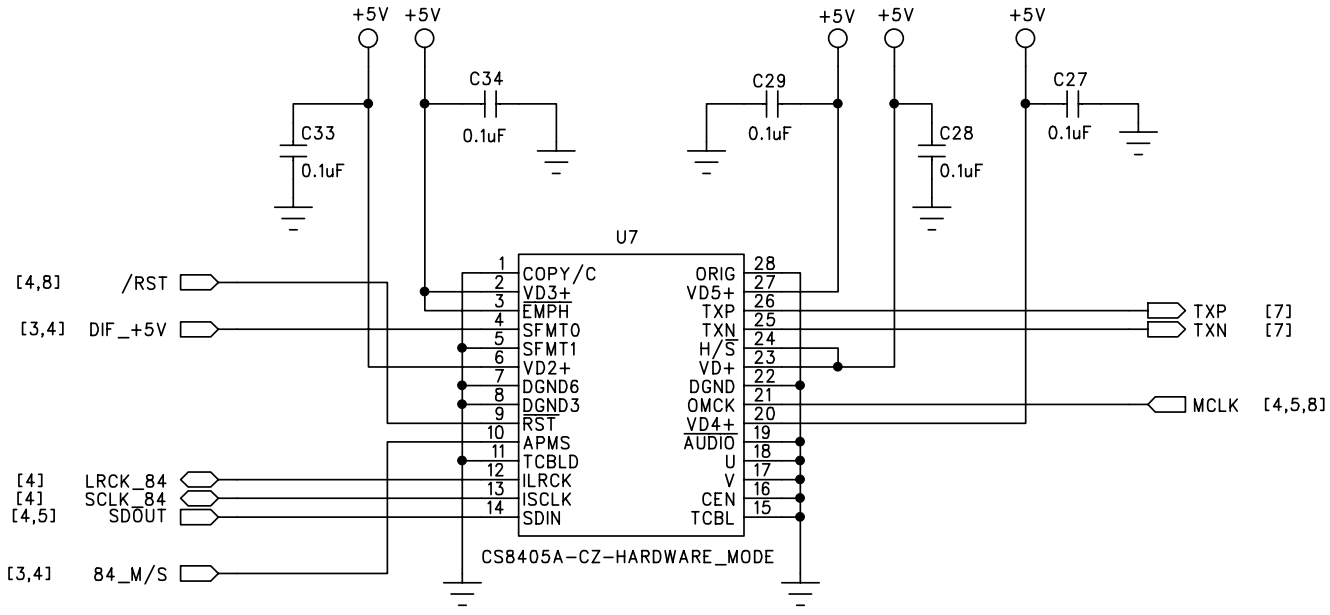

Figure 7. CS8405A Digital Audio Interface

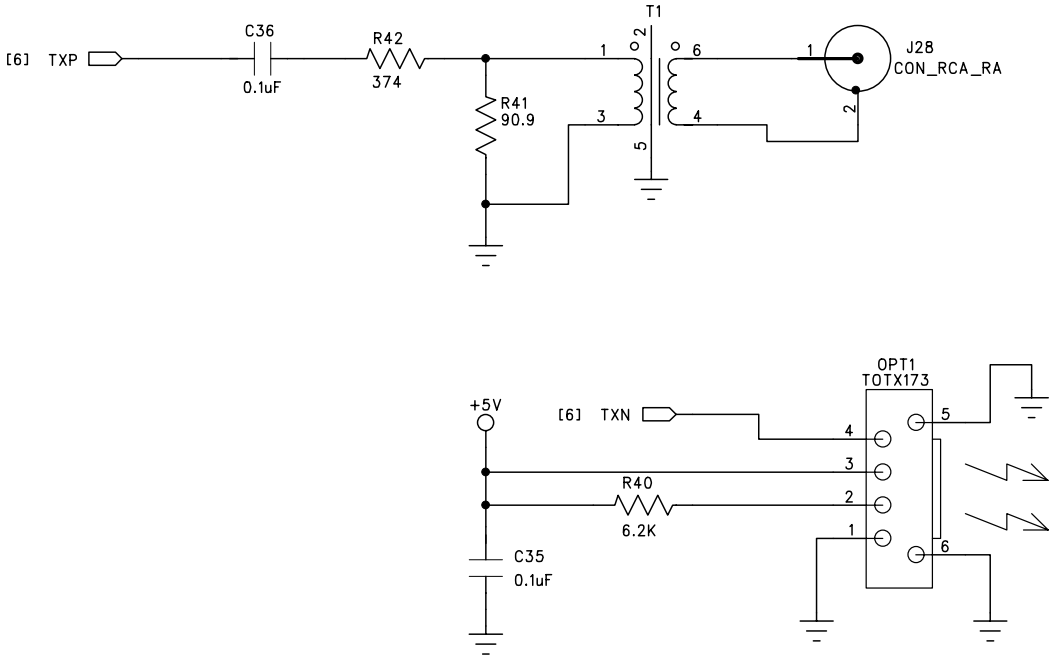

Figure 8. Digital Audio Output

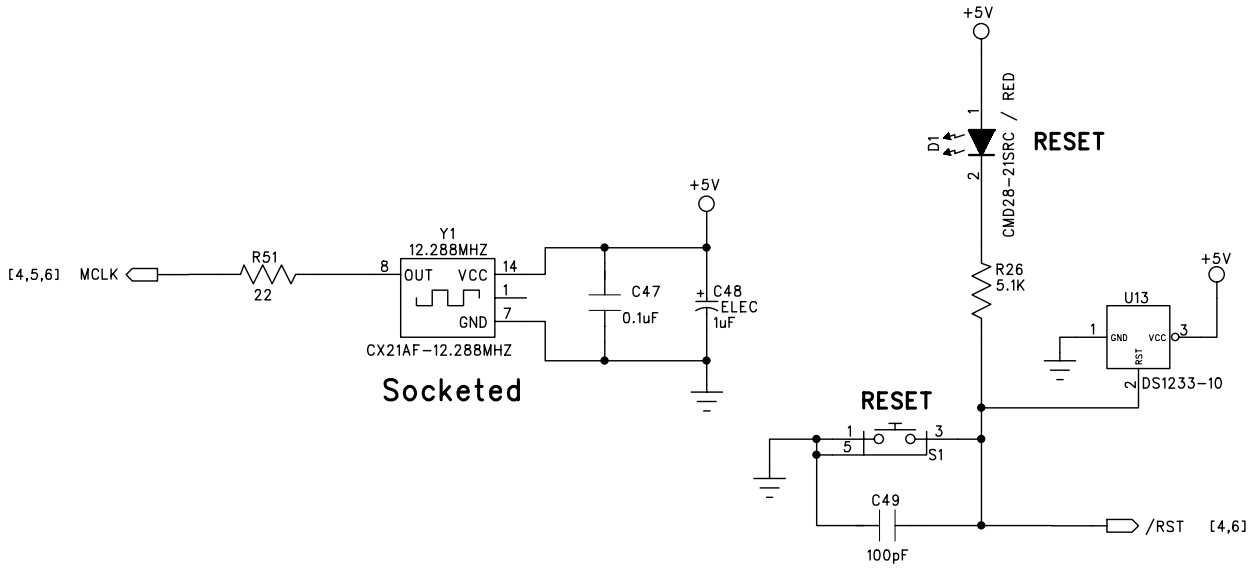

Figure 9. Reset Circuit

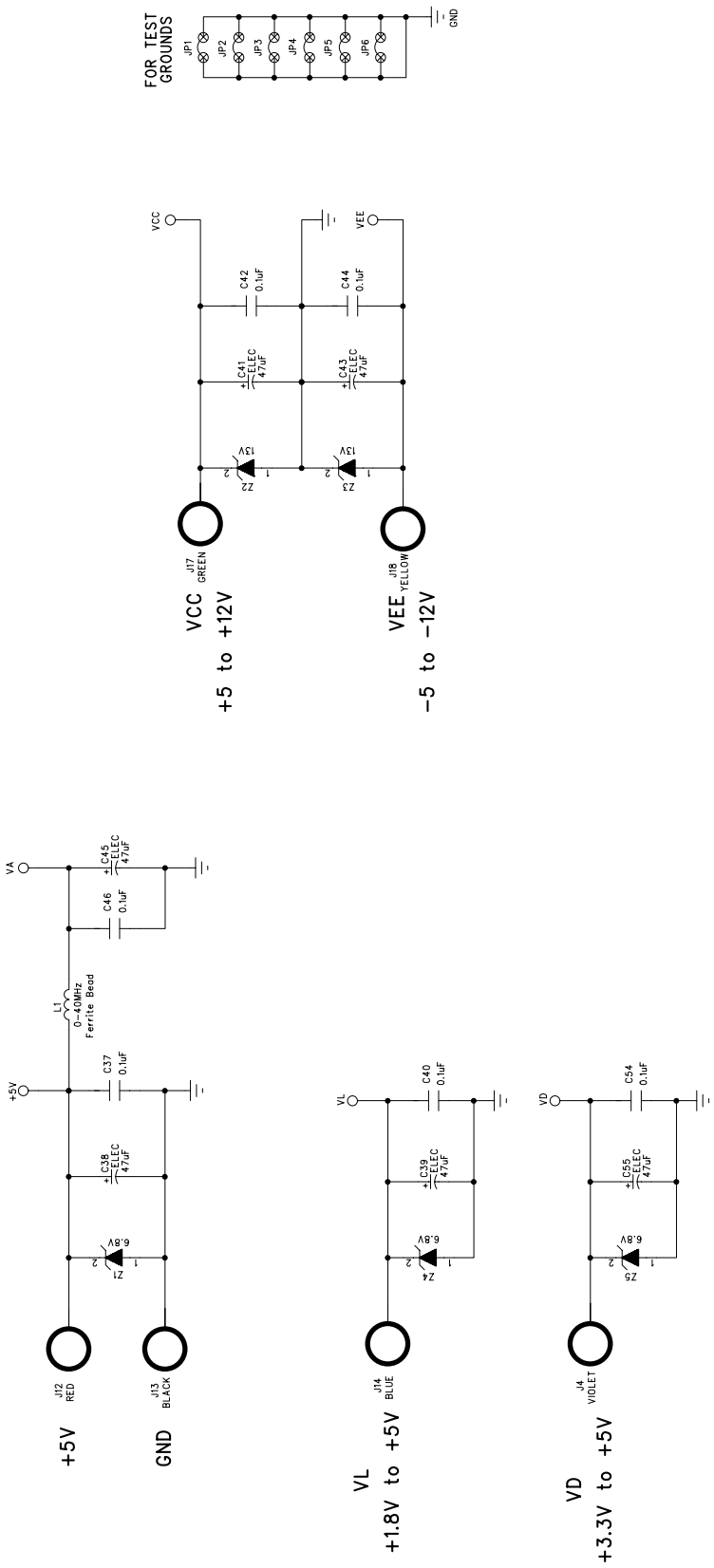

Figure 10. Power Circuit

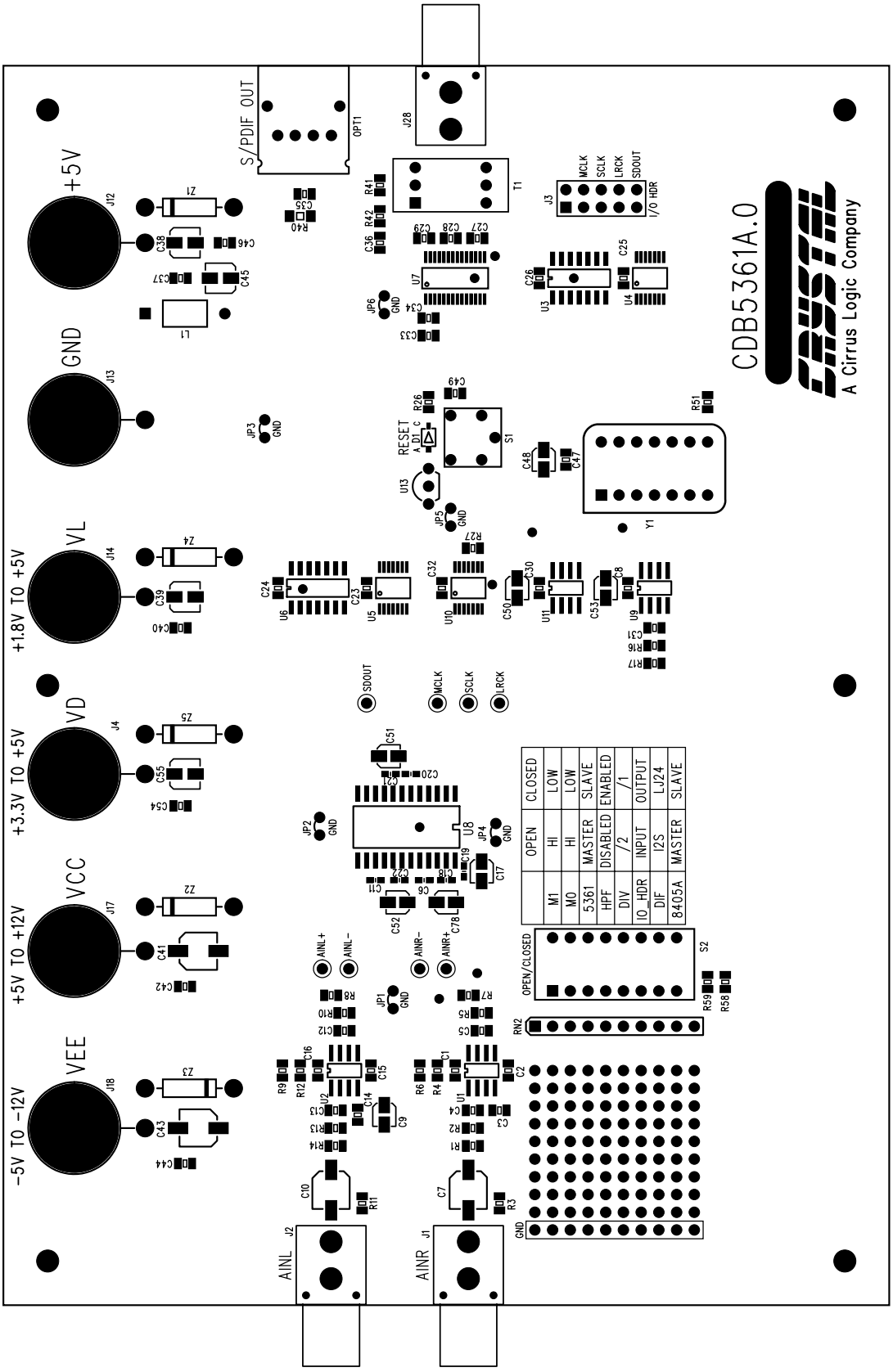

Figure 11. Top Layer Silkscreen

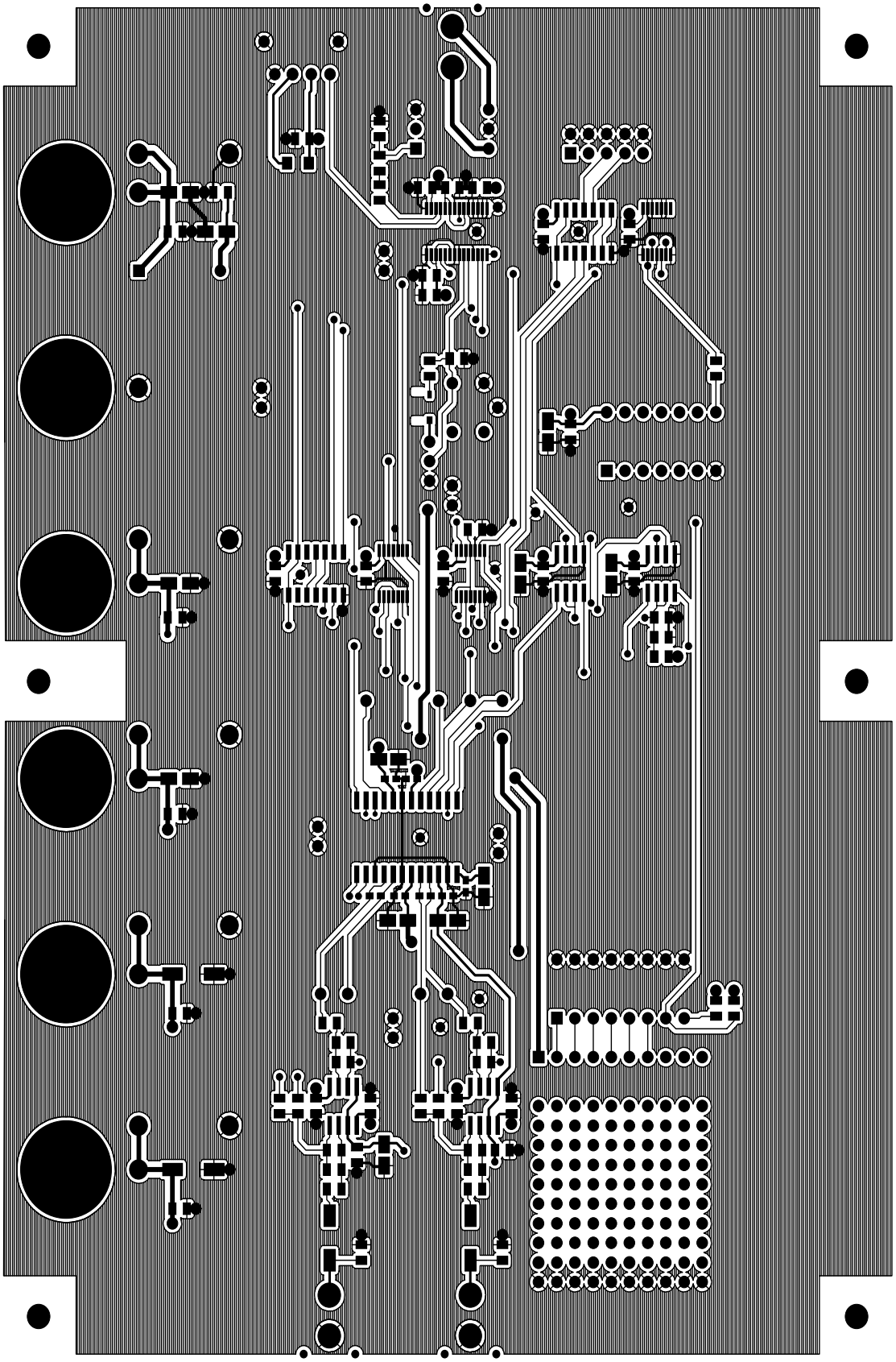

Figure 12. Top Layer

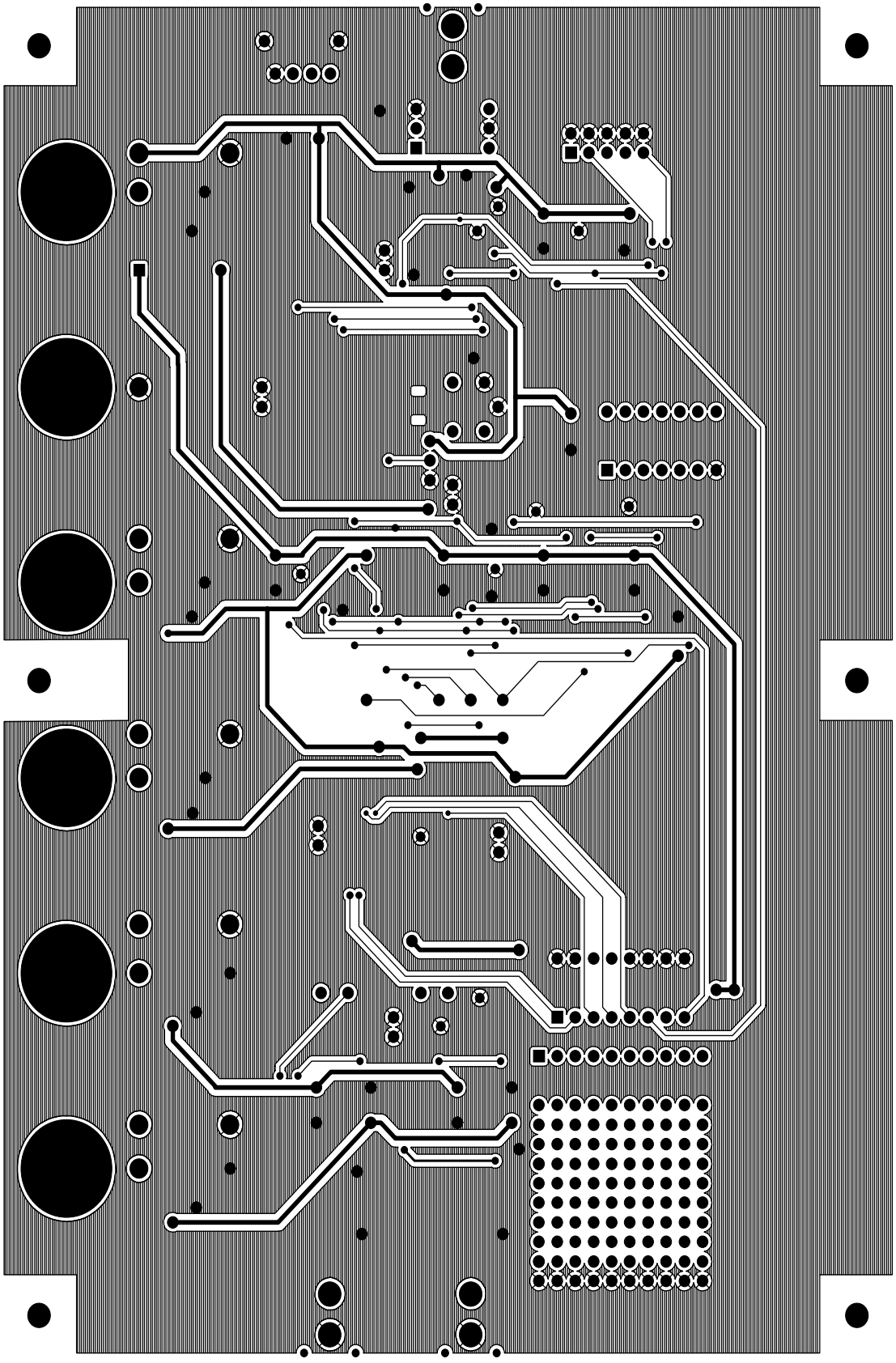

Figure 13. Bottom Layer


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