05/12/00

Errata: CS8405A-CS Rev. A Performance Update

(Reference CS8405A Data Sheet revision DS469PP1 dated Nov '99)

1. On page 9 of the data sheet it is specified that in I2C mode, SCL and SDA have a maximum rise time of 1 µS and a maximum fall time of 300 nS. The actual rise and fall times should be less than 25 nS.

2. On page 7 it is specified that the Serial Audio Ports are capable of receiving or transmitting data in slave mode at 27 MHz, if the necessary setup timing is observed. This is true as long as an additional condition is observed. There may be no more that 128 SCLK cycles per frame. This means a high-speed burst clock can be used for SCLK, but a high-speed continuous clock cannot.

3. An error in the design causes a problem if VD2+ is connected to a 3-Volt supply. VD+ and any VD pins other than VD2+ may be operated from a nominal 3-Volt supply. VD2+ needs to be connected to a 5-Volt supply. Operating the other supply pins at 3 Volts allows the part to interface directly to 3-Volt logic.

If there are any questions concerning this information,
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