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TECHNICAL DATA

DSP56005

Advance Information

24-bit Digital Signal Processor

The DSP56005 is an MPU-style general purpose Digital Signal Processor (DSP), composed of an efficient 24-bit digital signal processor core, program and data memories, various peripherals, and support circuitry. The 56000-Family-compatible DSP core is fed by a large program RAM, two independent data RAMs, and two data ROMs with sine and arc-tangent tables. Like the DSP56002, the DSP56005 contains a Serial Communication Interface (SCI), Synchronous Serial Interface (SSI), parallel Host Interface (HI), a 24-bit timer / event counter, and On-Chip Emulation (OnCE™) port. Features of the DSP56005 include the large on-chip program memory, five Pulse Width Modulators (PWM), a watchdog timer, and an address decode pin for external peripherals. This combination of features, illustrated in Figure 1, makes the DSP56005 a cost-effective, high-performance solution for many DSP and control applications, especially in high-performance motor control, optical disk drives and audio processing.

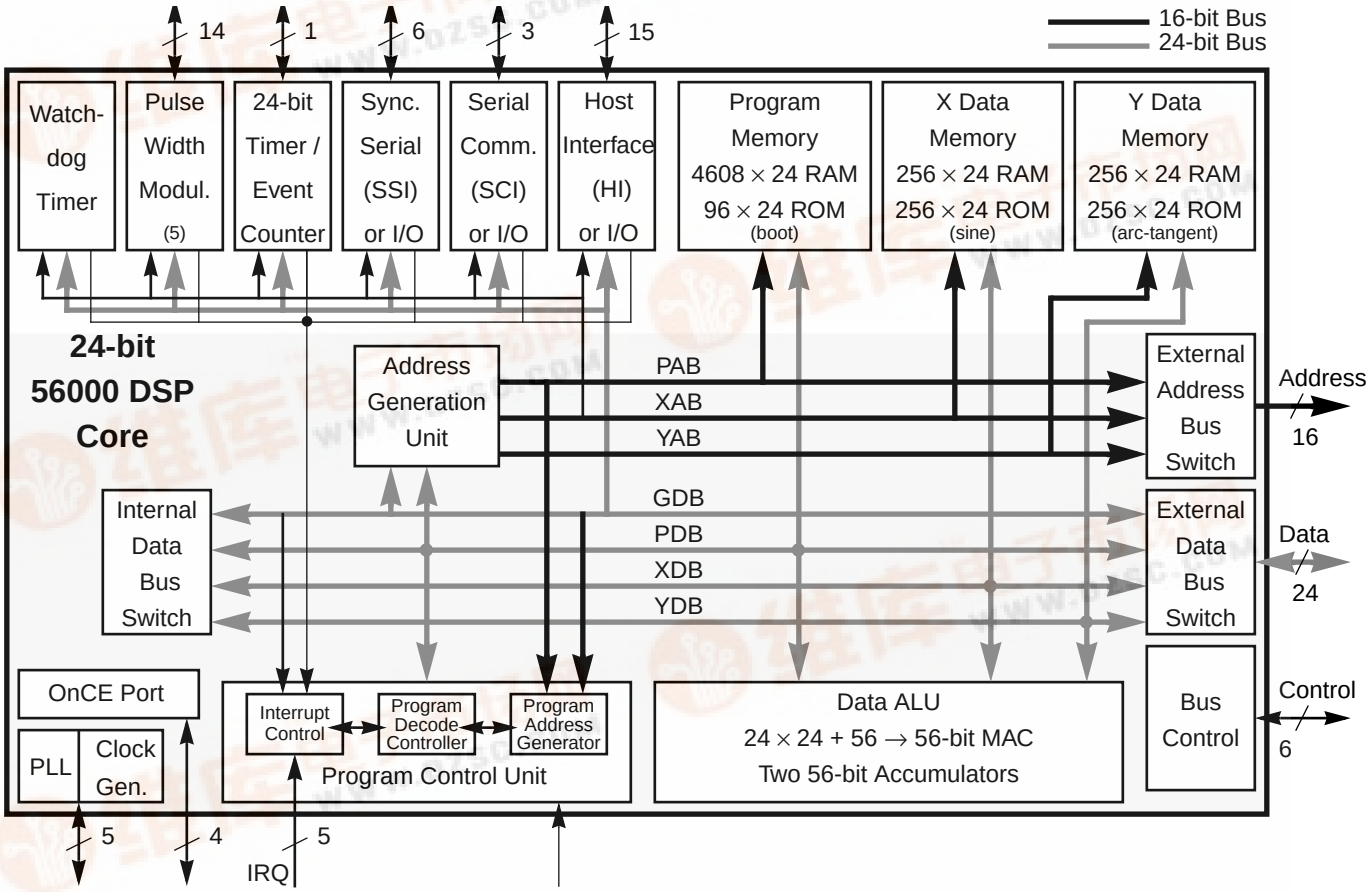

Figure 1 DSP56005 Block Diagram

DSP56005 Features

Digital Signal Processing Core

- Efficient, object code compatible, 24-bit 56000-Family DSP engine
  - — Up to 25 Million Instructions per Second (MIPS) – 40 ns instruction cycle at 50 MHz
  - — Up to 150 Million Operations per Second (MOPS) at 50 MHz
  - — Executes a 1024-point complex Fast Fourier Transform (FFT) in 59,898 clocks
  - — Highly parallel instruction set with unique DSP addressing modes
  - — Two 56-bit accumulators including extension byte
  - — Parallel 24 × 24-bit multiply-accumulate in 1 instruction cycle (2 clock cycles)
  - — Double precision 48 × 48-bit multiply with 96-bit result in 6 instruction cycles
  - — 56-bit Addition / subtraction in 1 instruction cycle
  - — Fractional arithmetic with support for multiprecision arithmetic
  - — Hardware support for block-floating point FFT
  - — Hardware nested DO loops
  - — Zero-overhead fast interrupts (2 instruction cycles)
  - — Four 24-bit internal data buses and three 16-bit internal address buses for simultaneous accesses to one program and two data memories

Memory

- On-chip Harvard architecture permitting simultaneous accesses to program and two data memories
- 4608 × 24-bit on-chip program RAM and 96 × 24-bit bootstrap ROM
- Two 256 × 24-bit on-chip data RAMs
- Two 256 × 24-bit on-chip data ROMs containing sine and arc-tangent tables
- External memory expansion with 16-bit address and 24-bit data buses
- Bootstrap loading from external data bus, Host Interface, or Serial Communications Interface

Peripheral and Support Circuits

- Byte-wide Host Interface (HI) with Direct Memory Access (DMA) support
- Synchronous Serial Interface (SSI) to communicate with codecs and synchronous serial devices
- Serial Communication Interface (SCI) for full-duplex asynchronous communications
- Five Pulse Width Modulators (PWM)
  - — Three with alternate outputs; two with open drain or TTL outputs
  - — 9- to 16-bit data width
  - — Alternate outputs independently selectable as active-high or active-low
- 24-bit timer / event counter also generates and measures digital waveforms
- 16-bit Watchdog timer

- On-chip peripheral registers memory mapped in data memory space
- Double buffered peripherals
- Up to 25 general purpose I/O pins
- Five external interrupt request pins
- On-Chip Emulation (OnCE) port for unobtrusive, processor speed-independent debugging
- Software-programmable, Phase-Locked Loop (PLL) based frequency synthesizer for the core clock
- External peripheral address decode signal

Miscellaneous Features

- Power-saving Wait and Stop modes
- Fully static, HCMOS design for operating frequencies from 50 MHz down to DC
- 144-pin Thin Quad Flat Pack (TQFP) surface-mount package; $20 \times 20 \times 1.4$ mm
- 5 V Power supply

Product Documentation

More detailed documentation is available describing the DSP56005. The three documents listed in Table 1 are required for a complete description of the DSP56005 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor or semiconductor sales office, or through a Motorola Literature Distribution Center.

Table 1 Additional DSP56005 Documentation

Document Name	Description	Order Number
DSP56000 Family Manual	Detailed description of the 56000-family architecture and the 24-bit core processor and instruction set	DSP56KFAMUM/AD
DSP56005 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56005UM/AD
DSP56005 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56005/D

Related Documentation

Table 2 lists additional documentation relevant to the DSP56005.

Table 2 DSP56005 Related Documentation

Document Name	Description	Order Number
Motorola's 16-, 24-, and 32-bit Digital Signal Processing Families	Overview of all of the DSP product families.	BR1105/D
Digital Sine-Wave Synthesis	Application Report. Uses the DSP56001 look-up table.	APR1/D
Digital Stereo 10-band Graphic Equalizer	Application Report. Includes code and circuitry; features the DSP56001.	APR2/D
Fractional and Integer Arithmetic	Application Report. Includes code.	APR3/D
Implementation of Fast Fourier Transforms	Application Report. Comprehensive FFT algorithms and code for DSP56001, DSP56156, and DSP96002.	APR4/D
Implementation of PID Controllers	Application Report. PWM using the SCI timer and three phase output using modulo addressing.	APR5/D
Convolutional Encoding and Viterbi Decoding with a V.32 Modem Trellis Example	Application Report. Theory and code; features the DSP56001.	APR6/D
Implementing IIR/FIR Filters	Application Report. Comprehensive example using the DSP56001.	APR7/D
Principles of Sigma-Delta Modulation for A-to-D Converters	Application Report. Features the DSP56ADC16; improving resolution with half-band filters	APR8/D
Full-Duplex 32-kbit/s CCITT ADPCM Speech Coding	Application Report. Features the DSP56001	APR9/D
DSP56001 Interface Techniques and Examples	Application Report. Interfaces for pseudo static RAM, dynamic RAM, ISA bus, Host	APR11/D
Twin CODEC Expansion Board for the DSP56000 ADS	Application Report. Circuit, code, FIR filter design for two voice band CODECs connecting to the SSI	APR12/D
Conference Bridging in the Digital Telecommunications Environment	Application Report. Theory and code; features the DSP56001/002	APR14/D
Implementation of Adaptive Controllers	Application Report. Adaptive control using reference models; generalized predictive control; includes code	APR15/D

Table 2 DSP56005 Related Documentation (Continued)

Document Name	Description	Order Number
Calculating Timing Requirements of External SRAM	Application Report. Determination of SRAM speed for optimum performance	APR16/D
PC Media Hardware Reference Design Version 4.0	Application Report. Audio, telephony, and entertainment board design	APR19/D
Low Cost Controller for DSP56001	Application Report. Circuit and code to connect two DSP56001s to an MC68008	APR402/D
G.722 Audio Processing	Application Report. Theory and code using SB-ADPCM	APR404/D
Minimal Logic DRAM Interface	Application Report. 1M x 480 ns DRAM, 1 PAL, code	APR405/D
Logarithmic/Linear Conversion Routines	Application Report. μ-law and A-law companding routines for PCM mono-circuits	ANE408/D
Dr. BuB Bulletin Board	Flyer. Motorola's electronic bulletin board where free DSP software is available	BR297/D
DSP Development Tools	Overview of Motorola's hardware and software development tools	DSPTOOLSP/D
Third Party Compendium	Brochures from companies selling hardware and software that supports Motorola DSPs	DSP3RDPTYPAK/D
University Support Program	Flyer. Motorola's program supporting Universities in DSP research and education	BR382/D
Technical Training Schedule	Technical Training Schedule	BR348/D
Real Time Signal Processing Applications with Motorola's DSP56000 Family	Textbook by Mohamed El-Sharkawy; 398+ pages. (This is a charge item.)	Prentice-Hall, 1990; ISBN 0-13-767138-5

Data Sheet Contents

This data sheet contains:

Data Sheet Conventions

This data sheet uses the following conventions:

- $\overline{\text{OVERBARS}}$ are used to indicate a signal that is active when pulled to ground (see Table 3) e.g. the $\overline{\text{HREQ}}$ pin is active when pulled to ground. Therefore, references to the $\overline{\text{HREQ}}$ pin will always have an overbar.
- The word “assert” (see Table 3) means that a high true (active high) signal is pulled high to V_{CC} or that a low true (active low) signal is pulled low to ground.
- The word “deassert” (see Table 3) means that a high true signal is pulled low to ground or that a low true signal is pulled high to V_{CC}.

Table 3 High True / Low True Signal Conventions

Signal/Symbol	Logic State	Signal State	Voltage
$\overline{\text{PIN}}$	True	Asserted	Ground
$\overline{\text{PIN}}$	False	Deasserted	V_{CC}
PIN	True	Asserted	V_{CC}
PIN	False	Deasserted	Ground

NOTES:

1. PIN is a generic term for any pin on the chip.
2. Ground is an acceptable low voltage level. See the DC electrical specifications for the range of acceptable low voltage levels (typically a TTL logic low).
3. V_{CC} is an acceptable high voltage level. See the DC electrical specifications for the range of acceptable high voltage levels (typically a TTL logic high).

Pin Groupings

The input and output signals of the DSP56005 are organized into function groups as shown in Table 4 and as illustrated in Figure 2.

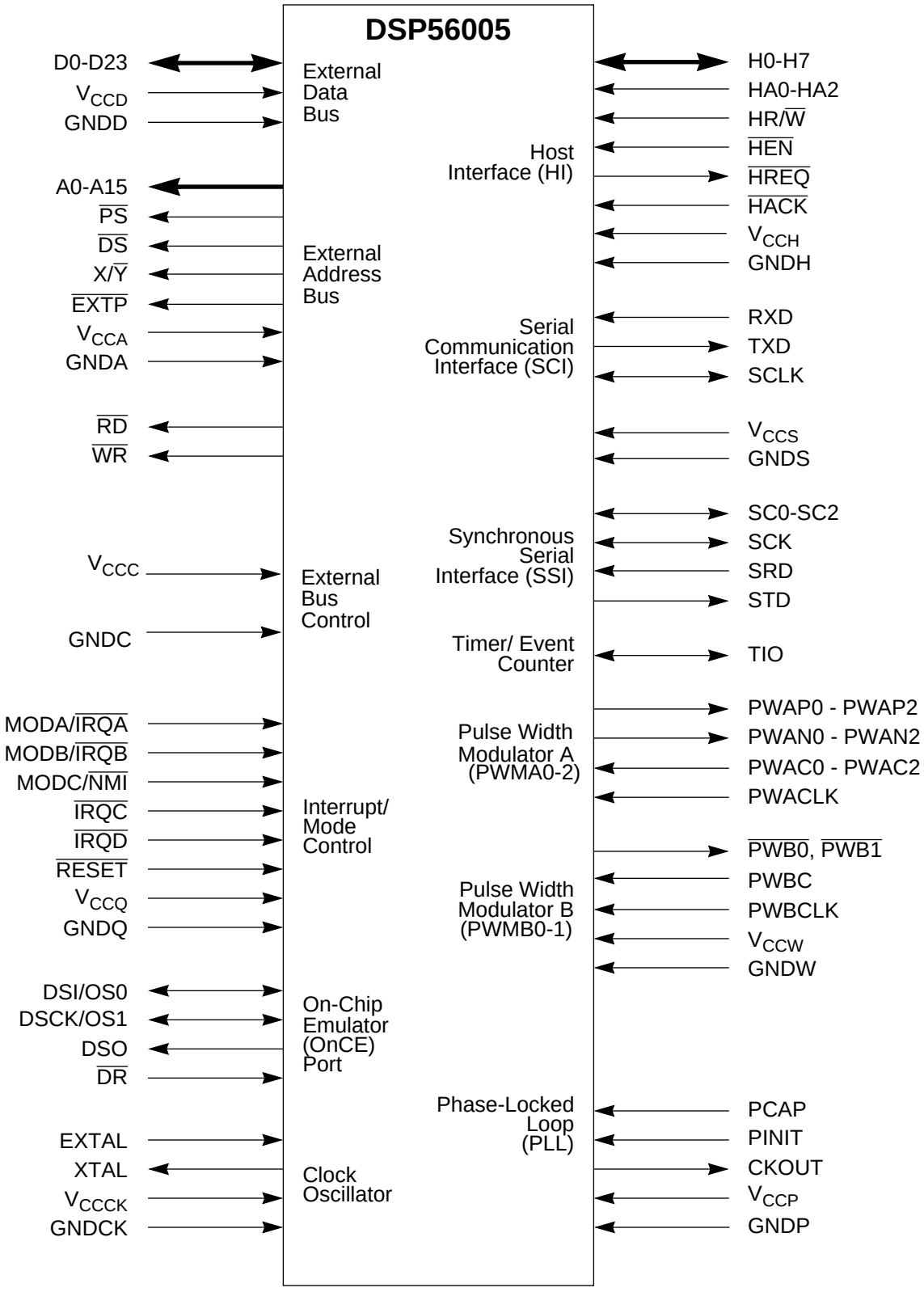

Figure 2 DSP56005 Pin Functions

Pin Descriptions

The DSP56005 is available in a 144 TQFP. The pins are organized into the functional groups indicated in Table 4. The signals are discussed in the paragraphs that follow.

All unused inputs should have pull-up resistors for two reasons:

1. floating inputs draw excessive power
2. floating input can cause erroneous operation

For example, during reset, all signals are three-stated. A pull-up resistor in the 50 kΩ range should be sufficient.

Also, for future enhancements, all reserved "no connect" (NC), pins should be left unconnected.

Address and Data Bus

The Port A address and data bus signals control the access to external memory. These signals are three-stated during reset unless noted otherwise, and may require pull-up resistors to minimize power consumption and to prevent erroneous operation.

A0–A15 (Address Bus) — three-state, outputs. A0-A15 specify the address for external program and data memory accesses. If there is no external bus activity, A0-A15 remain at their previous values. A0-A15 are three-stated during hardware reset.

D0–D23 (Data Bus) — three-state, bidirectional input/outputs. Data for external memory I/O is presented on D0-D23. If there is no external bus activity, D0-D23 are three-stated. D0-D23 are also three-stated during hardware reset.

Bus Control

The bus control signals are three-stated during reset and may require pull-up resistors to prevent erroneous operation.

$\overline{PS}$ (Program Memory Select) — three-state, active low output This output is asserted only when external program memory is referenced (see Table 5). $\overline{PS}$ timing is the same as the A0-A15 address lines. If the external bus is not used during an instruction cycle, $\overline{PS}$ is driven high. $\overline{PS}$ is three-stated during hardware reset.

$\overline{DS}$ (Data Memory Select) — three-state, active low output This three-state output is asserted only when external data memory is referenced (see Table 5). If the external bus is not used during an instruction cycle, $\overline{DS}$ is driven high. $\overline{DS}$ is three-stated during hardware reset.

X/$\overline{Y}$ (X/$\overline{Y}$ Select) — three-state output. This three-state output selects which external data memory space (X or Y) is referenced by $\overline{DS}$ (see Table 5). X/$\overline{Y}$ is three-stated during hardware reset.

$\overline{RD}$ (Read Enable) — three-state, active low output. This output is asserted during external memory read cycles. When $\overline{RD}$ is asserted, the data bus pins D0-D23 become inputs, and an external device is enabled onto the data bus. When $\overline{RD}$ is deasserted, the external data is latched inside the DSP. When $\overline{RD}$ is asserted, it qualifies the A0-A15, $\overline{PS}$ and $\overline{DS}$ pins. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a static RAM or ROM. $\overline{RD}$ is three-stated during hardware reset.

$\overline{WR}$ (Write Enable) — three-state, active low output. This output is asserted during external memory write cycles. When $\overline{WR}$ is asserted, the data bus pins D0-D23 become outputs, and the DSP puts data on the bus. When $\overline{WR}$ is deasserted, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0-A15, $\overline{PS}$ and $\overline{DS}$ pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a static RAM. $\overline{WR}$ is three-stated during hardware reset.

$\overline{EXTP}$ (External Peripheral) — active low output. The $\overline{EXTP}$ pin is an output asserted whenever the external Y memory I/O space (Y:$FFC0-$FFFF) is accessed. This signal simplifies generating peripheral enable signals. No additional circuitry is needed if only one external peripheral is used. For most applications, no more than one decode chip is needed and, as a result, decode delays are minimized. Using the Y memory I/O space allows the MOVEP instruction to be used to send and to receive data. Using the MOVEP instruction may allow the entire I/O routine to fit in a fast interrupt. $\overline{EXTP}$ is three-stated during hardware reset.

Host Interface

The following paragraphs discuss the host interface signals, which provide a convenient connection to another processor.

H0–H7 (Host Data Bus) — bidirectional. This bidirectional data bus is used to transfer data between the host processor and the DSP. This bus is an input unless enabled by a host processor read. It is high impedance when $\overline{HEN}$ is deasserted. H0-H7 may be programmed as Port B general purpose parallel I/O pins called PB0-PB7 when the Host Interface (HI) is not being used. These pins are configured as GPIO input pins during hardware reset.

HA0–HA2 (Host Address) — input.* These inputs provide the address selection for each HI register and must be stable when $\overline{HEN}$ is asserted. HA0-HA2 may be programmed as Port B general purpose parallel I/O pins called PB8-PB10 when the HI is not being used. These pins are configured as GPIO input pins during hardware reset.

*Note that these pins can be inputs or outputs when programmed as general purpose I/O.

Table 5 Program and Data Memory Select Encoding

$\overline{PS}$	$\overline{DS}$	X/$\overline{Y}$	External Memory Reference
1	1	1	No Activity
1	0	1	X Data Memory on Data Bus
1	0	0	Y Data Memory on Data Bus
0	1	1	Program Memory on Data Bus (Not an Exception)
0	1	0	External Exception Fetch: Vector or Vector +1 (Development Mode Only)
0	0	X	Reserved
1	1	0	Reserved

HR/$\overline{W}$ (Host Read/Write) — input.* This input selects the direction of data transfer for each host processor access. If HR/$\overline{W}$ is high and $\overline{HEN}$ is asserted, H0-H7 are outputs, and DSP data is transferred to the host processor. If HR/$\overline{W}$ is low and $\overline{HEN}$ is asserted, H0-H7 are inputs and host data is transferred to the DSP when $\overline{HEN}$ is deasserted. When $\overline{HEN}$ is asserted, HR/$\overline{W}$ must be stable. HR/$\overline{W}$ may be programmed as a general purpose I/O pin called PB11 when the HI is not being used. This pin is configured as a GPIO input pin during hardware reset.

$\overline{HEN}$ (Host Enable) — active low input.* This input enables a data transfer on the host data bus. When $\overline{HEN}$ is asserted and HR/$\overline{W}$ is high, H0-H7 becomes an output and DSP data may be latched by the host processor. When $\overline{HEN}$ is asserted and HR/$\overline{W}$ is low, H0-H7 is an input and host data is latched inside the DSP when $\overline{HEN}$ is deasserted. Normally a chip select signal derived from host address decoding and an enable clock is connected to the Host Enable. $\overline{HEN}$ may be programmed as a general purpose I/O pin called PB12 when the HI is not being used. This pin is configured as a GPIO input pin during hardware reset.

$\overline{HREQ}$ (Host Request) — active low output.* This open-drain output signal is used by the DSP to request service from the host processor. $\overline{HREQ}$ may be connected to a host processor interrupt request pin, a DMA controller transfer request pin, or a control input to external circuitry. $\overline{HREQ}$ is asserted when an enabled request occurs in the HI. $\overline{HREQ}$ is deasserted when the enabled request is cleared or masked, DMA $\overline{HACK}$ is asserted, or the DSP is reset. $\overline{HREQ}$ may be programmed as a general purpose I/O pin (not open-drain) called PB13 when the HI is not being used. This pin is configured as a GPIO input pin during hardware reset.

$\overline{HACK}$ (Host Acknowledge) — active low input.* This input has two functions:

- to provide a host acknowledge signal for DMA transfers
- to control handshaking and to provide a host interrupt acknowledge compatible with MC68000 family processors

If programmed as a host acknowledge signal, $\overline{HACK}$ may be used as a data strobe for HI DMA data transfers. If programmed as an MC68000 host interrupt acknowledge, $\overline{HACK}$ enables the HI Interrupt Vector Register (IVR) onto the host data bus H0-H7 if the Host Request $\overline{HREQ}$ output is asserted. In this case, all other HI control pins are ignored and the HI state is not affected. $\overline{HACK}$ may be programmed as a general purpose I/O pin called PB14 when the HI is not being used. This pin is configured as a GPIO input pin during hardware reset.

NOTE: $\overline{HACK}$ should always be pulled high when not in use.

Serial Communication Interface (SCI)

RXD (Receive Data) — input.* This input receives byte-oriented data and transfers the data to the SCI receive shift register. Input data is sampled on the

*Note that these pins can be inputs or outputs when programmed as general-purpose I/O.

positive or the negative edge of the receive clock, depending on how the SCI control register is programmed. RXD may be programmed as a general-purpose I/O pin called PC0 when it is not being used as an SCI pin. This pin is configured as a GPIO input pin during hardware reset.

TXD (Transmit Data) — output.* This output transmits serial data from the SCI transmit shift register. Data changes on the negative edge of the transmit clock. This output is stable on the positive or the negative edge of the transmit clock, depending on how the SCI control register is programmed. TXD may be programmed as a general-purpose I/O pin called PC1 when the SCI TXD function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SCLK (SCI Serial Clock) — bidirectional. This bidirectional pin provides an input or output clock from which the transmit and/or receive baud rate is derived in the asynchronous mode, and from which data is transferred in the synchronous mode. SCLK may be programmed as a general-purpose I/O pin called PC2 when the SCI SCLK function is not being used. This pin is configured as a GPIO input pin during hardware reset.

Synchronous Serial Interface (SSI)

SC0 (Serial Control 0) — bidirectional. This bidirectional pin's function is determined by whether the SSI is in synchronous or asynchronous mode. In synchronous mode, this pin is used for serial flag I/O. In asynchronous mode, this pin receives clock I/O. SC0 and SC1 are independent serial I/O flags but may be used together for multiple serial device selection. SC0 may be programmed as a general-purpose I/O pin called PC3 when the SSI SC0 function is not used. This pin is configured as a GPIO input pin during hardware reset.

SC1 (Serial Control 1) — bidirectional. The SSI uses this bidirectional pin to control flag or frame synchronization. This pin's function is determined by whether the SSI is in synchronous or asynchronous mode. In asynchronous mode, this pin is frame sync I/O. For synchronous mode with continuous clock, this pin is serial flag SC1 and operates like the SC0. SC0 and SC1 are independent serial I/O flags but may be used together for multiple serial device selection. SC1 may be programmed as a general-purpose I/O pin called PC4 when the SSI SC1 function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SC2 (Serial Control 2) — bidirectional. The SSI uses this bidirectional pin to control frame synchronization only. As with SC0 and SC1, its function is defined by the SSI operating mode. SC2 may be programmed as a general-purpose I/O pin called PC5 when the SSI SC2 function is not being used. This pin is configured as a GPIO input pin during hardware reset.

SCK (SSI Serial Clock) — bidirectional. This bidirectional pin provides the serial bit rate clock for the SSI when only one clock is being used. SCK may be

*These pins can be input or output when programmed as general-purpose I/O.

programmed as a general-purpose I/O pin called PC6 when it is not needed as an SSI pin. This pin is configured as a GPIO input pin during hardware reset.

SRD (SSI Receive Data) — input.* This input pin receives serial data into the SSI receive shift register. SRD may be programmed as a general-purpose I/O pin called PC7 when the SRD function is not being used. This pin is configured as a GPIO input pin during hardware reset.

STD (SSI Transmit Data) — output.* This output pin transmits serial data from the SSI transmit shift register. STD may be programmed as a general-purpose I/O pin called PC8 when the STD function is not being used. This pin is configured as a GPIO input pin during hardware reset.

Timer/Event Counter

TIO (Timer/Event Counter Input/Output) — bidirectional. The TIO pin provides an interface to the Timer/Event Counter module. When the module functions as an external event counter or is used to measure an external pulse width/signal period, the TIO is used as an input. When the module functions as a timer, the TIO is an output and the signal on the TIO pin is the timer pulse. When not used by the timer module, the TIO can act as a general purpose I/O pin. Reset disables the TIO pin and causes it to be three-stated.

Pulse Width Modulator A (PWMA)

Pulse Width Modulator A is a set of three 16-bit signed two's complement fractional data pulse width modulators and has 10 dedicated external pins. These pulse width modulators are independent of the PWMB modulators.

PWAP0 - PWAP2 (Pulse Width Modulator A Positive) — output. These three pins are the positive outputs for the three PWMA modulators (PWMA0, PWMA1, and PWMA2). When a positive two's complement number is loaded in one of the three PWMA Count Registers, an output signal will be generated on the respective pin (e.g., loading PWACR0 with a positive two's complement number will generate an output on PWAP0).

When a negative two's complement number is loaded in a PWMA Count Register, PWAP0-PWAP2 will be at its inactive logic level (as defined by the polarity bits in the PWMA Control/Status Register 1). These pins are driven at their inactive logic level (as defined by the polarity bits in the Control/Status Register 1) when the individual PWM modulator (PWMA0, PWMA1, or PWMA2) is not enabled. During hardware reset, these pins are driven to a high logic level.

PWAN0 - PWAN2 (Pulse Width Modulator A Negative) — output. These three pins are the negative outputs for the three PWMA modulators (PWMA0, PWMA1, and PWMA2). When a negative two's complement number is loaded in one of the three PWMA Count Registers, an output signal will be generated on the respective pin (e.g. loading PWACR0 with a negative two's

***** These pins can be input or output when programmed as general purpose I/O.

complement number will generate an output on PWAN0).

When a positive two's complement number is loaded in a PWMA Count Register, the N-output (PWAN0-PWAN2) of this PWMA block will be at its inactive logic level (as defined by the polarity bits in the PWMA Control/Status Register 1). These pins are driven at their inactive logic level (as defined by the polarity bits in the Control/Status Register 1) when the individual PWM modulator (PWMA0, PWMA1, or PWMA2) is not enabled. During hardware reset, these pins are driven to a high logic level.

PWAC0 - PWAC2 (Pulse Width Modulator A Carrier) — input. These three pins are inputs that provide the external carrier signals for the three PWMAs (PWMA0, PWMA1 and PWMA2). When the carrier source for the respective PWMA block is programmed to be external, the modulator starts operation at each rising edge of its carrier signal. While a PWMA block is either disabled, or is enabled and programmed to operate with the internal carrier, its respective internal input buffer is disconnected from the pin and no external pull-up is necessary.

PWACLK (Pulse Width Modulator A Clock) — input. This input increments the prescaler which connects to the three PWMA blocks and increments the counter in each these blocks. If all of the PWMA blocks are either disabled, or are programmed to use the internal clock, the internal input buffer is disconnected from the pin and no external pull-up is necessary.

Pulse Width Modulator B (PWMB)

Pulse Width Modulator B is a pair 16-bit positive fractional data pulse width modulators and has four dedicated external pins. These two pulse width modulators are independent of the PWMA modulators.

PWBC (Pulse Width Modulator B Carrier) — input. This pin is an input that provides the external carrier signals for the two PWMB blocks (PWMB0 and PWMB1). When the carrier source for these blocks is programmed to be external, these blocks start operation at each rising edge of this signal. While a PWMB block is either disabled, or is enabled and programmed to operate with the internal carrier, its respective internal input buffer is disconnected from the pin and no external pull-up is necessary.

$\overline{\text{PWB0}}$-$\overline{\text{PWB1}}$ (Pulse Width Modulator B Output) — active low output. These two pins are the outputs for pulse width modulators PWMB0 and PWMB1. These pins are either open drain or driven at TTL levels depending on the programming of PWBCSR1 bit 14 (WBR0). These pins are also in the high-impedance state or in a high logic state (depending on the value of the bit WBO in PWBCSR1) when PWMB0 and PWMB1 are disabled. During hardware reset, these pins are in the high-impedance state.

PWBCLK (Pulse Width Modulator B Clock) — input. This input increments the prescaler which increments the counter connected to the two PWMB blocks. While both PWMB blocks are disabled, the internal input buffer is disconnected from the pin and no external pull-up

is necessary. While the PWMB blocks are programmed to use the internal clock, the internal input buffer is disconnected from the pin and no external pull-up is necessary.

On-Chip Emulation (OnCE™) Port

The following paragraphs describe the pins associated with the OnCE Port controller and its serial interface.

DSI/OS0 (Debug Serial Input/Chip Status 0) — bidirectional. The DSI/OS0 pin, when an input, is the pin through which serial data or commands are provided to the OnCE port controller. The data received on the DSI pin will be recognized only when the DSP has entered the debug mode of operation. Data must have valid TTL logic levels before the serial clock falling edge. Data is always shifted into the OnCE serial port most significant bit (MSB) first. When the DSP is not in the debug mode, the DSI/OS0 pin provides information about the chip status if it is an output and used in conjunction with the OS1 pin. When switching from output to input, the pin is three-stated. During hardware reset, this pin is defined as an output and it is driven low.

NOTE: To avoid possible glitches, an external pull-down resistor should be attached to this pin.

DSCK/OS1(Debug Serial Clock/Chip Status 1) — bidirectional. The DSCK/OS1 pin, when an input, is the pin through which the serial clock is supplied to the OnCE port. The serial clock provides pulses required to shift data into and out of the OnCE serial port. Data is clocked into the OnCE port on the falling edge and is clocked out of the OnCE serial port on the rising edge. If the DSCK/OS1 pin is an output and used in conjunction with the OS0 pin, it provides information about the chip status when the DSP is not in the debug mode. The debug serial clock frequency must be no greater than $^{1}/_{8}$ of the processor clock frequency. The pin is three-stated when it is changing from input to output. During hardware reset, this pin is defined as an output and is driven low.

NOTE: To avoid possible glitches, an external pull-down resistor should be attached to this pin.

DSO (Debug Serial Output) — output. The debug serial output provides the data contained in one of the OnCE port controller registers as specified by the last command received from the command controller. The most significant bit (MSB) of the data word is always shifted out of the OnCE serial port first. Data is clocked out of the OnCE Port serial port on the rising edge of DSCK.

The DSO pin also provides acknowledge pulses to the external command controller. When the chip enters the debug mode, the DSO pin will be pulsed low to indicate (acknowledge) that the OnCE Port is waiting for commands. After receiving a read command, the DSO pin will be pulsed low to indicate that the requested data is available and the OnCE Port serial port is ready to receive clock pulses in order to deliver the data. After receiving a write command, the DSO pin will be pulsed low to indicate that the OnCE serial port is ready to receive the data to be written;

after the data is written, another acknowledge pulse will be provided.

During hardware reset and when idle, the DSO pin is held high.

$\overline{DR}$ (Debug Request) — active low input. The debug request input provides a means of entering the debug mode of operation. This pin, when asserted, will cause the DSP to finish the current instruction being executed, to save the instruction pipeline information, to enter the debug mode, and to wait for commands to be entered from the debug serial input line. While the DSP is in the debug mode, the user can reset the OnCE Port controller by asserting $\overline{DR}$, waiting for an acknowledge from DSO, and then deasserting $\overline{DR}$. It may be necessary to reset the OnCE Port controller in cases where synchronization between the OnCE Port controller and external circuitry is lost. Asserting $\overline{DR}$ when the DSP is in the Wait or the Stop state, and keeping it asserted until an acknowledge pulse in the DSP is produced, sends the DSP into the debug mode. After receiving the acknowledge, $\overline{DR}$ must be deasserted before sending the first OnCE Port command. Power and Ground

NOTE: To avoid possible glitches, an external pull-up resister should be attached to this pin

The power and ground pins are presented in the following paragraphs. There are ten sets of power and ground pins (see Table 25). In accordance with good engineering practice, V_{CC} should be bypassed to ground (as needed) by a 0.1 µF capacitor located as close as possible to the chip package. The two circuits where this bypassing is most important are the PLL and the core processor internal logic circuits.

Power

These V_{CC} pins provide power to the circuits listed in Table 25, “DSP56005 Power Supply Pins,” on page 77. The voltage should be well regulated and the pin should be provided with an extremely low impedance path to the power rail.

V_{CCP} (PLL Circuit Power). This pin supplies a quiet power source to the Phase-Locked Loop (PLL) to provide greater frequency stability. The voltage should be well regulated and the pin should be provided with an extremely low impedance path to the power rail. V_{CCP} should be bypassed to GNDP by a 0.1 µF capacitor located as close as possible to the chip package.

Ground

These pins provide grounds for the circuits listed in Table 25, “DSP56005 Power Supply Pins,” on page 77. The pins should be provided with an extremely low impedance path to ground.

GNDP (PLL Circuit Ground). This pin supplies a quiet ground source to the PLL to provide greater frequency stability. The pin should be provided with an extremely low impedance path to ground. V_{CCP} should be bypassed to GNDP by a 0.1 µF capacitor located as close as possible to the chip package.

Interrupt and Mode Control

The interrupt and mode control pins select the chip’s operating mode as it comes out of hardware reset and receive interrupt requests from external sources after reset.

MODA/$\overline{\text{IRQA}}$ (Mode Select A/External Interrupt Request A) — input. This input pin has three functions:

- to work with the MODB and MODC pins to select the chip's initial operating mode
- to allow an external device to request a DSP interrupt after internal synchronization
- to turn on the internal clock generator when the DSP in the Stop processing state, causing the chip to resume processing

MODA is read and internally latched in the DSP when the processor exits the reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODA pin changes to the external interrupt request $\overline{\text{IRQA}}$. The chip operating mode can be changed by software after reset.

The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request. It may be programmed to be level sensitive or negative edge triggered. When the signal is edge triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{\text{IRQA}}$ will generate multiple interrupts also increases.

While the DSP is in the Stop processing state, asserting $\overline{\text{IRQA}}$ gates on the oscillator and, after a clock stabilization delay, enables clocks to the processor and peripherals. Hardware reset causes this input to act as MODA.

MODB/$\overline{\text{IRQB}}$ (Mode Select B/External Interrupt Request B) — input. This input pin has two functions:

- to work with the MODA and MODC pins to select the chip's initial operating mode
- to allow an external device to request a DSP interrupt after internal synchronization

MODB is read and internally latched in the DSP when the processor exits the reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODB pin changes to the external interrupt request $\overline{\text{IRQB}}$. The chip operating mode can be changed by software after reset.

The $\overline{\text{IRQB}}$ input is a synchronized external interrupt request. It may be programmed to be level sensitive or negative edge triggered. When the signal is edge triggered, triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{\text{IRQB}}$ will generate multiple interrupts also increases.

Hardware reset causes this input to act as MODB.

MODC/$\overline{\text{NMI}}$ (Mode Select C/Non-Maskable Interrupt Request) — edge triggered input. This input pin has two functions:

- to work with the MODA and MODB pins to select the chip's initial operating mode
- to allow an external device to request a DSP interrupt after internal synchronization

MODC is read and internally latched in the DSP when the processor exits the reset state. MODA, MODB, and MODC select the initial chip operating mode. Several clock cycles after leaving the reset state, the MODC pin changes to the non-maskable interrupt request, $\overline{\text{NMI}}$. The chip operating mode can be changed by software after reset.

The $\overline{\text{NMI}}$ input is a negative-edge triggered external interrupt request. This is a level 3 interrupt that can not be masked out. Triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{\text{NMI}}$ will generate multiple interrupts also increases. Hardware reset causes this input to act as MODC.

$\overline{\text{IRQC}}$ (External Interrupt Request C) — edge triggered input. This negative edge triggered input allows an external device to request a DSP interrupt after internal synchronization. Triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{\text{IRQC}}$ will generate multiple interrupts also increases.

$\overline{\text{IRQD}}$ (External Interrupt Request D) — edge triggered input. This negative edge triggered input allows an external device to request a DSP interrupt after internal synchronization. Triggering occurs at a voltage level and is not directly related to the fall time of the interrupt signal. However, as the fall time of the interrupt signal increases, the probability that noise on $\overline{\text{IRQD}}$ will generate multiple interrupts also increases.

$\overline{\text{RESET}}$ (Reset) — input. This input is a direct hardware reset of the processor. When $\overline{\text{RESET}}$ is asserted, the DSP is initialized and placed in the reset state. A Schmitt trigger input is used for noise immunity. When the reset pin is deasserted, the initial chip operating mode is latched from the MODA, MODB, and MODC pins. The chip also samples the PINIT pin and writes its status into the PEN bit of the PLL Control Register. When the chip comes out of the reset state, deassertion occurs at a voltage level and is not directly related to the rise time of the $\overline{\text{RESET}}$ signal. However, the probability that noise on $\overline{\text{RESET}}$ will generate multiple resets increases with increasing rise time of the $\overline{\text{RESET}}$ signal.

Clock, Oscillator, and PLL

The following pins are dedicated to the PLL, clock, and oscillator operation.

CKOUT (Output Clock) — output. This output pin provides a 50% duty cycle output clock synchronized to the internal processor clock when the PLL is enabled and locked. When the PLL is disabled, the output clock at CKOUT is derived from, and has the same frequency and duty cycle as, EXTAL.

NOTE: If the PLL is enabled and the multiplication factor is less than or equal to 4, then CKOUT is synchronized to EXTAL. (For information on the DSP56005's PLL multiplication factor, see Section 3.5 — DSP56005 Phase-Locked Loop Configuration in the *DSP56005 User's Manual.*

EXTAL (External Clock/Crystal) — input. This pin may be used in one of two ways:

- driven from an external clock
- interface the internal crystal oscillator input to an external crystal circuit

If the PLL is enabled, this pin is internally connected to the on-chip PLL. The PLL can multiply the frequency on the EXTAL pin to generate the internal DSP clock. The PLL output is divided by two to produce a four-phase instruction cycle clock, with the minimum instruction time being two PLL output clock periods. If the PLL is disabled, EXTAL is divided by two to produce the four-phase instruction cycle clock.

XTAL (Crystal) — output. This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL should not be connected. It may be disabled through software control using the XTLD bit in the PLL control register.

PCAP (PLL Filter Capacitor) — input. This input is used to connect a high quality external capacitor needed for the PLL filter. The capacitor should be as close as possible to the chip with heavy, short traces connecting one terminal of the capacitor to PCAP and the other terminal to V_{CCP}.

PINIT (PLL Initialization) — input. During the assertion of hardware reset, the value at the PINIT input pin is written into the PEN bit of the PLL control register. When high, the PEN bit enables the PLL by causing it to derive the internal clocks from the PLL voltage controlled oscillator output. When the bit is clear, the PLL is disabled and the chip's internal clocks are derived from the clock connected to the EXTAL pin. After hardware reset is deasserted, the PINIT pin is ignored.

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Electrical Specifications

The preliminary DC / AC electrical specifications are generated from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The DSP56005 is fabricated in high density CMOS with TTL compatible inputs and outputs.

Table 6 Maximum Ratings (GND = 0Vdc)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
All Input Voltages	V_{IN}	GND - 0.5 to V_{CC} + 0.5	V
Current Drain per Pin Excluding V_{CC} and GND	I	10	mA
Operating Temperature Range	T_J	-40 to +105	°C
Storage Temperature	T_{stg}	-55 to +150	°C

Table 7 Thermal Characteristics of the TQFP Package

Thermal Resistance	Symbol	Value	Rating
Junction to Ambient	Θ_{JA}	49	°C/W
Junction to Case	Θ_{JC}	8	°C/W

NOTE: This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

DC Electrical Characteristics

V_{CC} = 5.0 Vdc ± 10%; T_J = -40° to +105°C

Table 8 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage • Except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, MODC • EXTAL • $\overline{\text{RESET}}$ • MODA, MODB, MODC	 V_{IH} V_{IHC} V_{IHR} V_{IHM}	 2.0 4.0 2.5 3.5	 — — — —	 V_{CC} V_{CC} V_{CC} V_{CC}	 V V V V
Input Low Voltage • Except EXTAL, MODA, MODB, MODC • EXTAL • MODA, MODB, MODC	 V_{IL} V_{ILC} V_{ILM}	 -0.5 -0.5 -0.5	 — — —	 0.8 0.6 2.0	 V V V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{NMI}}$	I_{IN}	-1	—	1	µA
Three-State (Off-State) Input Current (@ 2.4V / 0.4V)	I_{TSI}	-10	—	10	µA
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 3.2 mA; $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD I_{OL} = 6.7 mA)	V_{OL}	—	—	0.4	V
Internal Supply Current 5.5 V, 50 MHz (See Note 3) • in Wait Mode (See Note 1) • in Stop Mode (See Note 1)	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 125 25 2	 TBD TBD TBD	 mA mA µA
PLL Supply Current (See Note 4)		—	TBD	TBD	mA
Clockout Supply Current (See Note 5)		—	TBD	TBD	mA
Input Capacitance (See Note 2)	C_{IN}	—	10	—	pF

NOTES:

1. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float).
2. Periodically sampled and not 100% tested
3. **Power Consumption** in the **Design Considerations** section describes how to calculate the external supply current.
4. Values given are for PLL enabled.
5. Values given are for CKOUT enables.

AC Electrical Characteristics

The timing waveforms in the **AC Electrical Characteristics** are tested with a V_{IL} maximum of 0.5V and a V_{IH} minimum of 2.4V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, MODB, and MODC. These five pins are tested using the input levels set forth in **DC Electrical Characteristics**. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56005 output levels are measured on the production test machine with V_{OL} and V_{OH} reference levels set at 0.8V and 2.0V respectively.

Internal Clocks

For each occurrence of T_H, T_L, T_C or I_{CYC} substitute with the numbers given in Table 9:

Table 9 Internal Clocks

Characteristics	Symbol	Expression
Internal Operation Frequency	f	
Internal Clock High Period	T_H	
- with PLL disabled		ET_H (See Note 1)
- with PLL enabled and MF ≤ 4		(Min) 0.48 x ET_C x DF/MF (Max) 0.52 x ET_C x DF/MF (See Note 2)
- with PLL enabled and MF > 4		(Min) 0.467 x ET_C x DF/MF (Max) 0.533 x ET_C x DF/MF
Internal Clock Low Period	T_L	
- with PLL disabled		ET_L (See Note 1)
- with PLL enabled and MF ≤ 4		(Min) 0.48 x ET_C x DF/MF (Max) 0.52 x ET_C x DF/MF
- with PLL enabled and MF > 4		(Min) 0.467 x ET_C x DF/MF (Max) 0.533 x ET_C x DF/MF
Internal Clock Cycle Time	T_C	ET_C x DF/MF (See Note 1)
Instruction Cycle Time	I_{CYC}	2 x T_C

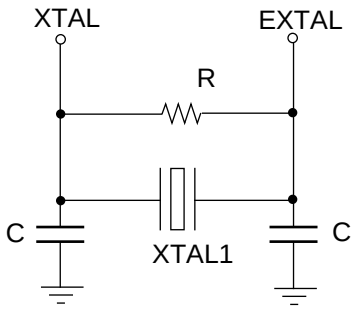
NOTES:

1. The "E" in ET_H, ET_L, and ET_C means external.
2. MF is the PCTL Multiplication Factor bits (MF0 - MF11).
   DF is the PCTL Division Factor bits (DF0 - DF3).

Clock

The DSP56005 system clock may be derived from the on-chip crystal oscillator as shown in Figure 3, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected (see Figure 4) to the board or socket. The rise and fall time of this external clock should be 3 ns maximum.

When using a crystal to provide a clock input, the frequency must be greater than 500 kHz. This restriction does not apply when providing an external clock to the EXTAL pin.



Fundamental Frequency Crystal Oscillator

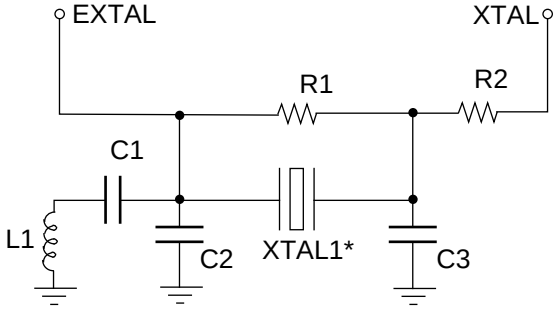
Suggested Component Values

R = 680 kΩ ± 10%

C = 20 pF ± 20%

NOTES:

1. The suggested crystal source is ICM, # 433163 - 4.00 (4 MHz fundamental, 20 pF load)
2. To reduce system cost, a ceramic resonator may be used instead of the crystal. Suggested source: Murata-Erie #CST4.00MGW040 (4 MHz fundamental)



3rd Overtone Crystal Oscillator

Suggested Component Values

R1 = 470 kΩ ± 10%

R2 = 330 Ω ± 10%

C1 = 0.1 µF ± 20%

C2 = 26 pF ± 20%

C3 = 20 pF ± 10%

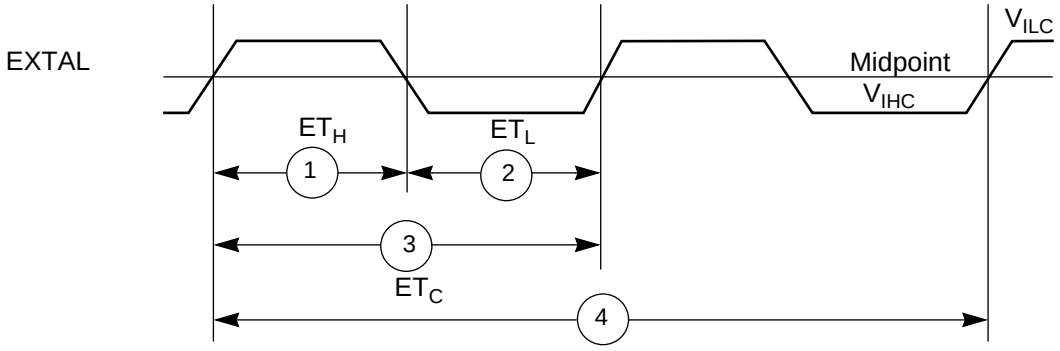
L1 = 2.37 µH ± 10%

XTAL = 50 MHz, AT cut, 20 pF load, 50 Ω max series resistance

NOTES:

1. *3rd overtone crystal.
2. The suggested crystal source is ICM, # 471163 - 50.00 (50 MHz 3rd overtone, 20 pF load).
3. R2 limits crystal current.
4. Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley & Sons, 1983.

Figure 3 Crystal Oscillator Circuits



NOTE: The midpoint is $V_{ILC} + 0.5 (V_{IHC} - V_{ILC})$.

Figure 4 External Clock Timing

Table 10 Clock Operation

Num	Characteristics	Symbol	50 MHz		Unit
			Min	Max	
	Frequency of Operation (EXTAL Pin)	f	0	50	MHz
1	Clock Input High (See Note) • with PLL disabled (46.7% - 53.3% duty cycle) • with PLL enabled (42.5% - 57.5% duty cycle)	ET_H	9.34 8.5	∞ 235500	ns ns
2	Clock Input Low (See Note) • with PLL disabled (46.7% - 53.3% duty cycle) • with PLL enabled (42.5% - 57.5% duty cycle)	ET_L	9.34 8.5	∞ 235500	ns ns
3	Clock Cycle Time • with PLL disabled • with PLL enabled	ET_C	20 20	∞ 409600	ns ns
4	Instruction Cycle Time = $I_{CYC} = 2 \times T_C$ (See Note) • with PLL disabled • with PLL enabled	I_{CYC}	40 40	∞ 819200	ns ns

NOTE: External Clock Input High and External Clock Input Low are measured at 50% of the input transition.

Phase-Locked Loop (PLL)

Table 11 Phase-Locked Loop Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled	MF x E_f (See Notes 1,2)	10	f (See Note 3)	MHz
PLL external capacitor (PCAP pin to V_{CCP})	MF × Cpcap (See Note 4) @ MF ≤ 4 @ MF > 4	 MF × 340 MF × 380	 MF × 480 MF × 970	pF

NOTES:

1. The “E” in E_f, ET_H, ET_L, and ET_C means external.
2. MF is the PCTL Multiplication Factor bits (MF0 - MF11).
   DF is the PCTL Division Factor bits (DF0 - DF3).
3. The maximum VCO frequency is limited to the internal operation frequency.
4. Cpcap is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}) for MF=1. The recommended value for Cpcap is 400 pF for MF ≤ 4 and 540 pF for MF > 4.

Reset, Stop, Mode Select, and Interrupt Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Loads

WS = Number of wait states (1 WS = T_C) programmed into external bus access using BCR (WS = 0 - 15)

Table 12 Reset, Stop, Mode Select, and Interrupt Timing

Num	Characteristics	50 MHz		Unit
		Min	Max	
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested)	—	26	ns
10	Minimum Stabilization Duration • Internal Oscillator PLL Disabled (See Note 1) • External Clock PLL Disabled (See Note 2) • External Clock PLL Enabled (See Note 2)	 $75000 \times T_C$ $25 \times T_C$ $2500 \times T_C$	 — — —	 ns ns ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Deassertion)	$8 \times T_C$	$9 \times T_C + 20$	ns
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to CKOUT Falling Edge	8.5	T_C	ns
13	Synchronous Reset Delay Time from the CKOUT Falling Edge to the First External Address Output	$8 \times T_C$	$8 \times T_C + 6$	ns
14	Mode Select Setup Time	21	—	ns
15	Mode Select Hold Time	0	—	ns
16	Minimum Edge-Triggered Interrupt Request Assertion Width	13	—	ns
16a	Minimum Edge-Triggered Interrupt Request Deassertion Width	13	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to External Memory Access Address Out Valid • Caused by First Interrupt Instruction Fetch • Caused by First Interrupt Instruction Execution	 $5 \times T_C + T_H$ $9 \times T_C + T_H$	 — —	 ns ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{NMI}}$ Assertion to General Purpose Transfer Output Valid caused by First Interrupt Instruction Execution	$11 \times T_C + T_H$	—	ns
19	Delay from Address Output Valid caused by First Interrupt Instruction Execute to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 3)	—	$2\ T_C + T_L + (T_C \times WS) - 23$	ns
20	Delay from $\overline{\text{RD}}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts (See Note 3)	—	$2T_C + (T_C \times WS) - 21$	ns
21	Delay from $\overline{\text{WR}}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts • WS = 0 • WS > 0 (See Note 3)	 — —	 $2 \times T_C - 21$ $T_C + T_L + (T_C \times WS) - 21$	 ns ns

Table 12 Reset, Stop, Mode Select, and Interrupt Timing (continued)

Num	Characteristics	50 MHz		Unit
		Min	Max	
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts - If Second Interrupt Instruction is: • Single Cycle • Two Cycles (See Note 3)	 — —	 T_L - 31 $(2 \times T_C) + T_L$ - 31	 ns ns
23	Synchronous Interrupt Setup Time from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{NMI}$ Assertion to the CKOUT transition #2	10	T_C	ns
24	Synchronous Interrupt Delay Time from the CKOUT transition #2 to the First External Address Output Valid caused by the First Instruction Fetch after coming out of Wait State	$13 \times T_C + T_H$	$13 \times T_C + T_H + 6$	ns
25	Duration for $\overline{IRQA}$ Assertion to Recover from Stop State	12	—	ns
26	Delay from $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17 = 1 (See Note 1)	 $65548 \times T_C$ $20 \times T_C$ $13 \times T_C$	 — — —	 ns ns ns
27	Duration of Level Sensitive $\overline{IRQA}$ Assertion to ensure interrupt service (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17 = 1 (See Note 1)	 $65534 \times T_C + T_L$ $6 \times T_C + T_L$ 12	 — — —	 ns ns ns
28	Delay from Level Sensitive $\overline{IRQA}$ Assertion to Fetch of First Interrupt Instruction (when exiting 'Stop') • Internal Crystal Oscillator Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 $65548 \times T_C$ $20 \times T_C$ $13 \times T_C$	 — — —	 ns ns ns

NOTES:

1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

   During this stabilization period, T_C, T_H, and T_L will not be constant. Since this stabilization period varies, a delay of $75{,}000 \times T_C$ is typically allowed to assure that the oscillator is stable before executing programs.

2. Circuit stabilization delay is required during reset when using an external clock in two cases:
   - after power-on reset, and
   - when recovering from Stop mode.

3. When using fast interrupts and $\overline{IRQA}$ and $\overline{IRQB}$ are defined as level-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deassertive edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using level-sensitive mode.

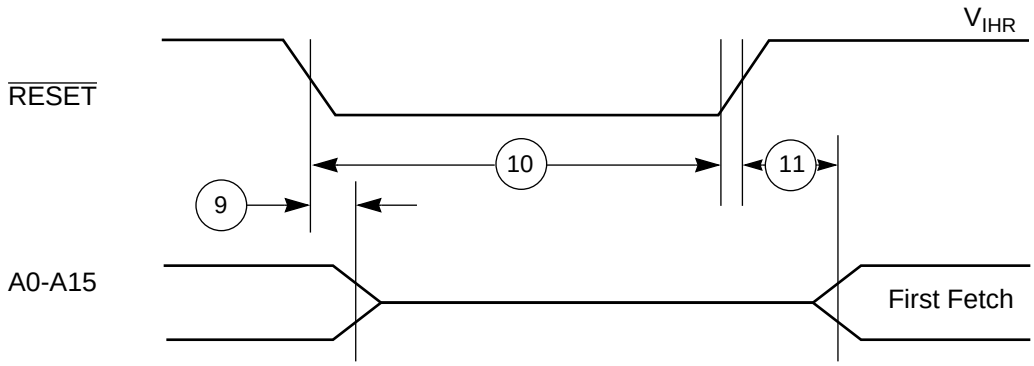


Figure 5 Reset Timing

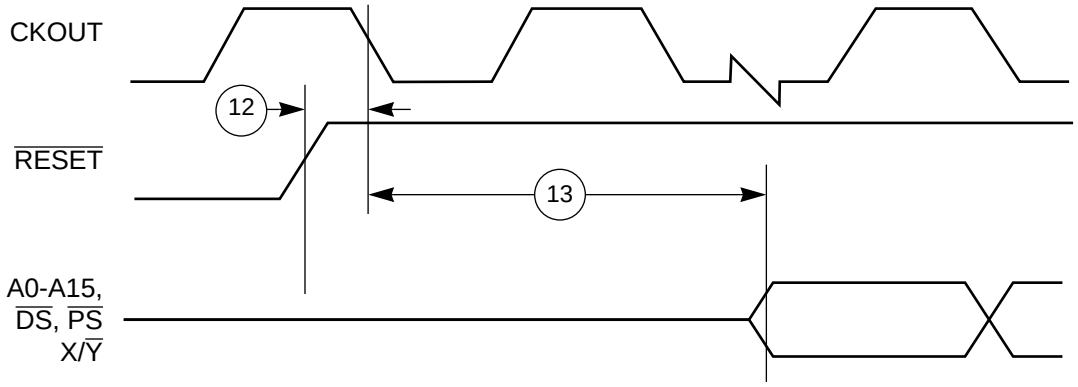


Figure 6 Synchronous Reset Timing

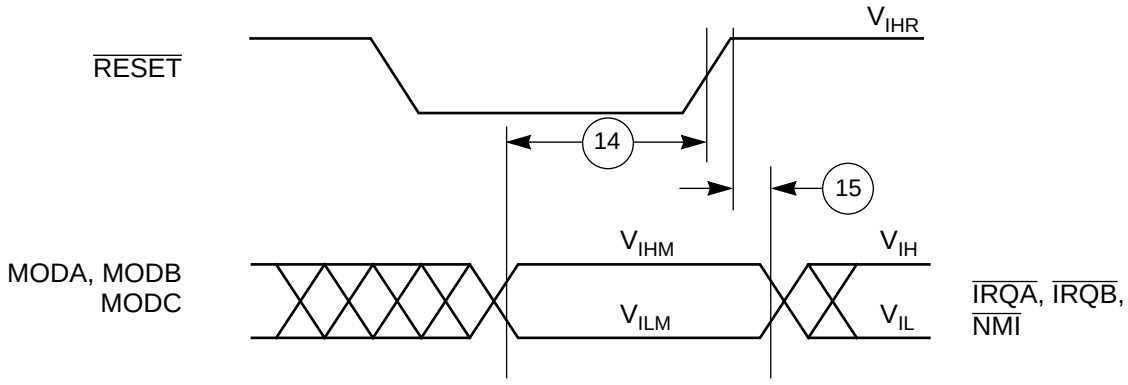


Figure 7 Operating Mode Select Timing

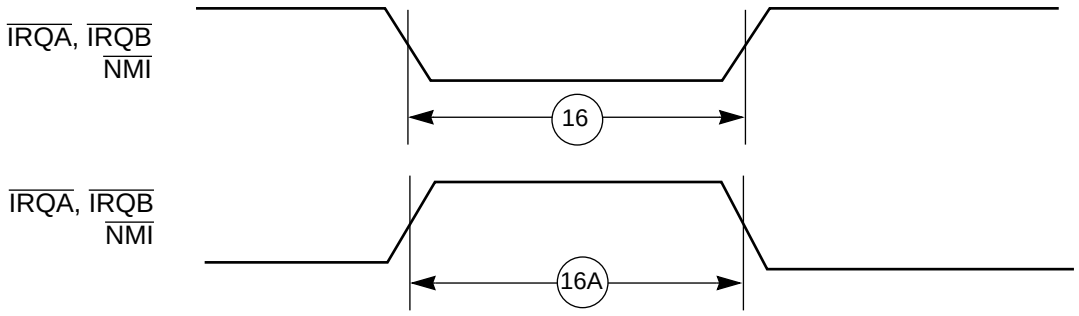
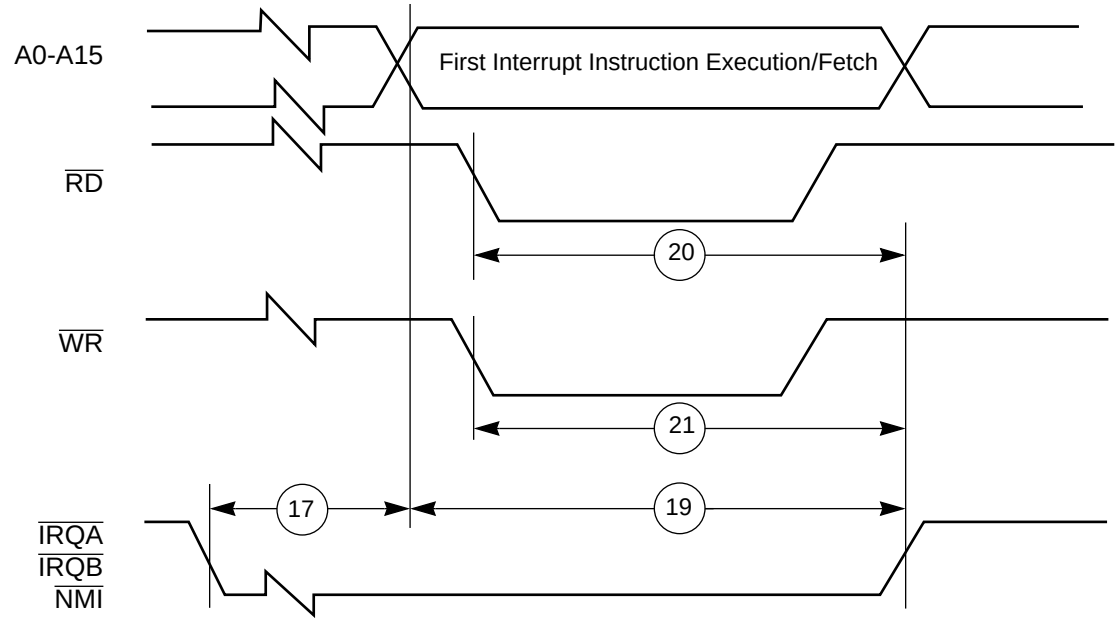
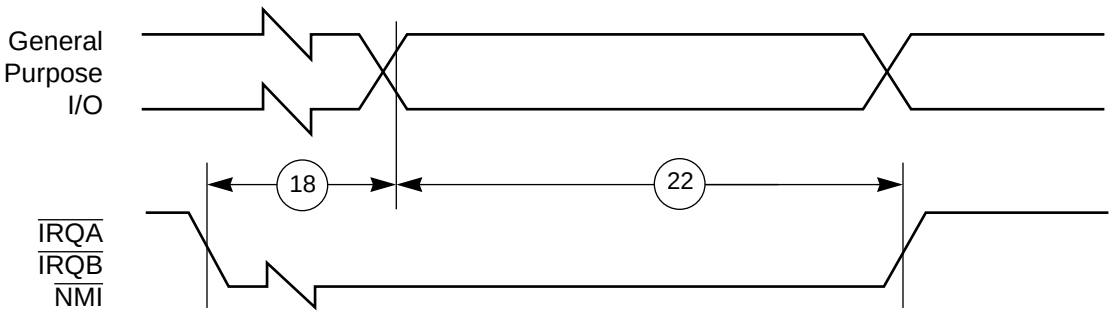


Figure 8 External Interrupt Timing (Negative Edge-Triggered)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 9 External Level-Sensitive Fast Interrupt Timing

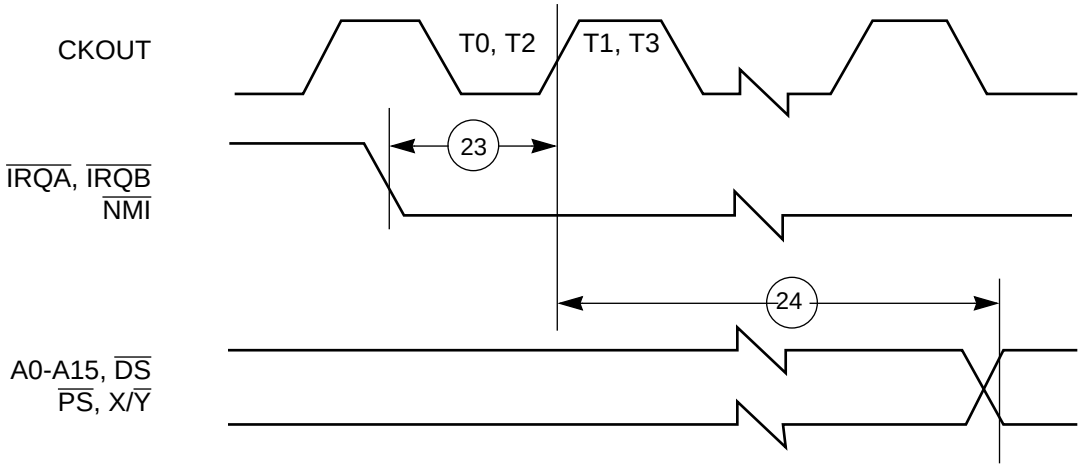


Figure 10 Synchronous Interrupt from Wait State Timing

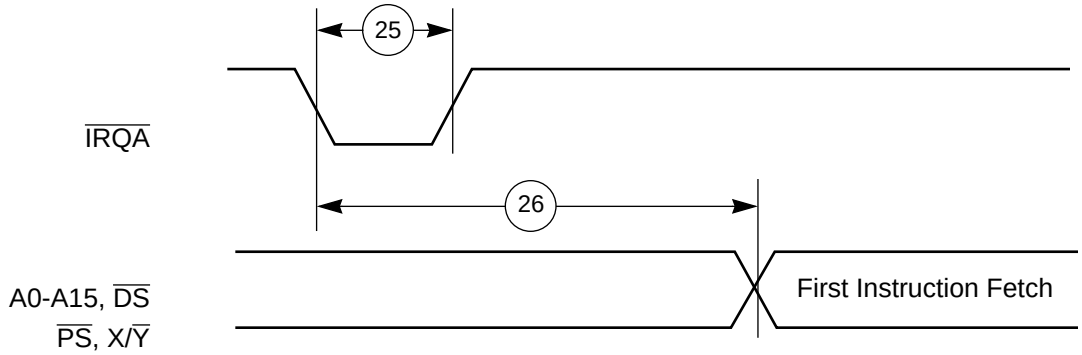


Figure 11 Recovery from Stop State Using IRQA

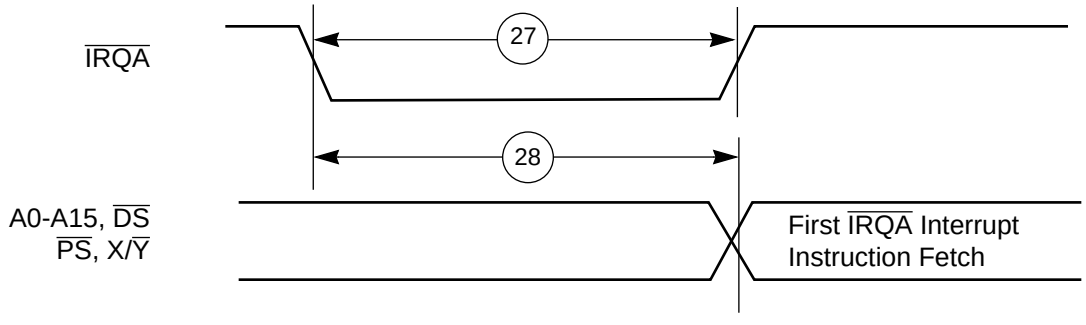


Figure 12 Recovery from Stop State Using IRQA Interrupt Service

Host I/O Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Load

Active low lines should be “pulled up” in a manner consistent with the AC and DC specifications.

Table 13 Host I/O Timing

Num	Characteristics	50 MHz		Unit
		Min	Max	
31	$\overline{HEN}/\overline{HACK}$ Assertion Width (See Note 1) • CVR, ICR, ISR, RXL Read • IVR, RXH/M Read • Write	 $T_C + 31$ 26 13	 — — —	ns
32	$\overline{HEN}/\overline{HACK}$ Deassertion Width (See Note 1) • Between Two TXL Writes (See Note 2) • Between Two CVR, ICR, ISR, RXL Reads (See Note 3)	13 $2 \times T_C + 31$ $2 \times T_C + 31$	— — —	ns ns ns
33	Host Data Input Setup Time Before $\overline{HEN}/\overline{HACK}$ Deassertion	4	—	ns
34	Host Data Input Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	3	—	ns
35	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	ns
36	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Valid	—	26	ns
37	$\overline{HEN}/\overline{HACK}$ Deassertion to Output Data High Impedance (See Note 5)	—	18	ns
38	Output Data Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion (See Note 6)	2.5	—	ns
39	HR/$\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
40	HR/$\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
41	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	ns
42	HR/$\overline{W}$ High Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	3	—	ns
43	HA0-HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	ns
44	HA0-HA2 Hold Time After $\overline{HEN}$ Deassertion	3	—	ns
45	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion (See Note 4)	3	45	ns

Table 13 Host I/O Timing (Continued)

Num	Characteristics	50 MHz		Unit
		Min	Max	
46	DMA $\overline{\text{HACK}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion (See Notes 4, 5) • for DMA RXL Read • for DMA TXL Write • all other cases	 $T_L + T_C + T_H$ $T_L + T_C$ 0	 — — —	 ns ns ns
47	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for RXL Read (See Notes 4, 5)	$T_L + T_C + T_H$	—	ns
48	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for TXL Write (See Notes 4, 5)	$T_L + T_C$	—	ns
49	Delay from $\overline{\text{HEN}}$ Assertion to $\overline{\text{HREQ}}$ Deassertion for RXL Read, TXL Write (See Notes 4, 5)	3	58	ns

NOTES:

1. See **Host Port Use Considerations** in the Design Considerations section of this data sheet.
2. This timing must be adhered to only if two consecutive Writes to the TXL are executed without polling TXDE or $\overline{\text{HREQ}}$.
3. This timing must be adhered to only if two consecutive reads from one of these registers are executed without polling the corresponding status bits or $\overline{\text{HREQ}}$.
4. $\overline{\text{HREQ}}$ is pulled up by a 1kΩ resistor.
5. Specifications are periodically sampled and not 100% tested.
6. May decrease to 0 ns for future versions.

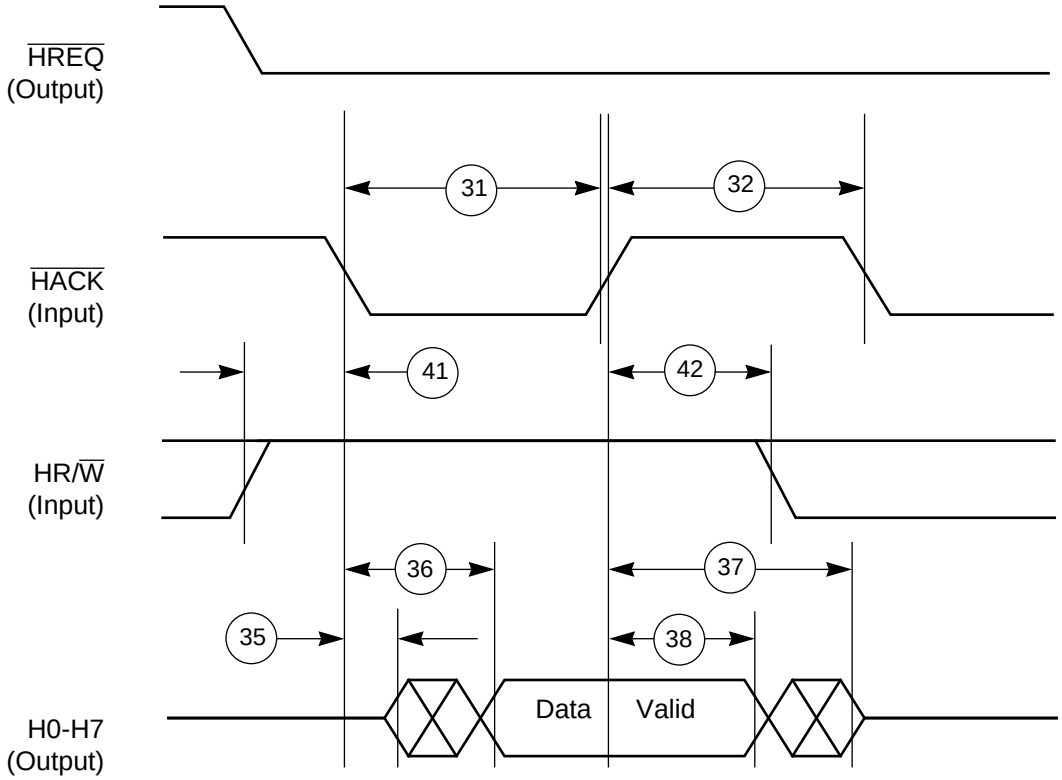


Figure 13 Host Interrupt Vector Register (IVR) Read

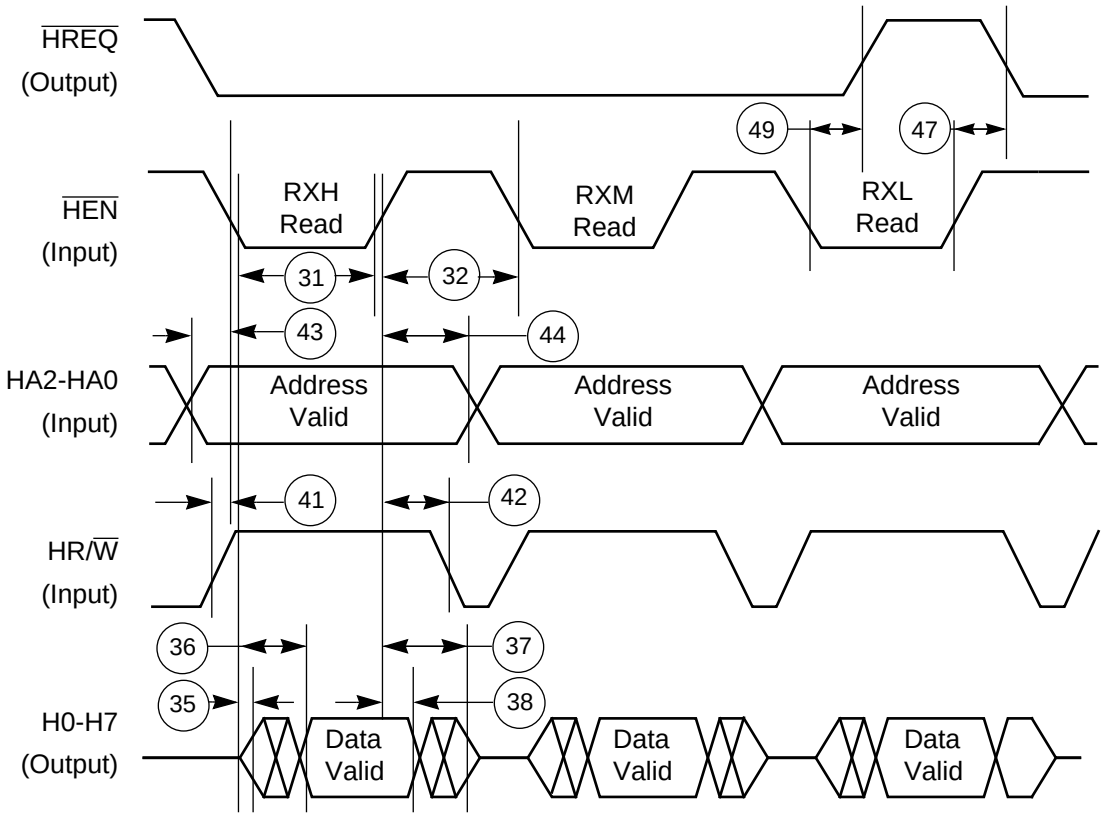


Figure 14 Host Read Cycle (Non-DMA Mode)

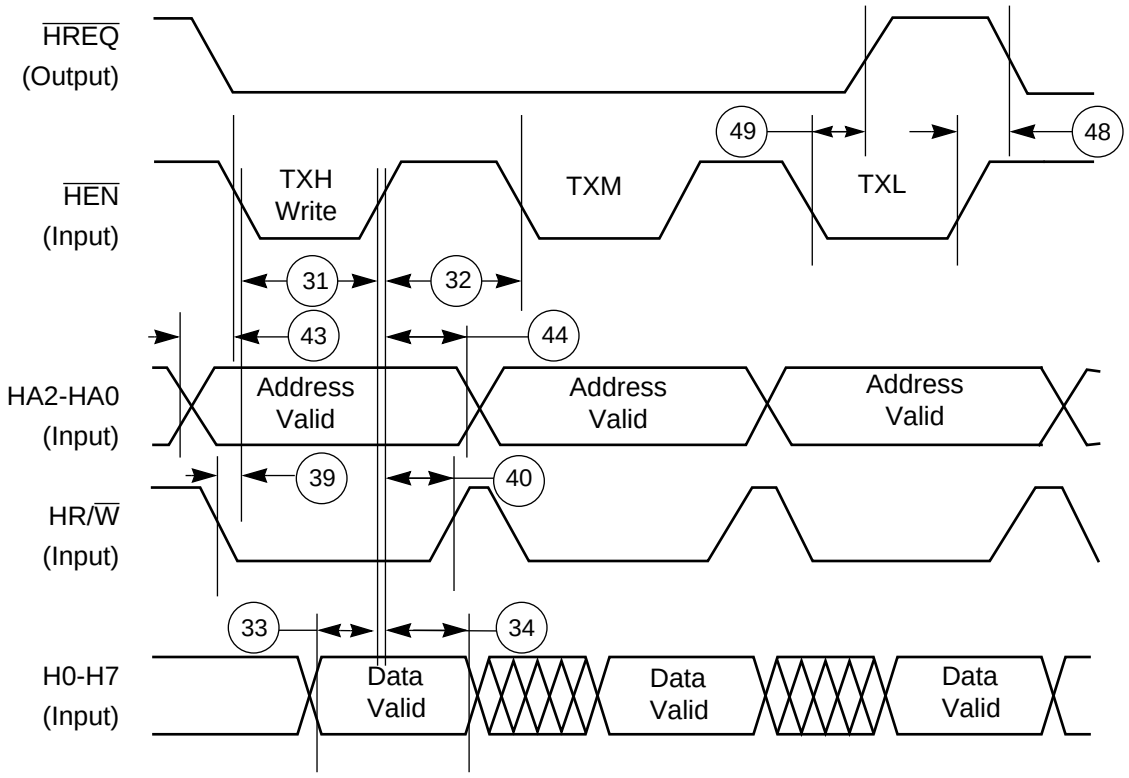


Figure 15 Host Write Cycle (Non-DMA Mode)

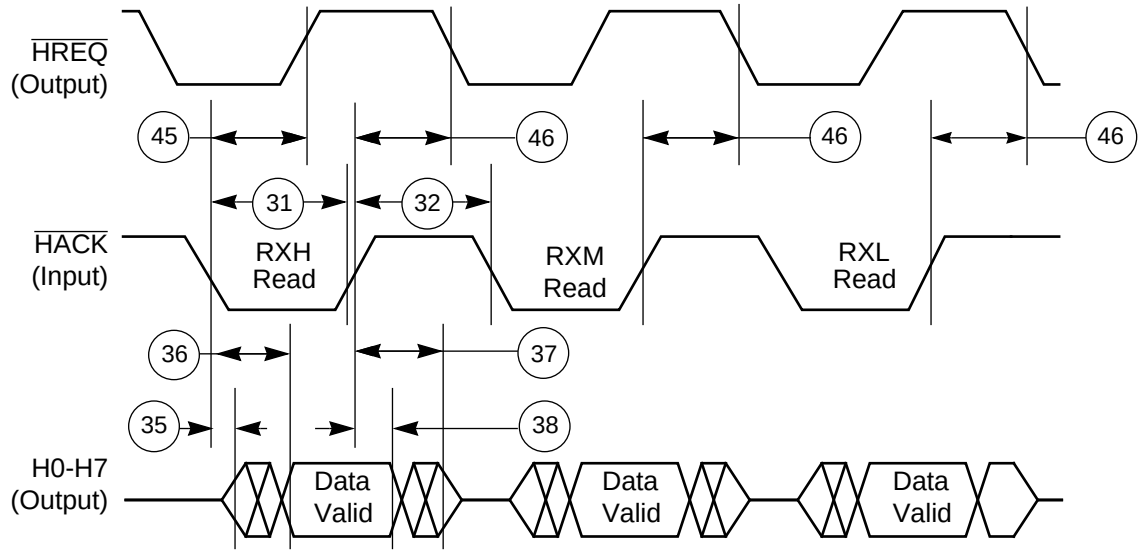


Figure 16 Host DMA Read Cycle

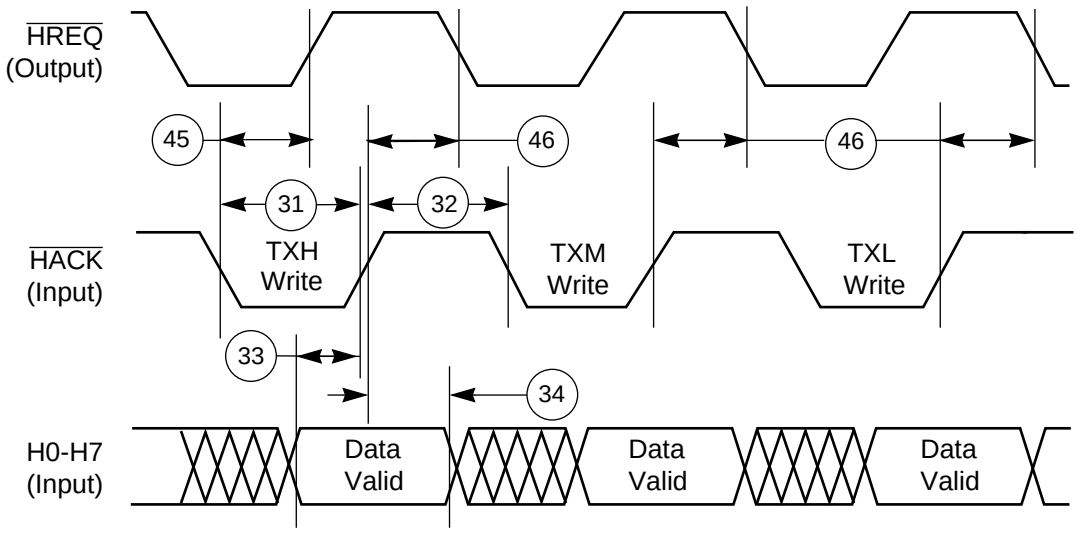


Figure 17 Host DMA Write Cycle

Serial Communication Interface (SCI) Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Load,

tSCC = Synchronous Clock Cycle Time (for internal clock, tSCC is determined by the SCI clock control register and T_C). The minimum tSCC value is $8 \times T_C$.

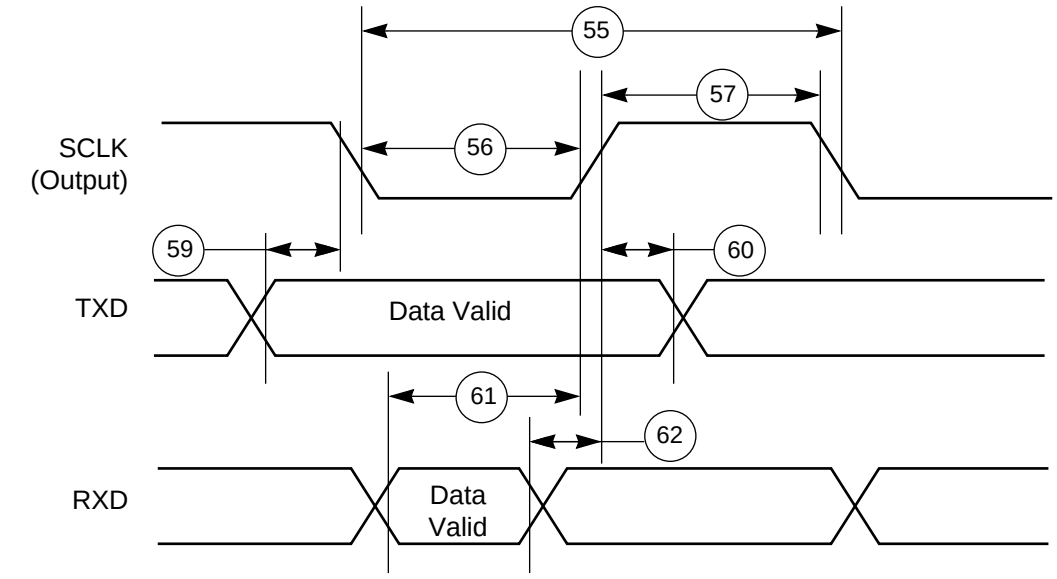
Table 14 SCI Synchronous Mode Timing

Num	Characteristics	50 MHz		Unit
		Min	Max	
55	Synchronous Clock Cycle — tSCC	$8 \times T_C$	—	ns
56	Clock Low Period	tSCC/2 - 10.5	—	ns
57	Clock High Period	tSCC/2 - 10.5	—	ns
58	< intentionally blank >	—	—	—
59	Output Data Setup to Clock Falling Edge (Internal Clock)	tSCC/4 + T_L - 26	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	tSCC/4 -T_L - 8	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	tSCC/4 + T_L + 23	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	tSCC/4 + T_L - 5.5	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	32.5	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	T_C + 3	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	16	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	21	—	ns

Table 15 SCI Asynchronous Mode Timing — 1X Clock

Num	Characteristics	50 MHz		Unit
		Min	Max	
67	Asynchronous Clock Cycle - tACC	$64 \times T_C$	—	ns
68	Clock Low Period	tACC/2 -11	—	ns
69	Clock High Period	tACC/2 -11	—	ns
70	< intentionally blank >	—	—	—
71	Output Data Setup to Clock Rising Edge (Internal Clock)	tACC/2 -51	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	tACC/2 -51	—	ns

Internal Clock



External Clock

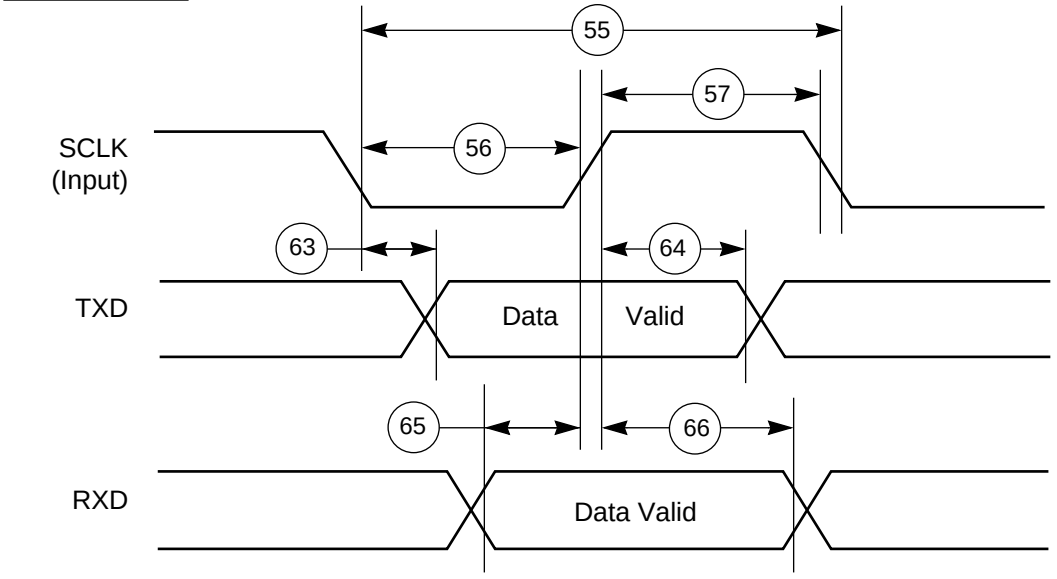
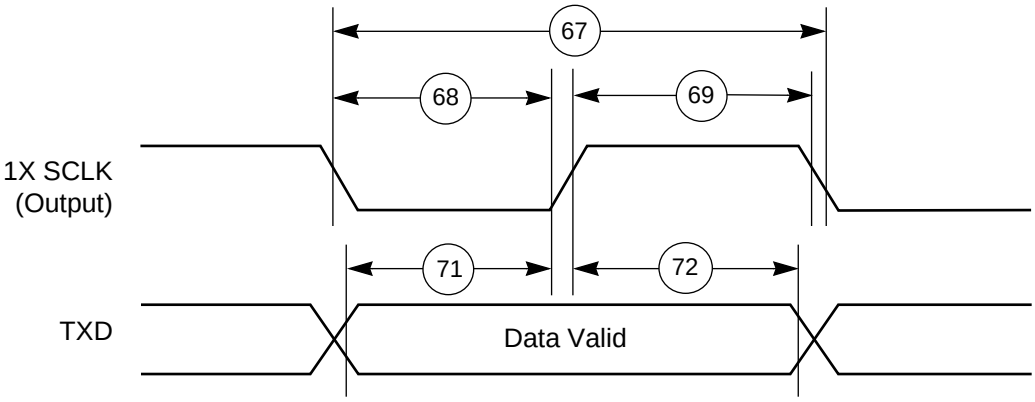


Figure 18 SCI Synchronous Mode Timing



NOTE: In the wire-OR mode, TXD can be pulled up by 1 KΩ

Figure 19 SCI Asynchronous Mode Timing

Synchronous Serial Interface (SSI) Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C_L = 50 pF + 2 TTL Load,

tSSICC = SSI clock cycle time
TXC (SCK Pin) = Transmit Clock
RXC (SC0 or SCK Pin) = Receive Clock
FST (SC2 Pin) = Transmit Frame Sync
FSR (SC1 or SC2 Pin) = Receive Frame Sync
ick = Internal Clock
xck = External Clock
gck = Gated Clock
ick a = Internal Clock, Asynchronous Mode (Asynchronous implies that TXC and RXC are two different clocks)
ick s = Internal Clock, Synchronous Mode (Synchronous implies that TXC and RXC are the same clock)
bl = bit length
wl = word length

Table 16 SSI Timing

Num	Characteristics	50 MHz		Case	Unit
		Min	Max		
80	Clock Cycle-tSSICC (See Note 1)	$4 \times T_C$ $3 \times T_C$	— —	i ck x ck	ns
81	Clock High Period	$t_{SSICC}/2$ - 10.8 $T_C + T_L$	— —	i ck x ck	ns
82	Clock Low Period	$t_{SSICC}/2$ - 10.8 $T_C + T_L$	— —	i ck x ck	ns
83	< intentionally blank >	—	—	—	—
84	SRD Rising Edge to FSR Out (bl) High	— —	40.8 25.8	x ck i ck a	ns
85	SRD Rising Edge to FSR Out (bl) Low	— —	35.8 25.8	x ck i ck a	ns
86	SRD Rising Edge to FSR Out (wl) High	— —	35.8 20.8	x ck i ck a	ns
87	RXC Rising Edge to FSR Out (wl) Low	— —	35.8 20.8	x ck i ck a	ns

Table 16 SSI Timing (Continued)

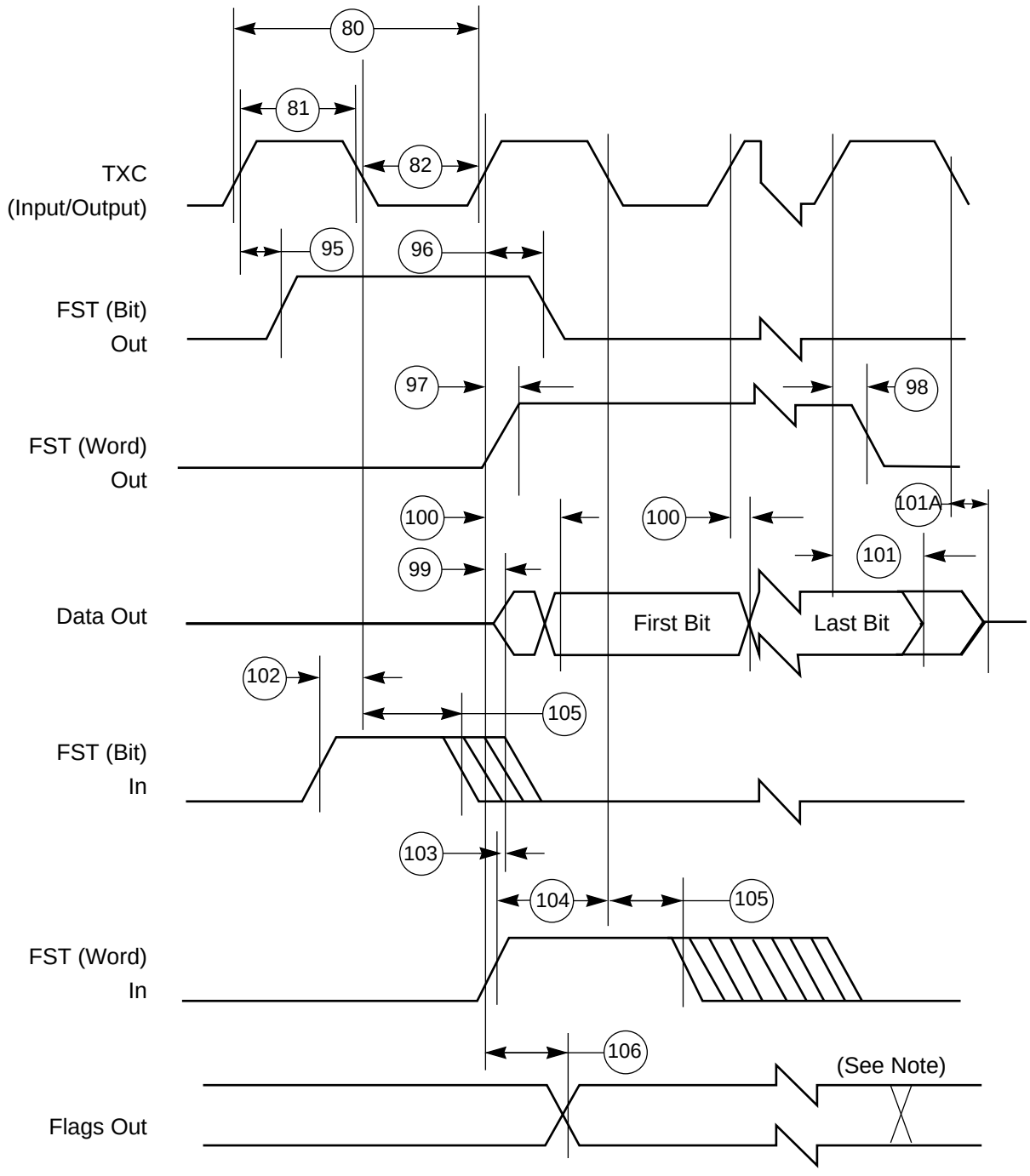
Num	Characteristics	50 MHz		Case	Unit
		Min	Max		
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge	3.3 15.8 13	— — —	x ck i ck a i ck s	ns
89	Data In Hold Time After RXC Falling Edge	18 3.3	— —	x ck i ck	ns
90	FSR Input (bl) High Before RXC Falling Edge	0.8 17.4	— —	x ck i ck a	ns
91	FSR Input (wl) High Before RXC Falling Edge	3.3 18.3	— —	x ck i ck a	ns
92	FSR Input Hold Time After RXC Falling Edge	18.3 3.3	— —	x ck i ck	ns
93	Flags Input Setup Before RXC Falling Edge	0.8 16.7	— —	x ck i ck s	ns
94	Flags Input Hold Time After RXC Falling Edge	18.3 3.3	— —	x ck i ck s	ns
95	TXC Rising Edge to FST Out (bl) High	— —	31.6 15.8	x ck i ck	ns
96	TXC Rising Edge to FST Out (bl) Low	— —	33.3 18.3	x ck i ck	ns
97	TXC Rising Edge to FST Out (wl) High	— —	30.8 18.3	x ck i ck	ns
98	TXC Rising Edge to FST Out (wl) Low	— —	33.3 18.3	x ck i ck	ns
99	TXC Rising Edge to Data Out Enable from High Impedance	— 	$33.3 + T_H$ 20.8	x ck i ck	ns
100	TXC Rising Edge to Data Out Valid	— 	$33.3 + T_H$ 22.4	x ck i ck	ns
101	TXC Rising Edge to Data Out High Impedance (See Note 2)	— —	35.8 20.8	x ck i ck	ns
101A	TXC Falling Edge to Data Out High Impedance (See Note 2)	—	$T_C + T_H$	g ck	ns
102	FST Input (bl) Setup Time Before TXC Falling Edge	0.8 18.3	 —	x ck i ck	ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	30.8		ns

Table 16 SSI Timing (Continued)

Num	Characteristics	50 MHz		Case	Unit
		Min	Max		
104	FST Input (wl) Setup Time Before TXC Falling Edge	0.8 20.0	— —	x ck i ck	ns
105	FST Input Hold Time After TXC Falling Edge	18.3 3.3	— —	x ck i ck	ns
106	Flag Output Valid After TXC Rising Edge	— —	32.5 20.8	x ck i ck	ns

NOTES:

1. For Internal Clock, External Clock Cycle is defined by I_{CYC} and SSI control register.
2. Periodically sampled, and not 100% tested.



NOTE: In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

Figure 20 SSI Transmitter Timing

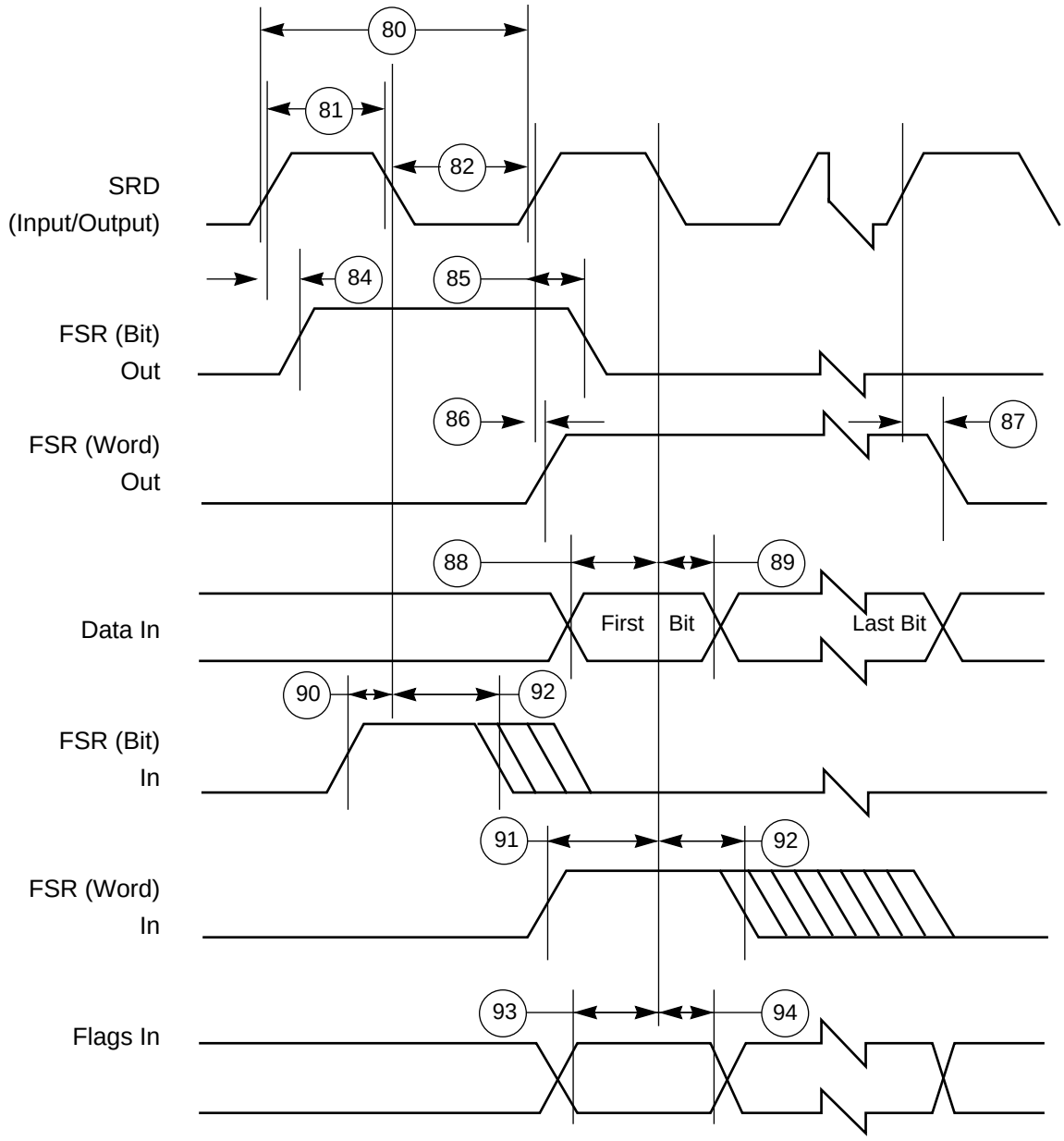


Figure 21 SSI Receiver Timing

External Bus Asynchronous Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, CL = 50 pF + 2 TTL Load

WS = Number of Wait States, Determined by BCR Register (WS = 0 to 15)

Capacitance Derating

The DSP56005 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$, $\overline{EXTP}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be “pulled up” in a manner consistent with the AC and DC specifications.

Table 17 External Bus Asynchronous Timing

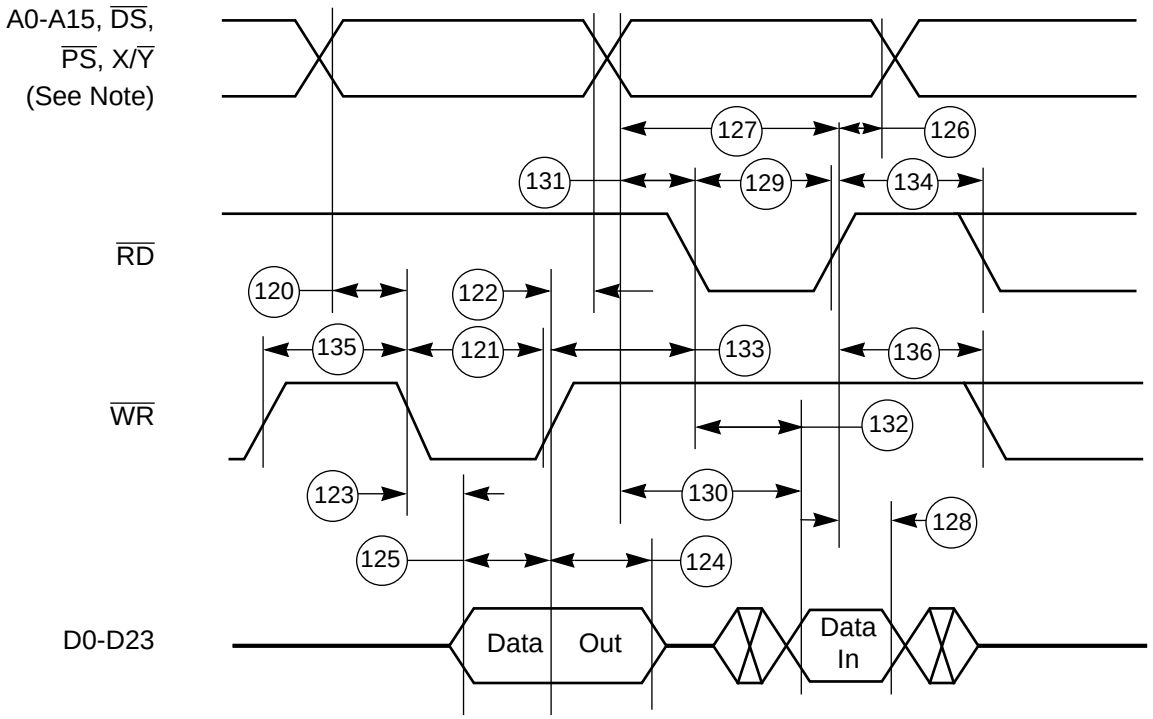
Num	Characteristics	50 MHz		Unit
		Min	Max	
120	Address Valid to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 T_L-6 T_C-6	 — —	ns
121	$\overline{WR}$ Assertion Width • WS = 0 • WS > 0	 T_C WS x T_C+T_L	 — —	ns
122	$\overline{WR}$ Deassertion to Address Not Valid	T_H-6	—	ns
123	$\overline{WR}$ Assertion to Data Out Active • WS = 0 From High Impedance • WS > 0	 T_H-4 0	 — —	ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (the maximum specification is periodically sampled, and not 100% tested)	T_H-7 (See Note 1)	T_H-2.5 (See Note 2)	ns
125	Data Out Setup Time to $\overline{WR}$ Deassertion • WS = 0 • WS > 0	 T_L-0.8 WS x T_C+T_L-0.8		ns
126	$\overline{RD}$ Deassertion to Address Not Valid	T_H	—	ns
127	Address Valid to $\overline{RD}$ Deassertion • WS = 0 • WS > 0	 T_C+T_L-6 ((WS+1)x T_C)+T_L-6	—	ns
128	Input Data Hold Time to $\overline{RD}$ Deassertion	0	—	ns

Table 17 External Bus Asynchronous Timing (Continued)

Num	Characteristics	50 MHz		Unit
		Min	Max	
130	Address Valid to Input Data Valid • WS = 0 • WS > 0	 — —	 $T_C+T_L-9.5$ ((WS+1) x T_C)+T_L-9.5	ns
131	Address Valid to $\overline{RD}$ Assertion	TL-6	—	ns
132	$\overline{RD}$ Assertion to Input Data Valid • WS = 0 • WS > 0	 — —	 T_C-7.5 ((WS+1) x T_C)-7.5	ns
133	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion	T_C-7	—	ns
134	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion	T_C-4	—	ns
135	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 T_C-4 T_C+T_H-4	 — —	ns ns ns
136	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion • WS = 0 • WS > 0	 T_C-4 T_C+T_H-4	 —	ns ns ns

NOTES:

1. $\overline{WR}$ Deassertion to the end of valid data.
2. $\overline{WR}$ Deassertion to data high impedance.



NOTE: During Read-Modify-Write instructions, the address lines do not change state.

Figure 22 External Bus Asynchronous Timing

External Bus Synchronous Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Load

Capacitance Derating

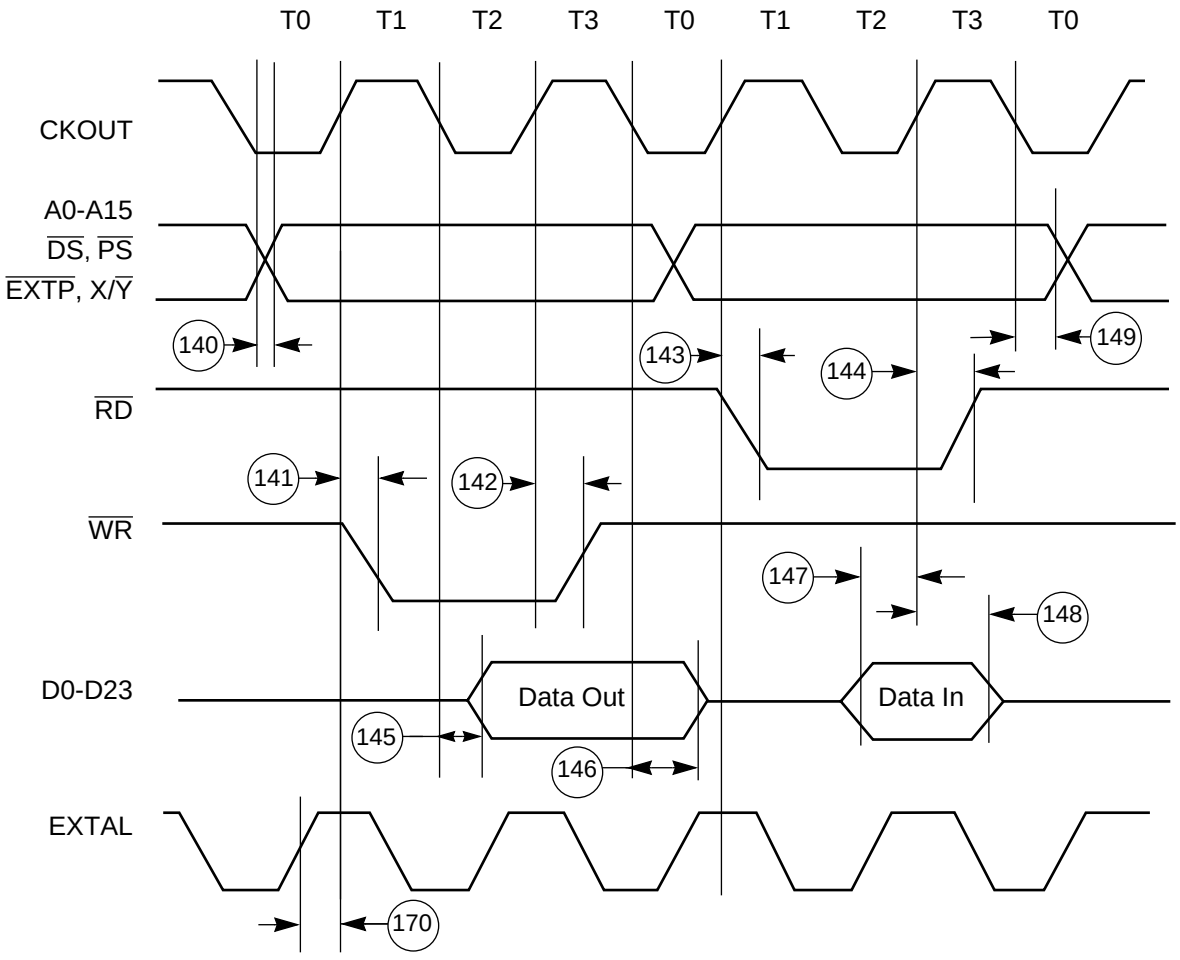
The DSP56005 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$, $\overline{EXTP}$) derates linearly at 1 ns per 12 pF of additional capacitance from 50 pF to 250 pF of loading. Port B and C pins derate linearly at 1 ns per 5 pF of additional capacitance from 50 pF to 250 pF of loading. Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications.

Table 18 External Bus Synchronous Timing

Num	Characteristics	50 MHz		Unit
		Min	Max	
140	CKOUT Falling Edge to Address Valid	—	6.2	ns
141	CKOUT Rising Edge to $\overline{WR}$ Assertion • WS=0 (See Note 1) • WS>0	 — —	 4.4 T_H+4.4	 ns ns
142	CKOUT Rising Edge to $\overline{WR}$ Deassertion	1.3	9.1	ns
143	CKOUT Rising Edge to $\overline{RD}$ Assertion	—	3.9	ns
144	CKOUT Rising Edge to $\overline{RD}$ Deassertion	0	3.4	ns
145	CKOUT Falling Edge to Data-Out Valid	—	5.4	ns
146	CKOUT Falling Edge to Data-Out Invalid (See Note 3)	0	—	ns ns
147	Data-In Valid To CKOUT Rising Edge (Setup)	3.4	—	ns
148	CKOUT Rising Edge to Data-In Invalid (Hold)	0	—	ns
149	CKOUT Falling Edge to Address Invalid (See Note 3)	0	—	ns
170	EXTAL to CKOUT — PLL Disabled EXTAL to CKOUT — PLL Enabled and MF < 5	3 0.3	9.7 3.7	ns ns

NOTES:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. WS are Wait state values specified in the BCR.
3. CKOUT Falling Edge to data-out invalid (specification T146) and CKOUT Falling Edge to address invalid (specification T149) indicate the time after which data/address are no longer guaranteed to be valid.
4. Timings are given from CKOUT midpoint to VOL or VOH of the corresponding pin(s).



NOTE: During Read-Modify-Write Instructions, the address lines do not change states.

Figure 23 Synchronous Bus Timing

OnCE™ Port Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Loads

Table 19 OnCE Port Timing

Num	Characteristics	50 MHz		Unit
		Min	Max	
230	DSCK Low	40	—	ns
231	DSCK High	40	—	ns
232	DSCK Cycle Time	200	—	ns
233	$\overline{DR}$ Asserted to DSO ($\overline{ACK}$) Asserted	$5T_C$	—	ns
234	DSCK High to DSO Valid	—	42	ns
235	DSCK High to DSO Invalid	3	—	ns
236	DSI Valid to DSCK Low (Setup)	15	—	ns
237	DSCK Low to DSI Invalid (Hold)	3	—	ns
238	Last DSCK Low to OS0-OS1, $\overline{ACK}$ Active	$3T_C + T_L$	—	ns
239	DSO ($\overline{ACK}$) Asserted to First DSCK High	$2T_C$	—	ns
240	DSO ($\overline{ACK}$) Assertion Width	$4T_C + T_H - 3$	$5T_C + 7$	ns
241	DSO ($\overline{ACK}$) Asserted to OS0-OS1 High Impedance (See Note 2)	—	0	ns
242	OS0-OS1 Valid to CKOUT Rising Edge	$T_C - 21$	—	ns
243	CKOUT Rising Edge to OS0-OS1 Invalid	0	—	ns
244	Last DSCK Low of Read Register to First DSCK High of Next Command	$7T_C + 10$	—	ns
245	Last DSCK Low to DSO Invalid (Hold)	3	—	ns
246	$\overline{DR}$ Assertion to CKOUT Rising Edge for Wake Up from Wait State	12	T_C	ns
247	CKOUT Rising Edge to DSO After Wake Up from Wait State	$17T_C$		ns
248	$\overline{DR}$ Assertion Width • to recover from Wait • to recover from Wait and enter DEBUG mode	 15 $13T_C+15$	 $12T_C - 15$ —	ns
249	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) after Asynchronous Recovery from Wait State	$17T_C$	—	ns

Table 19 OnCE Port Timing (Continued)

Num	Characteristics	50 MHz		Unit
		Min	Max	
250A	$\overline{DR}$ Assertion Width to Recover from Stop • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 15 15 15	 $65548T_C + T_L$ $20T_C + T_L$ $13T_C + T_L$	ns
250B	$\overline{DR}$ Assertion Width to Recover from Stop and Enter Debug Mode • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 $65549T_C + T_L$ $21T_C + T_L$ $14T_C + T_L$	 — — —	ns
251	$\overline{DR}$ Assertion to DSO ($\overline{ACK}$) Valid (Enter Debug Mode) after Recovery from Stop State • Stable External Clock, OMR bit 6 = 0 • Stable External Clock, OMR bit 6 = 1 • Stable External Clock, PCTL bit 17= 1 (See Note 1)	 $65553T_C + T_L$ $25T_C + T_L$ $18T_C + T_L$	 — — —	ns

NOTES:

1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   - after power-on reset
   - when recovering from stop mode

   During this stabilization period, T_C, $T_{H,}$ and T_L will not be constant. Since this stabilization period varies, a delay of 75,000 x T_C is typically allowed to assure that the oscillator is stable before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case.
2. The maximum specified is periodically sampled and not 100% tested.

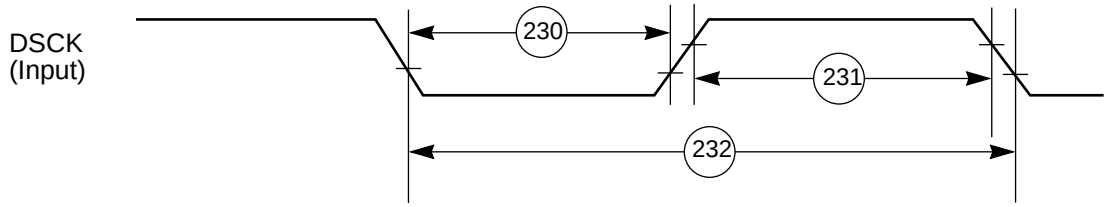


Figure 24 OnCE Serial Clock Timing

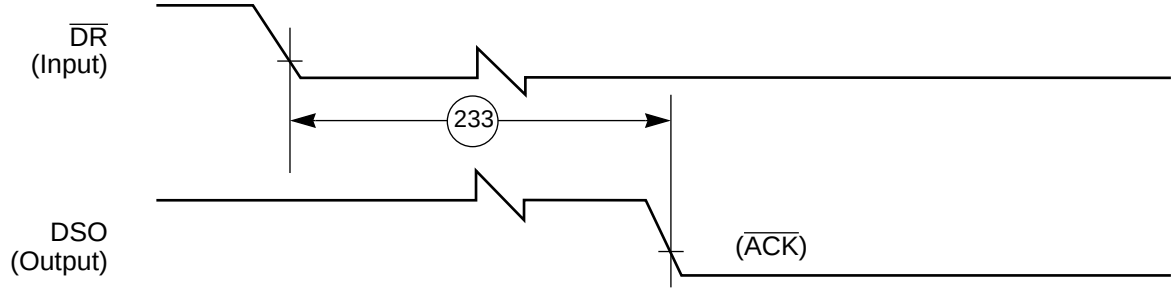
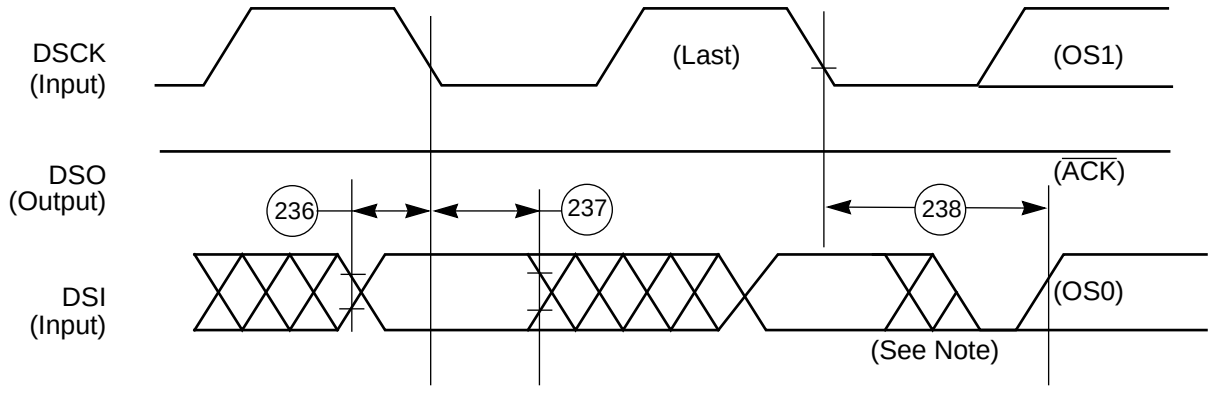
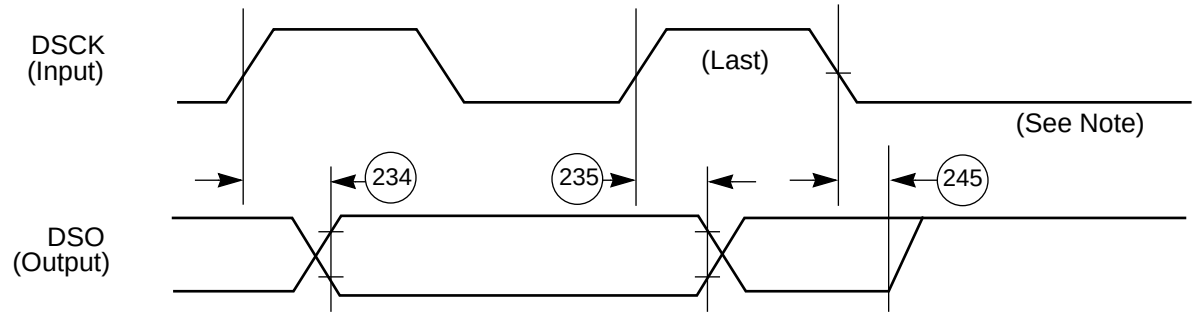


Figure 25 OnCE Acknowledge Timing



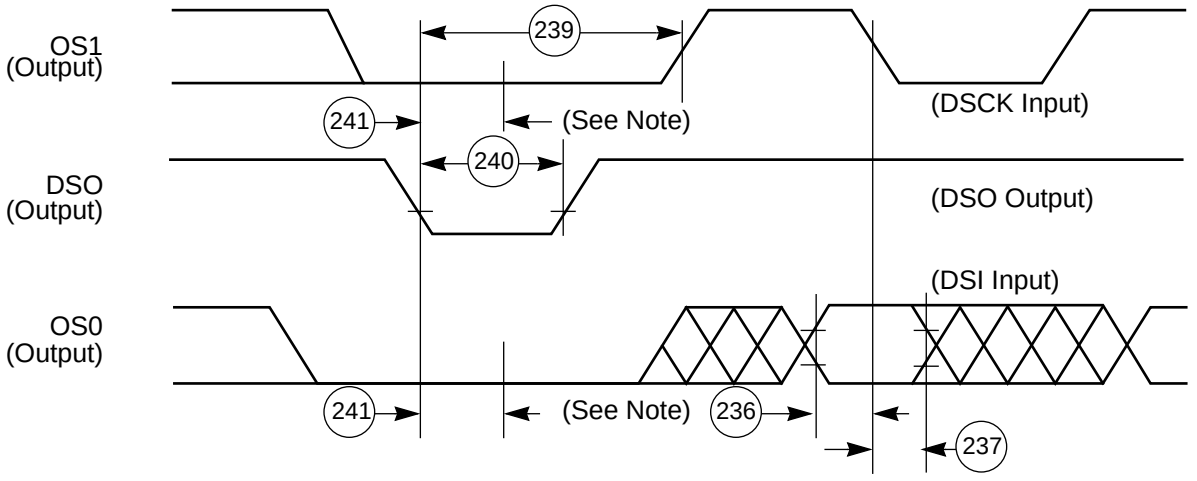
NOTE: High Impedance, external pull-down resistor

Figure 26 OnCE Data I/O To Status Timing



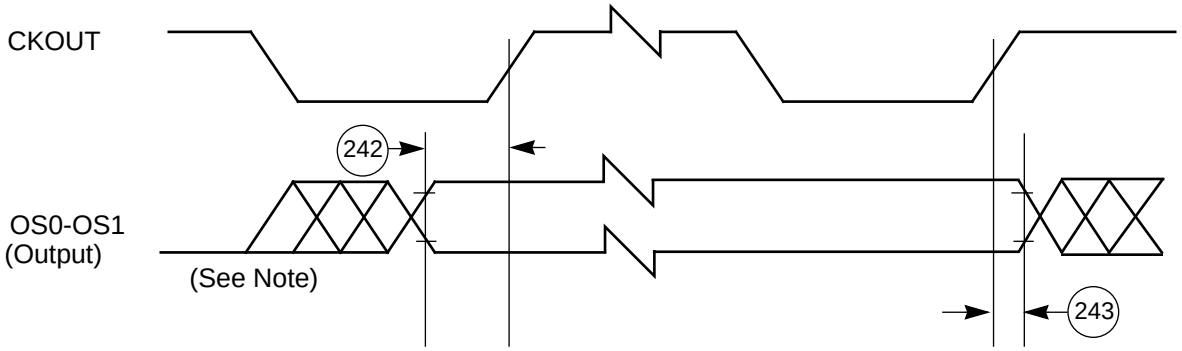
NOTE: High Impedance, external pull-down resistor

Figure 27 OnCE Read Timing



NOTE: High Impedance, external pull-down resistor

Figure 28 OnCE Data I/O To Status Timing



NOTE: High Impedance, external pull-down resistor

Figure 29 OnCE CKOUT To Status Timing

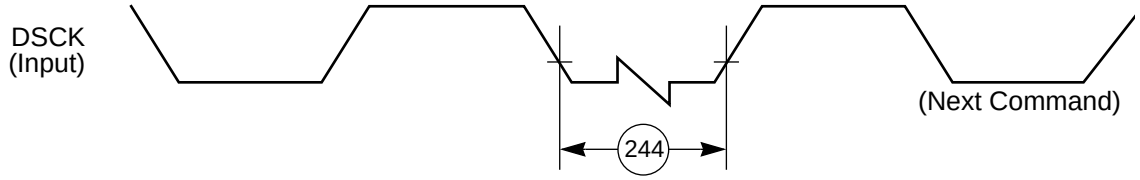


Figure 30 OnCE Read Register to Next Command Timing

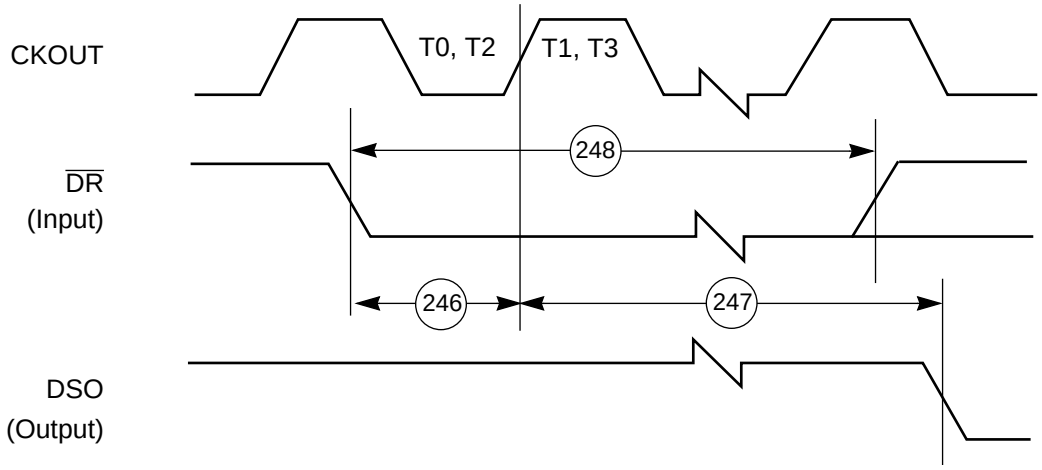


Figure 31 Synchronous Recovery from Wait State

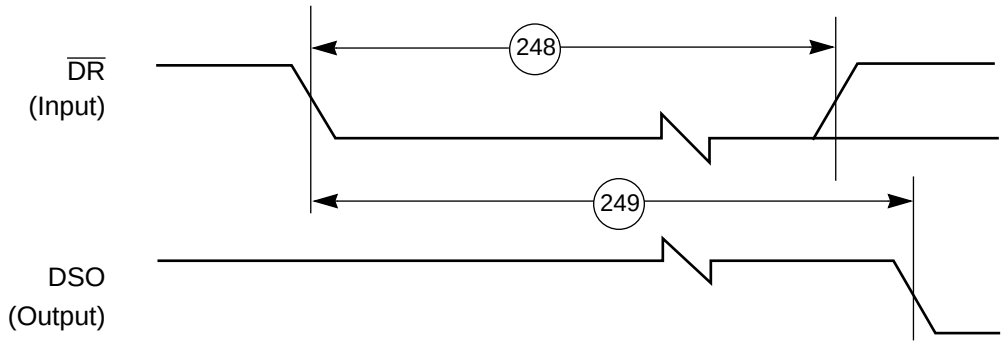


Figure 32 Asynchronous Recovery from Wait State

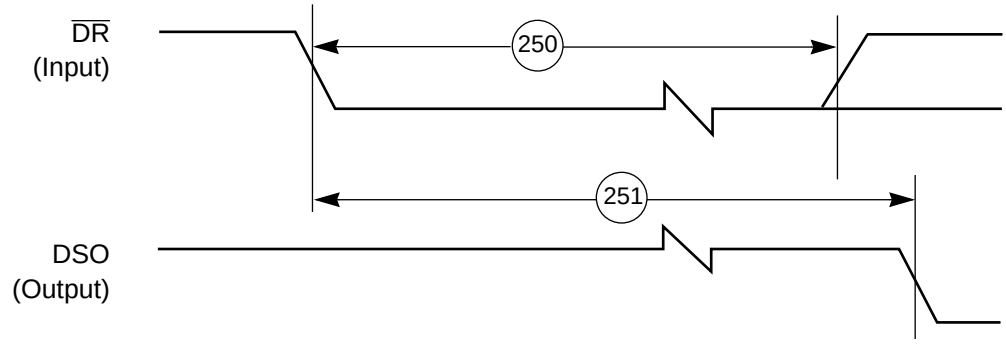


Figure 33 Asynchronous Recovery from Wait State

Timer Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Loads

Table 20 Timer Timing

Num	Characteristics	50 MHz		Unit
		Min	Max	
260	TIO Low	$2T_C$+7	—	ns
261	TIO High	$2T_C$+7	—	ns
262	Synchronous Timer Setup Time from TIO (input) Asssertion to CKOUT Rising Edge	10	T_C	ns
263	Synchronous Timer Delay Time from CKOUT Rising Edge to the External Memory Access Address Out Valid Caused by First Interrupt Instruction Execution	$5T_C+T_H$	—	ns
264	CKOUT Rising Edge to TIO (output) Assertion	0	8	ns
265	CKOUT Rising Edge to TIO (output) Deassertion	0	8	ns
266	CKOUT Rising Edge to TIO (General Purpose Output)	0	8	ns

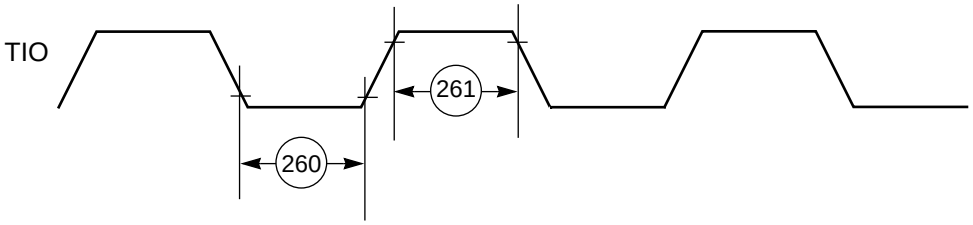


Figure 34 TIO Timer/ Event Input Restrictions

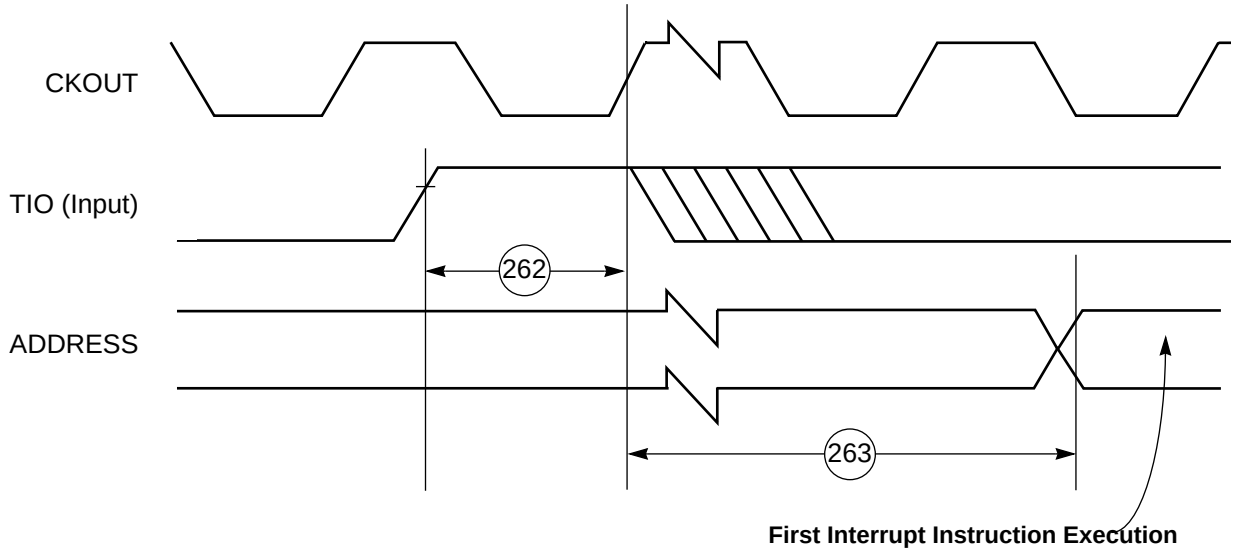


Figure 35 Timer Interrupt Generation

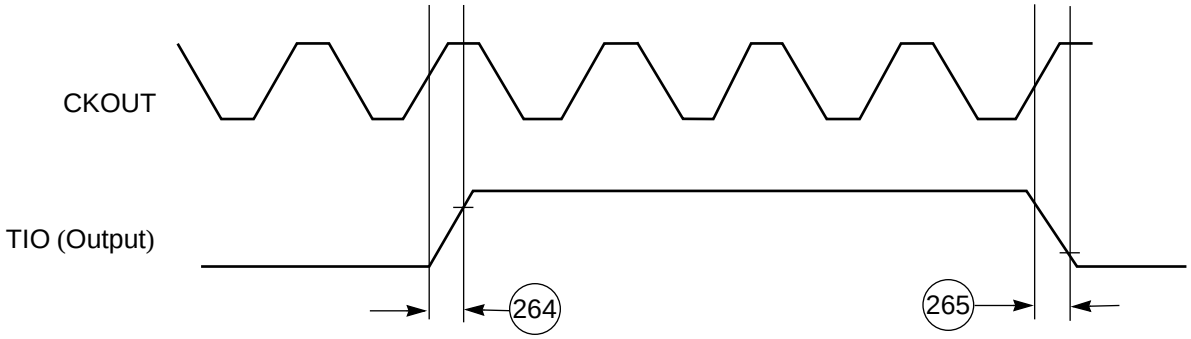


Figure 36 External Pulse Generation

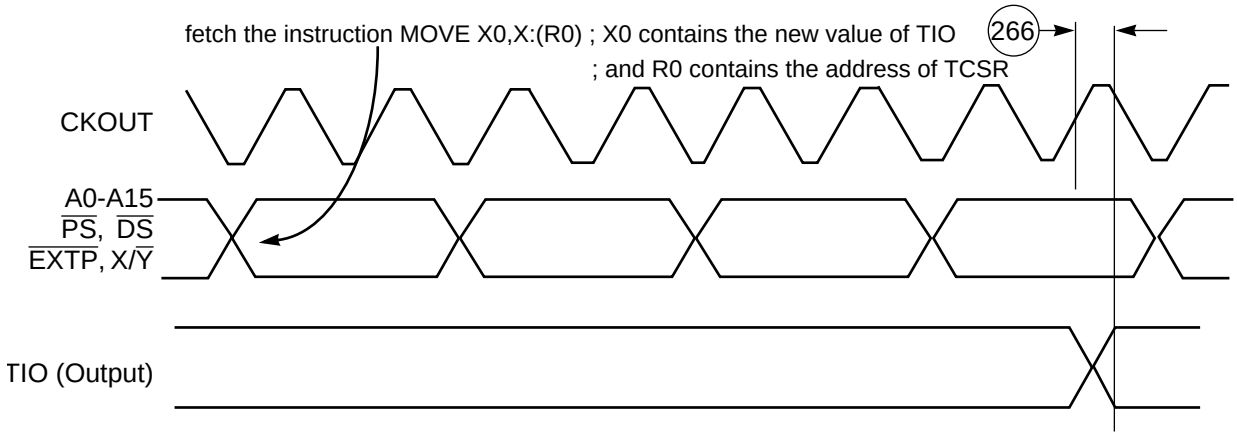


Figure 37 GPIO Output Timing

Pulse Width Modulator (PWM) Timing

V_{CC} = 5.0 Vdc ± 10%, T_J = -40° to +105°C, C_L = 50 pF + 2 TTL Load

WPS = PWM Prescale Factor
WCN = PWM Count
ick = Internal Clock
xck = External Clock

Table 21 PWM Timing

Num	Characteristics	50 MHz		Case	Unit
		Min	Max		
280	PWM External Clock Low (T_{WL})	T_C + 3	—		ns
281	PWM External Clock High (T_{WH})	T_C + 3	—		ns
282	PWM External Clock Cycle (T_{WC})	2 x T_C + 6	—		ns
283	PWM External Carrier Low	2 x T_C + 3 x WPS x T_C + 14 3 x T_C + T_{WC} + T_{WL} +14 3 x T_C + 1.5 x WPS x T_{WC} + 14	— — —	ick xck WPS = 1 xck WPS > 1	ns
284	PWM External Carrier High	15	—		ns
285	PWM Clock Rising Edge to PWM Output Assertion	—	2 x T_C+T_L+35		ns
286	PWM Carrier Rising Edge to PWM Output Assertion	3 x T_C 3 x T_C 3 x T_C	2 x T_C + 3 x WPS x T_C + 35 3 x T_C + T_{WC} + T_{WL} + 35 3 x T_C + 1.5 x WPS x T_{WC} + 35	ick xck WPS = 1 xck WPS > 1	ns
287	PWM Clock Rising Edge to PWM Output Deassertion	—	2 x T_C + T_L + 35	ns	ns
288	PWM Output Assertion Time (See Note)	2 x WCN x WPS x T_C - 3 WCN x WPS x T_{WC} - T_C - 3	2 x WCN x WPS x T_C + 3 WCN x WPS x TWC + T_C + 3	ick xck	ns
289	Synchronous PWM Rising Edge Clock Setup Time to CKOUT Falling Edge	12	T_C - 3		ns
290	Synchronous PWM Carrier Setup Time to CKOUT Rising Edge	14	T_C - 2		ns
291	CKOUT Rising Edge to PWM Output Assertion for Synchronous Operation	2 x T_C+WPS × T_C + 3 2 x T_C + T_{WL} + 3 2 x T_C + .5 x WPS x T_{WC} + 3	T_C + 3 x WPS x T_C + 26 T_C + T_{WC} + T_{WL} + 26 T_C + 1.5 x WPS x T_{WC} + 26	ick xck WPS = 1 xck WPS > 1	ns
292	PWM Output Assertion Time In Synchronous Operation	WCN x WPS x T_{WC} - 3	WCN x WPS x T_{WC} + 3	ns	ns

NOTE: If WCN=0 then the Output is not asserted at all.

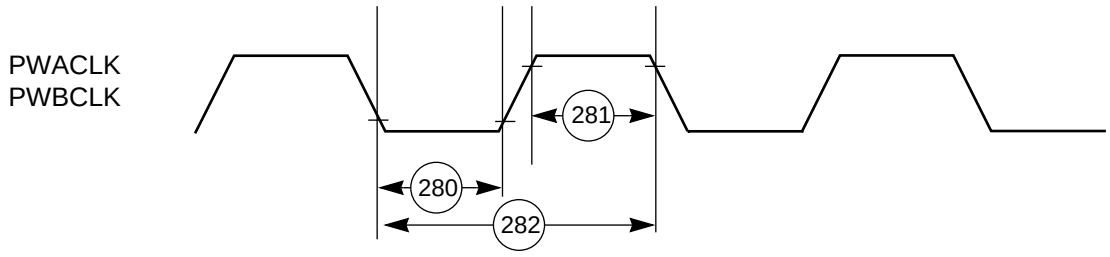


Figure 38 PWM Clock Input Restrictions

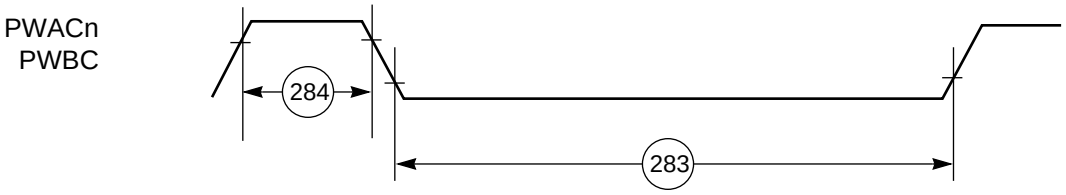


Figure 39 PWM Carrier Input Restrictions

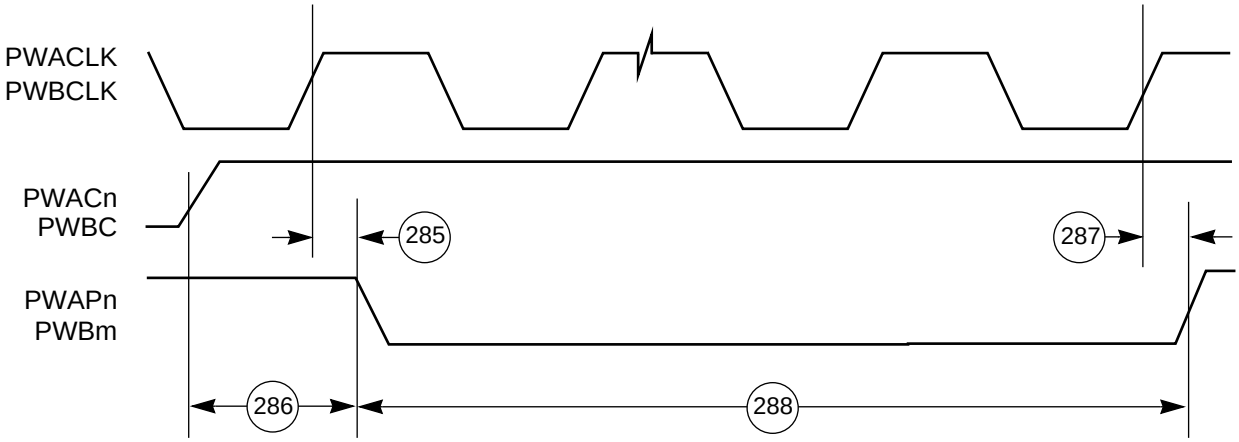


Figure 40 PWM Output Asynchronous Operation

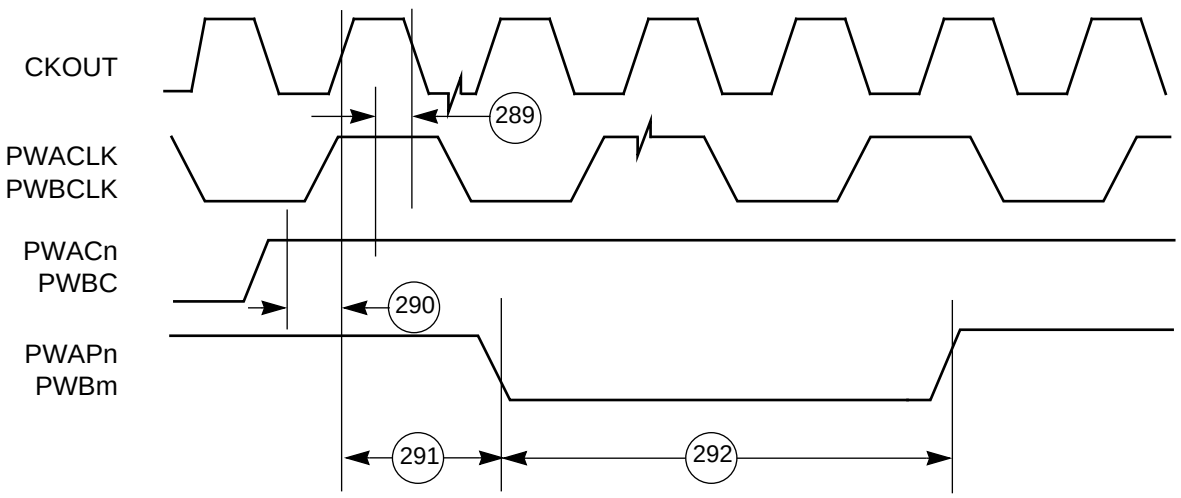
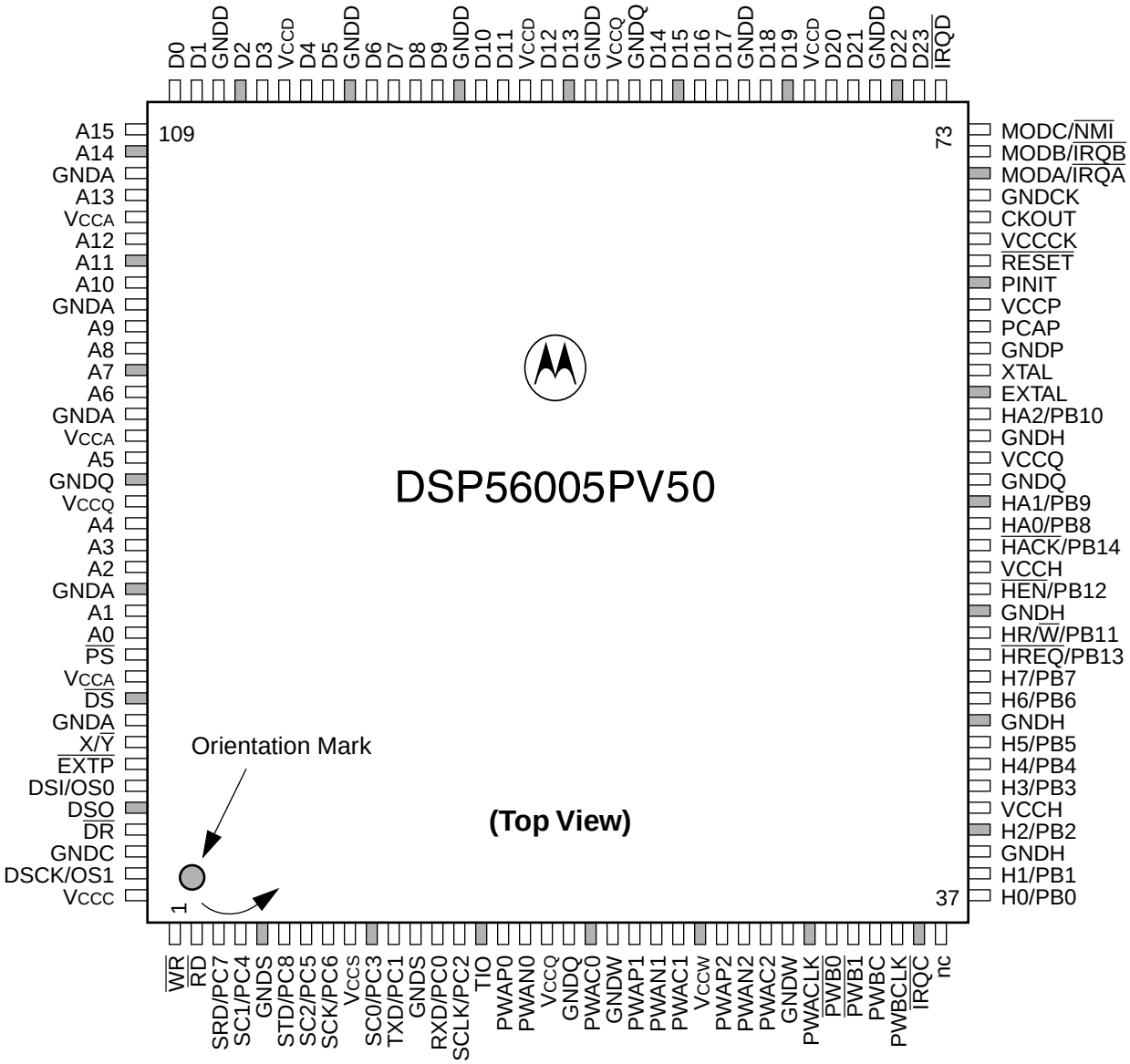


Figure 41 PWM Output Synchronous Operation

Pin-out and Package Information

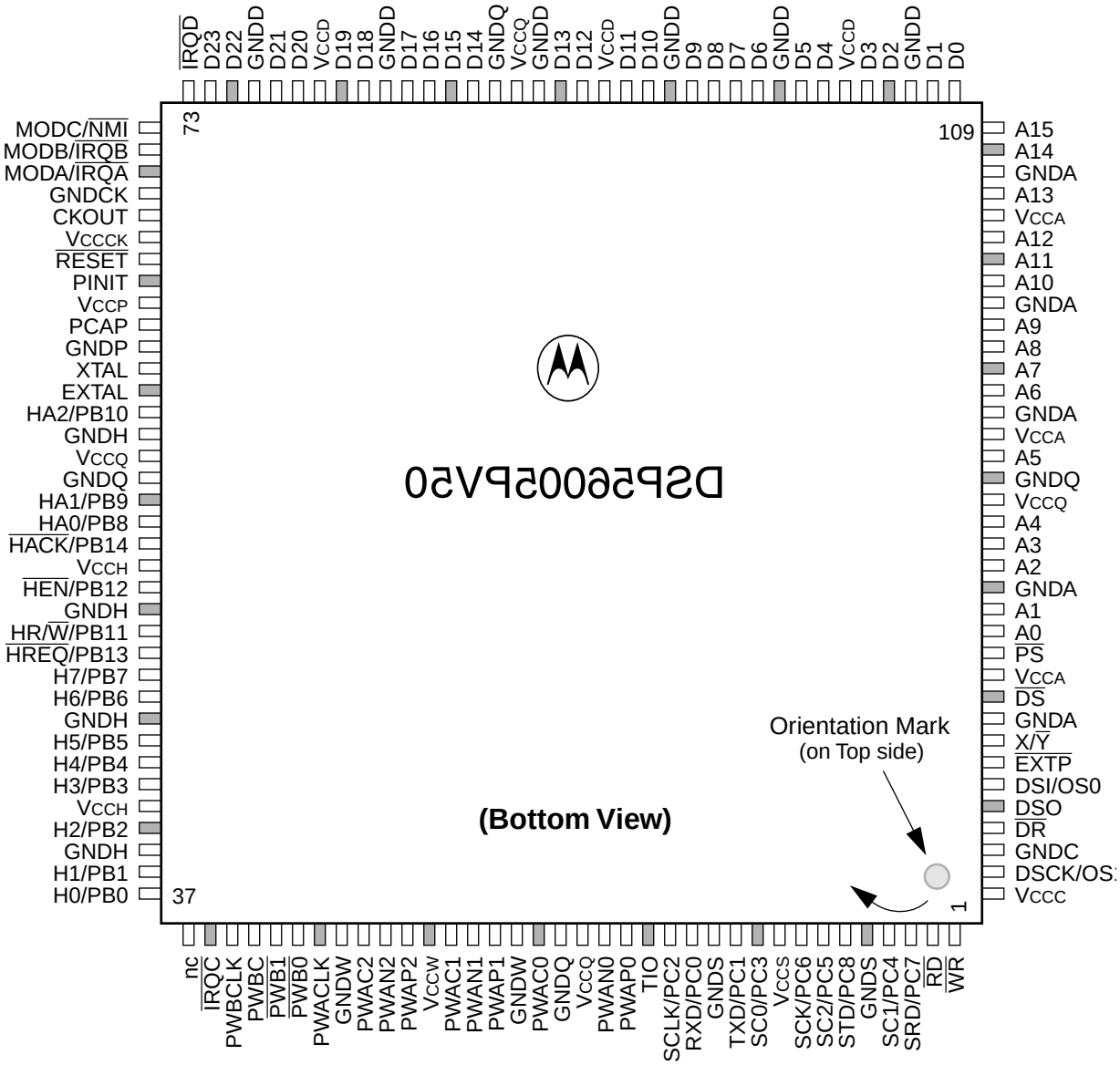
Top and bottom views of the Thin Quad Flat Package (TQFP) are shown in Figure 42 and Figure 43 with their pin-outs.



NOTES:

1. “nc” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
3. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 42 Top View of the DSP56005 144-pin Plastic Thin Quad Flat Package (TQFP)



NOTES:

4. “nc” are No Connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
5. An OVERBAR indicates the signal is asserted when the voltage = ground (active low).
6. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 43 Bottom View of the DSP56005 144-pin Plastic Thin Quad Flat Package (TQFP)

Shipping Tray

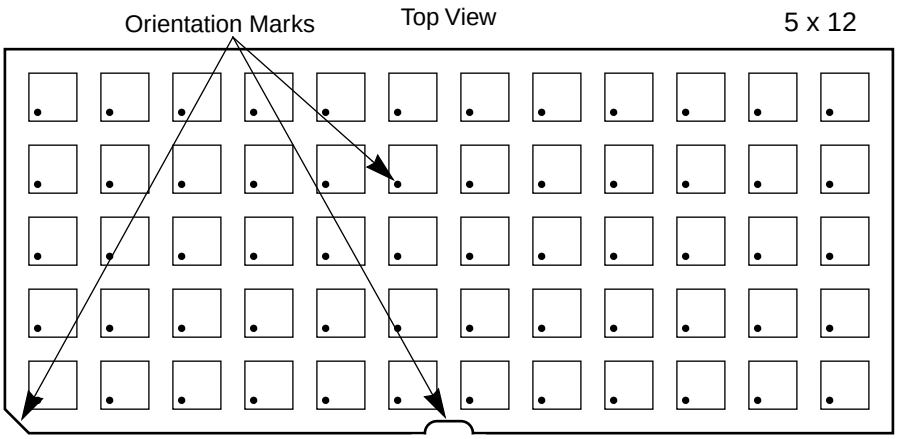


Figure 44 DSP56005 144-pin TQFP Shipping Tray

Pin-out and Package

By Pin Number

Pin-out and Package

By Pin Number

Pin-out and Package

By Signal Name

Pin-out and Package

By Signal Name

Power Supply Pins

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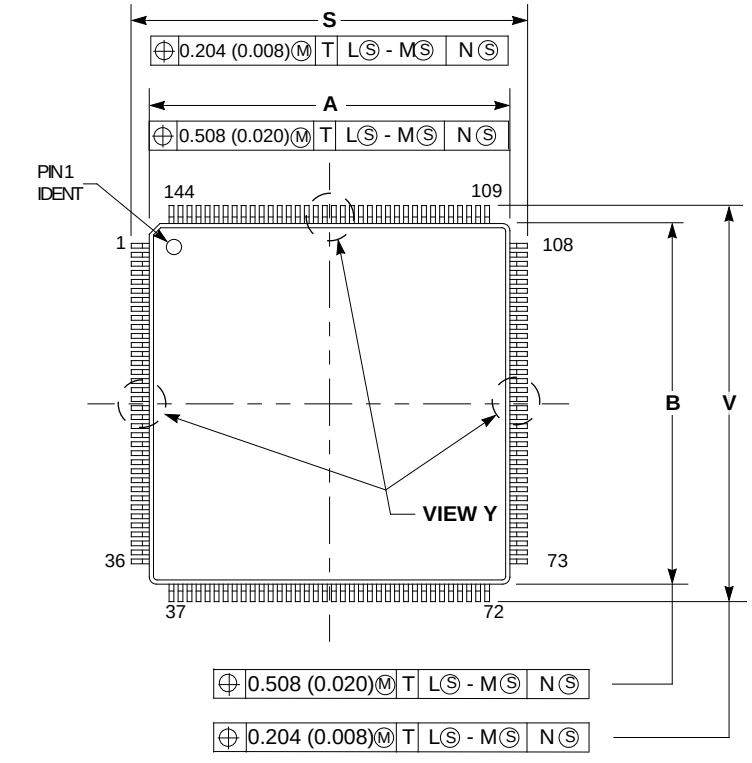
Table 25 DSP56005 Power Supply Pins

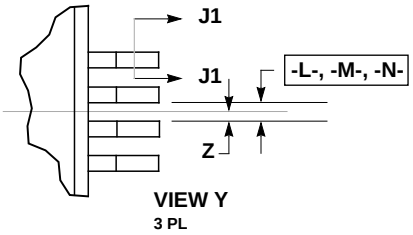
"005PV" 144-pin TQFP Pin	Power Supply	Circuit Supplied
113	V_{CCA}	Address Bus Buffers
123		
134		
111	GNDA	
117		
122		
130		
136		
144	V_{CCC}	Bus Control Buffers
142	GNDC	
67	V_{CCCK}	Clock
69	GNDCK	
79	V_{CCD}	Data Bus Buffers
92		
103		
76	GNDD	
82		
89		
95		
100		
106		

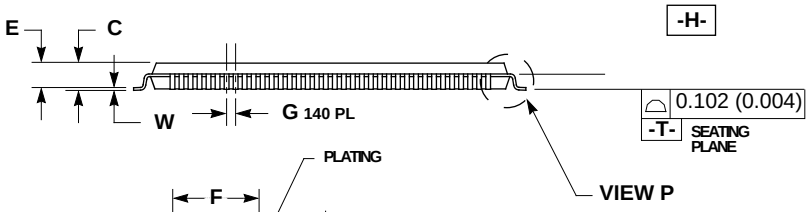
Table 25 DSP56005 Power Supply Pins (Continued)

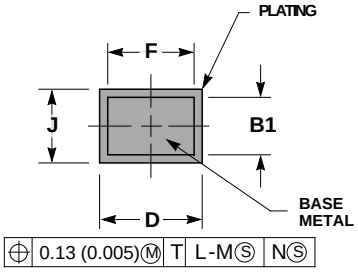
"005PV" 144-pin TQFP Pin	Power Supply	Circuit Supplied
41	V_{CCH}	Host Interface Buffers
52		
39	GNDH	
45		
50		
58		
18	V_{CCQ}	Internal Logic
57		
88		
126		
19	GNDQ	
56		
87		
125		
64	V_{CCP}	PLL
62	GNDP	
25	V_{CCW}	Pulse Width Modulator
21	GNDW	
29		
9	V_{CCS}	Serial Port
5	GNDS	
12		

Pin-out and Package

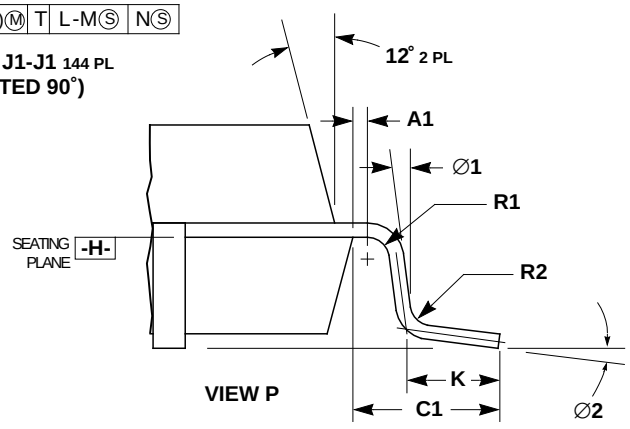








SECTION J1-J1 144 PL
(ROTATED 90°)



NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
2. Controlling dimension: millimeter.
3. Datum plane -H- is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datums -L-, -M- and -N- to be determined at datum plane -H-.
5. Dimensions S and V to be determined at seating plane -T-.
6. Dimensions A and B do not include mold protrusion. allowable protrusion is 0.25 (0.010) per side. Dimensions A and B do include mold mismatch and are determined at datum plane -H-.
7. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall be 0.08 (0.003) total in excess of the Ddimension at maximum material condition.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.900	20.100	0.783	0.791
B	19.900	20.100	0.783	0.791
C	1.400	1.600	0.056	0.062
D	0.170	0.280	0.0067	0.0110
E	1.350	1.450	0.054	0.057
F	0.160	0.270	0.063	0.011
G	0.500 BSC		0.197 BSC	
J	0.130	0.180	0.005	0.007
K	0.450	0.750	0.018	0.029
S	21.900	22.100	0.863	0.870
V	21.900	22.100	0.863	0.870
W	0.050	0.150	0.002	0.006
Z	0.250 BSC		0.0098 BSC	
A1	0.100	—	0.004	—
B1	0.100	0.150	0.004	0.006
C1	1.000 REF		0.039 REF	
R1	0.150 REF		0.006 REF	
R2	0.150	0.250	0.006	0.010
∅1	0 5	8 5	0 5	8 5
∅2	0 5	8 5	0 5	8 5

Figure 45 DSP56005 144-pin TQFP Mechanical Information

Design Considerations

Heat Dissipation

The average chip junction temperature, T_J, in °C, can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

T_A = ambient temperature, °C
Θ_{JA} = package thermal resistance, junction-to-ambient, °C / W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$ watts — chip internal power
$P_{I/O}$ = power dissipation on input and output pins — user determined

For most applications $P_{I/O} < P_{INT}$ and $P_{I/O}$ can be neglected. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K / (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273) + P_D \times \Theta_{JA} \quad (3)$$

Where: K is a constant pertaining to the particular package

K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A. The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JC} and Θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (Θ_{CA}). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA} \quad (4)$$

Θ_{JC} is device-related and cannot be influenced by the user. However, Θ_{CA} is user-dependent and can be minimized by thermal management techniques such as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management can significantly reduce Θ_{CA} so that Θ_{JA} approximately equals Θ_{JC}. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, “Thermal Resistance Measurement Method for MC68XX Microcomponent Devices”, and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

Note: Table 7, “Thermal Characteristics of the TQFP Package,” on page 21 contains the package thermal values for this chip.

Power, Ground, and Noise

Each DSP56005 V_{CC} pin should be provided with a low-impedance path to the board's supply. Each DSP56005 GND pin should also be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip as shown in Table 25, "DSP56005 Power Supply Pins," on page 77.

The V_{CC} power supply should be bypassed to GND using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be less than 0.5" per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes. All output pins on this DSP have fast rise and fall times. Printed Circuit Board (PCB) trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{RD}$, $\overline{WR}$, $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$, $\overline{HEN}$, and $\overline{HACK}$ pins. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Power Consumption

Power dissipation is a key issue in portable DSP applications. This section describes some factors which affect current consumption. This current consumption is described by the formula:

$$I = C \times V \times f$$

where: C = node / pin capacitance
V = voltage swing
f = frequency of node / pin toggle

For example, for a Port A address pin loaded with a 50 pF capacitance and operating at 5.5V with a 40 MHz clock, toggling at its maximum possible rate (which is 10 MHz), the current consumption is:

$$I = 50 \times 10^{-12} \times 5.5 \times 10 \times 10^{6} = 2.75 \text{ mA}$$

The Maximum Internal Current value (I_{CCI}-max), reflects the maximum possible switching of the internal buses, which is not necessarily a real application case. The Typical Internal Current value (I_{CCI}-typ) reflects the average switching of the internal buses.

The following steps are recommended for applications requiring very low current consumption:

1. minimize external memory accesses; use internal memory accesses instead
2. minimize the number of pins which are switching
3. minimize the capacitive load on the pins
4. connect the unused inputs to pull-up or pull-down resistors

Current consumption test code:

```
org  p:RESET
     jmp     MAIN
     org     p:MAIN
     movep   #$180000,x:$FFFD
     move    #0,r0
     move    #0,r4
     move    #$00FF,m0
     move    #$00FF,m4
     nop
     rep     #256
     move            r0,x:(r0)+
     rep     #256
     mov     r4,y:(r4)+
     clr     a
     move            l:(r0)+,a
     rep     #30
     mac     x0,y0,a x:(r0)+,x0
               y:(r4)+,y0
    move          a,p:(r5)
     jmp     TP1
TP1  nop
     jmp     MAIN
```

Host Port Considerations

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the host interface. The following paragraphs present considerations for proper operation.

Host Programming Considerations

1. Unsynchronized Reading of Receive Byte Registers
   When reading receive byte registers, RXH or RXL, the host program should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.

2. Overwriting Transmit Byte Registers
   The host program should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set, indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

3. Synchronization of Status Bits from DSP to Host
   HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF status bits are set or cleared from inside the DSP and read by the host processor (refer to *DSP56005 User's Manual* for descriptions of these status bits). The host can read these status bits very quickly without regard to the clock rate used by the DSP, but the state of the bit could be changing during the read operation. Generally, this is not a system problem, since the bit will be read correctly in the next pass of any host polling routine.
   However, if the host asserts $\overline{\text{HEN}}$ for more than timing number 31, with a minimum cycle time of timing number 31 + 32, then these status bits are guaranteed to be stable. Exercise care when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the host could read the wrong combination. Therefore, read the bits twice and check for consensus.

4. Overwriting the Host Vector
   The host program should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.

5. Cancelling a Pending Host Command Exception
   The host processor may elect to clear the HC bit to cancel the host command exception request at any time before it is recognized by the DSP. Because the host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the host command exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time that the HC bit is cleared.

6. Variance in the Host Interface Timing
   The Host Interface (HI) may vary (e.g. due to the PLL lock time at reset). Therefore, a host which attempts to load (bootstrap) the DSP56005 should first make sure that the part has completed its HI port programming (e.g. by setting the INIT bit in ICR then polling it and waiting it to be cleared, then reading the ISR or by writing the TREQ/RREQ together with the INIT and then polling INIT, ISR, and the $\overline{\text{HREQ}}$ pin).

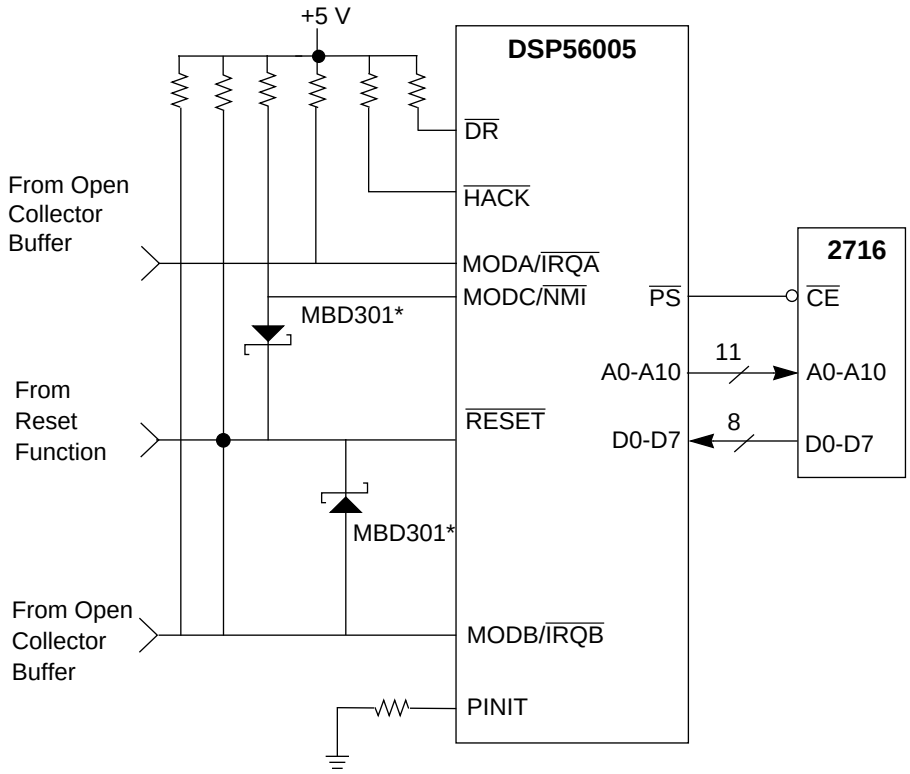
DSP Programming Considerations

1. Synchronization of Status Bits from Host to DSP
   DMA, HF1, HF0, and HCP, HTDE, and HRDF status bits are set or cleared by the host processor side of the interface. These bits are individually synchronized to the DSP clock. (Refer to the *DSP56005 User's Manual* for descriptions of these status bits.)

2. Reading HF0 and HF1 as an Encoded Pair
   Care must be exercised when reading status bits HF0 and HF1 as an encoded pair, i.e., the four combinations 00, 01, 10, and 11 each have significance. A very small probability exists that the DSP will read the status bits synchronized during transition. Therefore, HF0 and HF1 should be read twice and checked for consensus.

Application Examples

The lowest cost DSP56005 based system is shown in Figure 46. It uses no run time external memory and requires only two chips, the DSP56005 and a low cost EPROM. The EPROM read access time should be less than 300 nanoseconds when the DSP56005 is operating at a clock rate of 50 MHz.

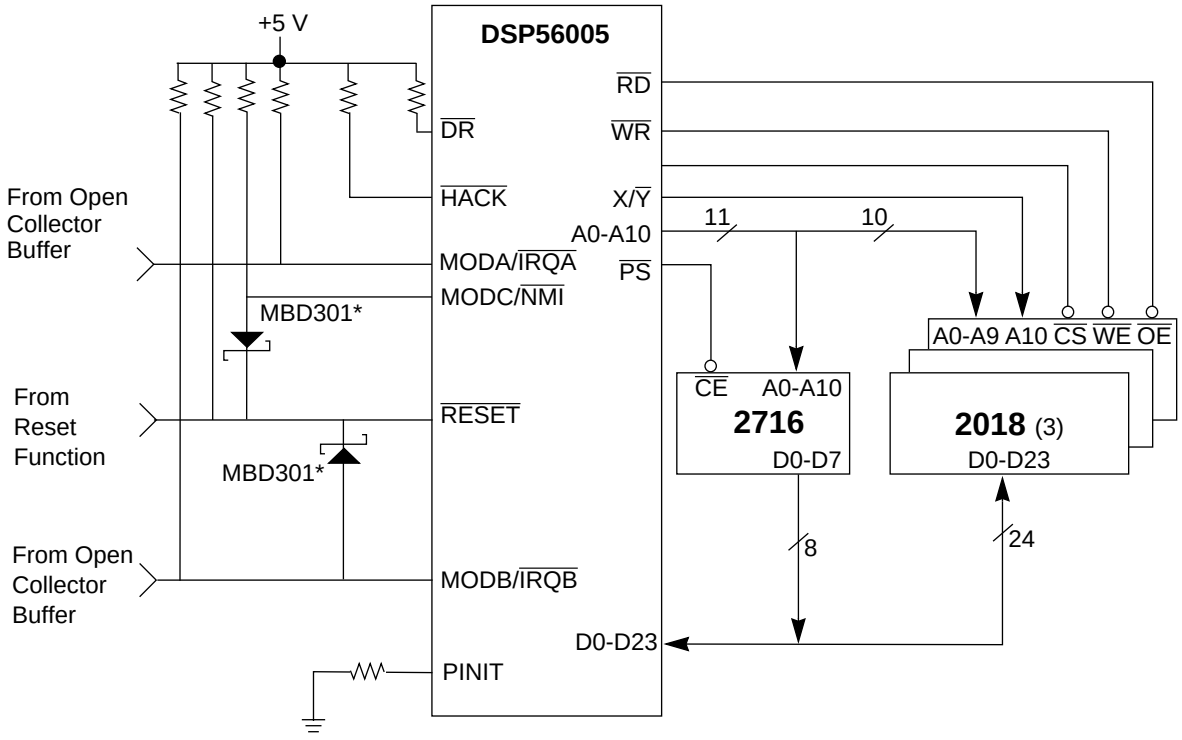


NOTES:

1. ***These diodes **must** be Schottky diodes.
2. All resistors are 15 KΩ unless noted otherwise.
3. When in Reset, IRQA, IRQB, and NMI must be deasserted by external peripherals.

Figure 46 No Glue Logic, Low Cost Memory Port Bootstrap — Mode 1

A system with external data RAM memory requires no glue logic to select the external EPROM from bootstrap mode. $\overline{PS}$ is used to enable the EPROM and $\overline{DS}$ is used to enable the high speed data memories as shown in Figure 47.



NOTES:

1. ***These diodes **must** be Schottky diodes.
2. All resistors are 15 KΩ unless noted otherwise.
3. When in Reset, $\overline{IRQA}$, $\overline{IRQB}$, and $\overline{NMI}$ must be deasserted by external peripherals.

Figure 47 Port A Bootstrap with External Data RAM — Mode 1

Figure 48 shows the DSP56005 bootstrapping via the Host Port from an MC68000.

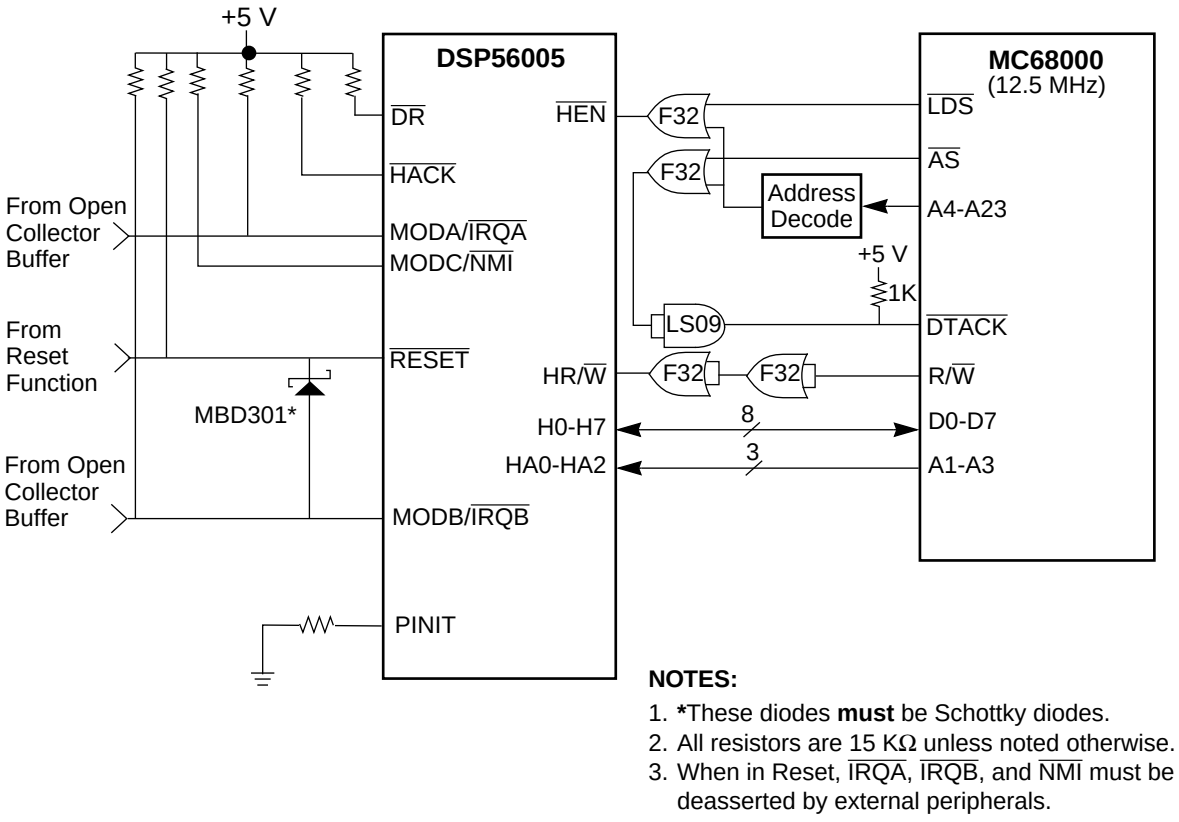


Figure 48 DSP56005 Host Bootstrap Example — Mode 5

In Figure 49, the DSP56005 is operated in mode 3 with external program memory at location $E000. The programmer can overlay the high speed on-chip P:RAM with DSP algorithms by using the MOVEM instruction.

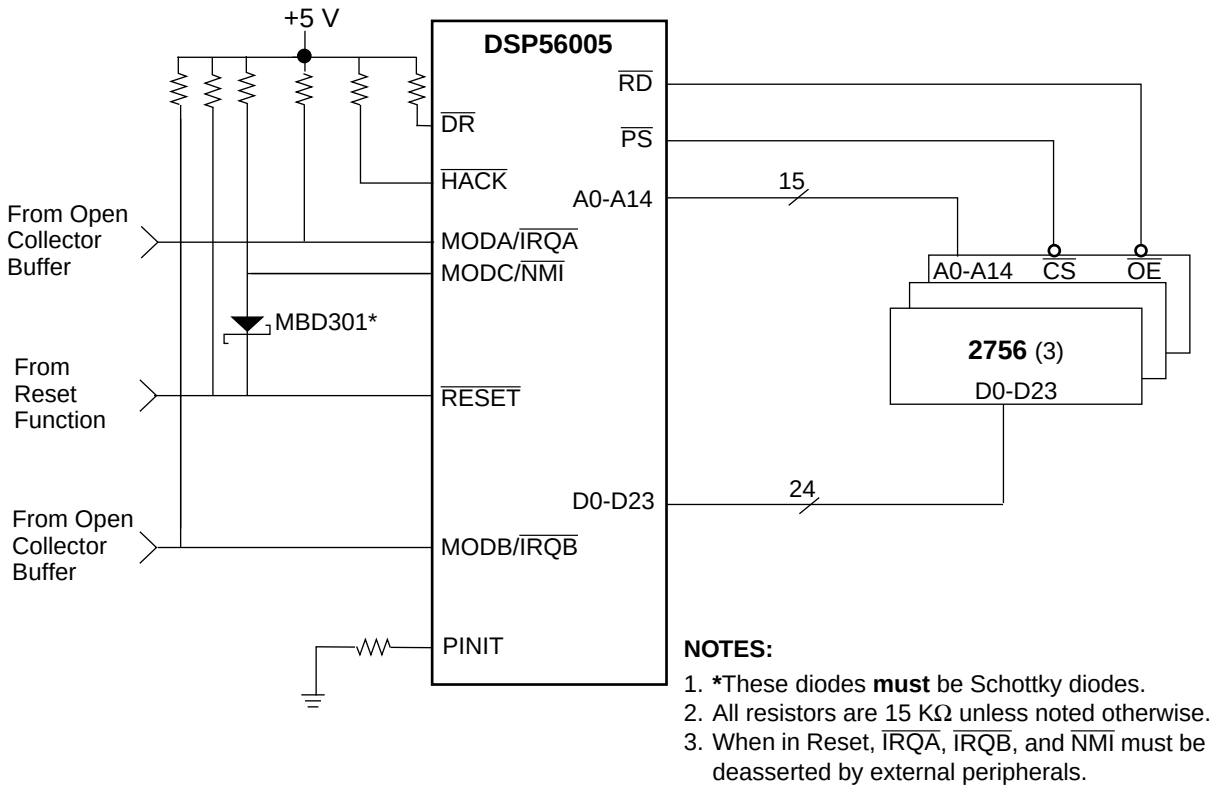


Figure 49 32K Words of External Program ROM — Mode 3

Figure 50 shows a circuit which waits until V_{CC} on the DSP56005 is at least 4.5 V before initiating a 75,000 × T_C oscillator stabilization delay required for the on-chip oscillator (only 25× T_C is required for an external oscillator without the PLL or 2500× T_C for an external oscillator with the PLL enabled). This insures that the DSP is operational and stable before releasing the reset signal.

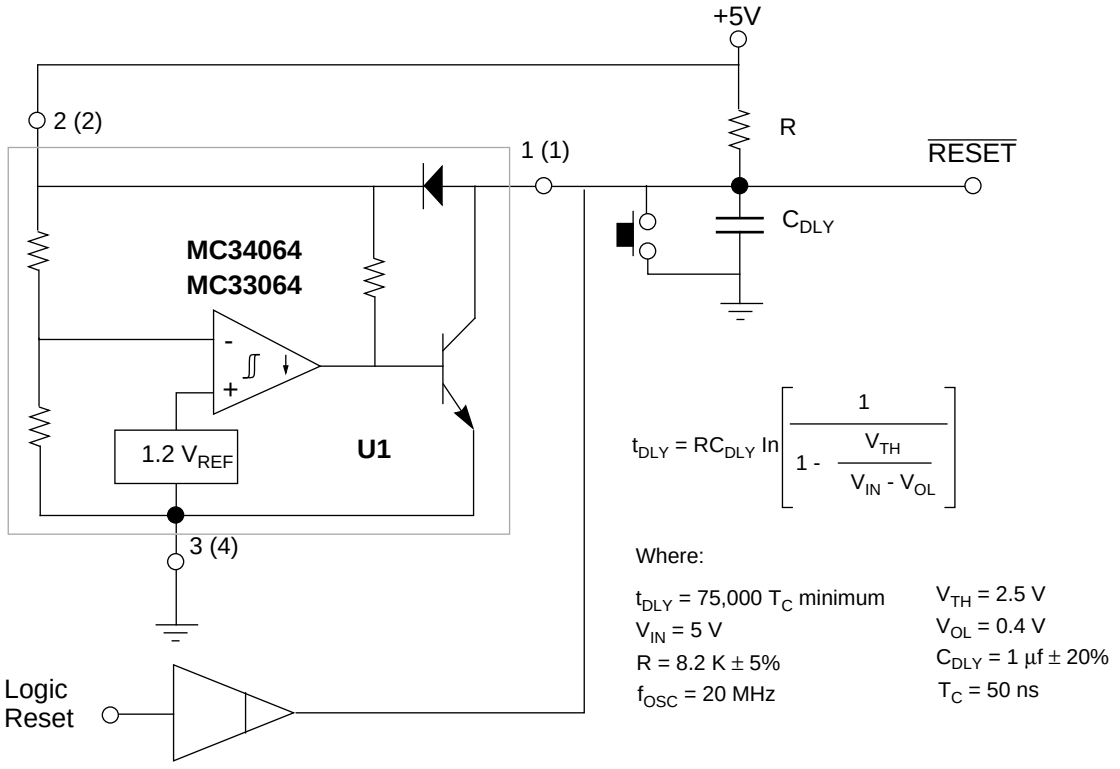


Figure 50 Reset Circuit Using MC34064/MC33064

Figure 51 shows the DSP56005 connected to the bus of an IBM-PC computer. This circuit is complete and does not require external ROM or RAM to load and execute code from the PC. The PAL equations and other details of this circuit are available in the application note entitled "DSP56001 Interface Techniques and Examples" (ARP11/D).

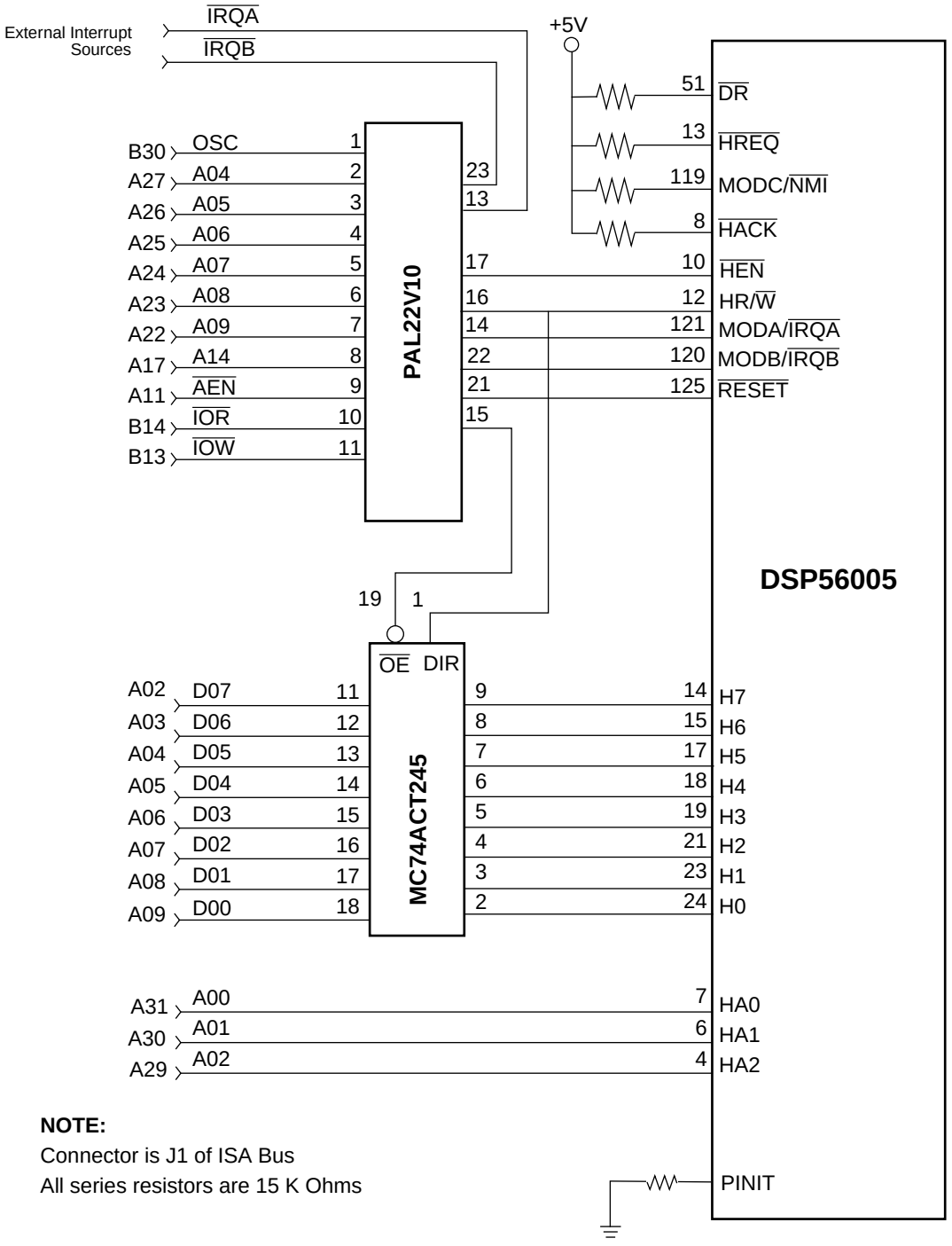


Figure 51 DSP56005 -to- ISA Bus Interface Schematic

Ordering Information

Table 26 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 26 DSP56005 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56005	5 V	Plastic Thin Quad Flat Pack (TQFP)	144	50	DSP56005PV50

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