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Order Number: MC145423/D
Rev. 0, 8/24/00

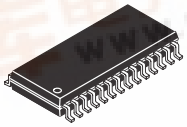
MOTOROLA
Semiconductor Products Sector

MC145423

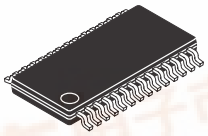
Product Preview

Universal Digital Loop Transceiver (UDLT-3)

Pin Selectable Master/Slave Limited Distance Modem



DW SUFFIX
SOIC
CASE 751F



DT SUFFIX
TSSOP
CASE 1168

ORDERING INFORMATION

MC145423DW	SOIC Package
MC145423DT	TSSOP Package

The MC145423 is a CMOS integrated circuit designed to be one of the major building blocks in digital subscriber voice/data telephone systems and remote data acquisition and control systems.

The UDLT-3 incorporates into one device, all the functionality of the MC145421 (ISDN UDLT-2 master), MC145425 (ISDN UDLT-2 slave), MC145422 (UDLT-1 master), and MC145426 (UDLT-1 slave).

Since these modes/functions are pin selectable, the MC145423 can be used in telephone switch line cards, as well as remote digital telsets or data terminals.

- V_{DD} = 4.5 V to 5.5 V
- 28-Pin SOIC and TSSOP Packages
- Protocol Independent
- Pin Controlled Power-Down
- LI Sensitivity Control in Master Mode
- 2.048 MHz Output in Slave Mode

UDLT-2 Features

- Synchronous Full Duplex 160 kbps Voice and Data Communications in a 2B+2D Format for ISDN Compatibility
- Provides CCITT Basic Access Data Transfer Rate (2B+D) for ISDNs on a Single Twisted Pair Up to 1 km on 26 AWG or Larger Cable

UDLT-1 Features

- Pin Controlled Loopback
- Automatic Power-Up/Down (Slave)
- Full Duplex Synchronous 64 kbps Voice/Data Channel and Two 8 kbps Signaling Data Channels Over One 26 AWG Wire Pair Up to 2 km

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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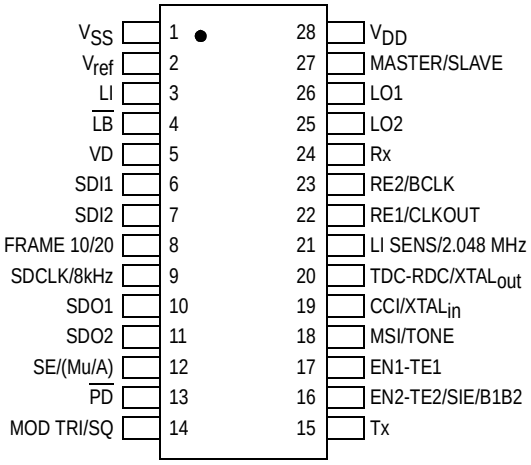
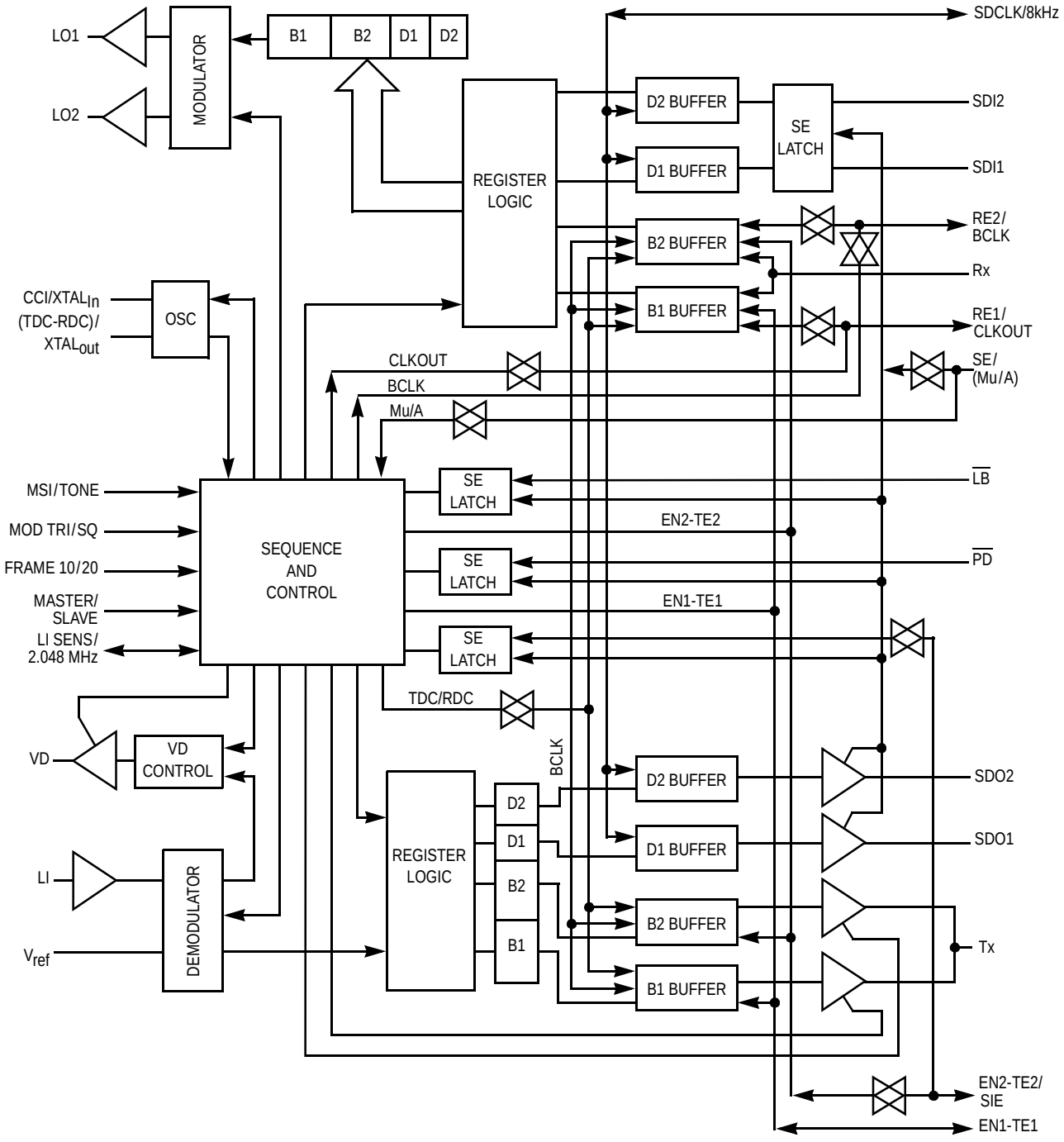
PIN ASSIGNMENT



28-PIN SOIC/TSSOP PACKAGES

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	–0.5 to 6	V
Voltage, Any Pin to V_{SS}	V	–0.5 to V_{DD} + 0.5	V
DC Current, Any Pin (Excluding V_{DD}, V_{SS})	I	±10	mA
Operating Temperature	T_A	–40 to 85	°C
Storage Temperature	T_{stg}	–85 to 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = –40° to 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.5	—	5.5	V
Power Dissipation ($\overline{PD}$ = V_{DD}) V_{DD} = 5 V	V_{DD}	—	—	80	mW
Power Dissipation ($\overline{PD}$ = V_{SS}) V_{DD} = 5 V	V_{DD}	—	—	80	mW
Frame Rate	MSI	7.9	8.0	8.1	kHz
CCI CLK Frequency (MSI = 8 kHz)	CCI				MHz
UDLT-1 (CCI = 256 x MSI)		—	2.048	—	
UDLT-2		—	8.192	8.29	
Frame Rate Slip*		—	—	0.25	%
Data Clock Rate (Master Mode)	TDC-RDC				kHz
UDLT-1		64	—	4100	
UDLT-2		128	—	4100	
SDCLK (UDLT-2 Only)		16	—	4100	kHz
Modulation Baud Rate	LO1, LO2				kHz
UDLT-1		—	—	256	
UDLT-2		—	—	512	

* The slave's crystal frequency divided by 512 (UDLT-1) or 1024 (UDLT-2), must equal the master's MSI frequency ±0.25% for optimum operation.

DIGITAL CHARACTERISTICS (V_{DD} = 5 V ±10%, T_A = –40° to 85°C, Unless Otherwise Stated)

Parameter		Min	Max	Unit
Input High Level		V_{DD} x 0.7	—	V
Input Low Level		—	V_{DD} x 0.3	V
Input Current (Digital Pins)		—	±1.0	µA
Input Current LI		—	±100	µA
Input Capacitance		—	7.5	pF
Output High Current (Excluding Tx and $\overline{PD}$)	$V_{OH} = V_{DD} – 0.5$ V	–1.6	—	mA
Output Current Low (Excluding Tx and $\overline{PD}$)	V_{OL} = 0.4V	1.6	—	mA
Tx Output High Current	V_{OH} = 2.5 V $V_{OH} = V_{DD} – 0.5$ V	–3.4 –2.5	— —	mA
Tx Output Low Current	V_{OL} = 0.4 V V_{OL} = 0.8 V	2.5 3.5	— —	mA
$\overline{PD}$ Output High Current — Slave Mode*	V_{OH} = 2.5 V $V_{OH} = V_{DD} – 0.5$ V	–90 –10	— —	µA
$\overline{PD}$ Output Low Current — Slave Mode*	V_{OL} = 0.8 V V_{OL} = 0.4 V	100 60	— —	µA
Tx, SDO1, SDO2, and VD Three-State Current		—	±10.0	µA
XTAL Output High Current	$V_{OH} = V_{DD} – 0.5$ V	–450	—	µA
XTAL Output Low Current	V_{OL} = 0.4 V	450	—	µA

* To overdrive $\overline{PD}$ from a low level to 3.5 V, or a high level to 1.5 V requires a minimum of ±800 µA drive capability.

ANALOG CHARACTERISTICS (V_{DD} = 5 V ±10%, T_A = –40° to 85°C)

Parameter		Min	Max	Unit
Modulation Differential Amplitude (RL = 440 Ω)	LO1 to LO2	4.5	6.0	Vp-p
Modulation Differential Offset		0	40	mV
V_{ref} Voltage, Typically 9/20 x ($V_{DD} – V_{SS}$)		2.0	2.5	V
PCM Tone Level		–22	–18	dBm
Demodulator Input Amplitude*		0.05	2.5	Vpeak
Demodulator Input Impedance (LI to V_{ref})		50	300	kΩ

* The input level into the demodulator to reliably demodulate incoming bursts. Input referenced to V_{ref}.

MASTER SWITCHING CHARACTERISTICS (V_{DD} = 5 V ±10%, T_A = –40° to 85°C, C_L = 50 pF)

Parameter	Figure No.	Symbol	Min	Max	Unit
Input Rise Time: All Digital Inputs		t_r	—	2	µs
Input Fall Time: All Digital Inputs		t_f	—	2	µs
Pulse Width: TDC, RDC, RE1, RE2, MSI, SDCLK (UDLT-2)		t_p	 90	 —	ns
CCI Duty Cycle		$t_{w2(H,L)}$	45	55	%
Propagation Delay: MSI to SDO1, SDO2, VD ($\overline{PD}$ = V_{DD}) TDC to Tx		t_{PLH}, t_{PHL}	 — —	 50 50	ns
MSI, TE1, TE2, RE1, RE2 to TDC-RDC Setup Time		t_{su3}	20	—	ns
TDC-RDC to MSI, TE1, TE2, RE1, RE2, Hold Time		t_{h5}	50	—	ns
Rx to TDC-RDC Setup Time		t_{su5}	30	—	ns
Rx to TDC-RDC Hold Time		t_{h1}	30	—	ns
SDI1, SDI2 to MSI Setup Time		t_{su2}	30	—	ns
SDI1, SDI2 to MSI Hold Time		t_{h2}	30	—	ns
MSI Rising Edge to First SDCLK Falling Edge (UDLT-2 Only)		t_{P1LH}	—	50	ns
TE Rising Edge to First Tx Data Bit Valid		t_{su6}	—	50	ns
TDC-RDC Rising Edge to Tx Data Bits 2 – 8 Valid		t_{su7}	—	50	ns
TE1,TE2 Falling Edge to Tx High Impedance		t_{dly}	—	70	ns
SDCLK Rising Edge to SDO1, SDO2 Bit Valid (UDLT-2 Only)		t_{su8}	—	135	ns
SDI1, SDI2 Data Setup (Data Valid Before SDCLK Falling Edge) (UDLT-2 Only)		t_{su9}	50	—	ns
SDI1, SDI2 Data Hold (Data Valid After SDCLK Falling Edge) (UDLT-2 Only)		t_{h3}	20	—	ns
$\overline{PD}$, $\overline{LB}$ Setup ($\overline{PD}$, $\overline{LB}$ Valid Before MSI Rising Edge)		t_{su10}	50	—	ns
$\overline{PD}$, $\overline{LB}$ Hold ($\overline{PD}$, $\overline{LB}$ Valid After MSI Rising Edge)		t_{h4}	20	—	ns

SLAVE SWITCHING CHARACTERISTICS (V_{DD} = 5 V ±10%, T_A = –40° to 85°C, C_L = 50 pF)

Parameter	Figure No.	Symbol	Min	Max	Unit
Input Rise Time: All Digital Inputs		t_r	—	2	µs
Input Fall Time: All Digital Inputs		t_f	—	2	µs
Clock Output Pulse Width: BCLK		$t_{w(H,L)}$	3.66	4.15	µs
Crystal Frequency		f_{x1}	4.086	4.1	MHz
Propagation Delay Times:					ns
EN1, EN2, TE1 Rising to BCLK (TONE = V_{DD})		t_{p1}	–50	175	
EN1, EN2, TE1 Rising to BCLK (TONE = V_{SS})		t_{p1}	300	400	
BCLK to EN1, EN2, TE1 Falling		t_{p2}	—	20	
RE1 Rising to BCLK (UDLT-1)		t_{p3}	—	20	
RE1 Falling to BCLK (TONE = V_{DD}) (UDLT-1)		t_{p4}	–50	50	
RE1 Falling to BCLK (TONE = V_{SS}) (UDLT-1)		t_{p4}	300	400	
BCLK to Tx		t_{p5}	—	50	
TE1,TE2 to SDO1, SDO2		t_{p6}	—	50	
Rx to BCLK Setup Time		t_{su5}	30	—	ns
Rx to BCLK Hold Time		t_{h1}	30	—	ns
SDI1, SDI2 to TE Setup Time		t_{su6}	30	—	ns
SDI1, SDI2 to TE Hold Time		t_{h2}	30	—	ns
EN1, EN2 Rising Edge to DCLK Rising Edge (UDLT-2)		t_{PHL}	—	±30	ns
EN1, EN2 Rising Edge to First Tx Data Bit Valid		t_{dly1}	—	30	ns
BCLK Rising Edge to Tx Data Bits 2 – 8 Valid		t_{su7}	—	–40	ns
DCLK Pulse Width High (UDLT-2)		$t_{w(H)}$	31	31.5	µs
DCLK Pulse Width Low (UDLT-2)		$t_{w(L)}$	31	31.5	µs
DCLK Rising Edge to SDO1, SDO2 (UDLT-2)		t_{dly2}	—	30	ns
SDI1, SDI2 Setup (SDI1, SDI2 Valid Before DCLK Falling Edge) (UDLT-2)		t_{su9}	10	—	ns
SDI1, SDI2 Hold (SDI1, SDI2 Valid After DCLK Falling Edge) (UDLT-2)		t_{h3}	—	30	ns
EN1, TE1 Rising Edge to VD Valid		t_{dly3}	—	30	ns

SE PIN TIMING

Parameter	Figure No.	Symbol	Min	Max	Unit
$\overline{LB}$, $\overline{PD}$ Hold ($\overline{LB}$, $\overline{PD}$ Valid After SE Falling Edge)		t_h	10	—	ns
SDO1, SDO2, VD High Impedance After SE Falling Edge		t_{dly1}	—	40	ns
SDO1, SDO2, VD Valid After SE Rising Edge		t_{dly2}	30	—	ns
$\overline{LB}$, $\overline{PD}$ Setup ($\overline{LB}$, $\overline{PD}$ Valid Before SE Rising Edge)		t_{su}	25	—	ns

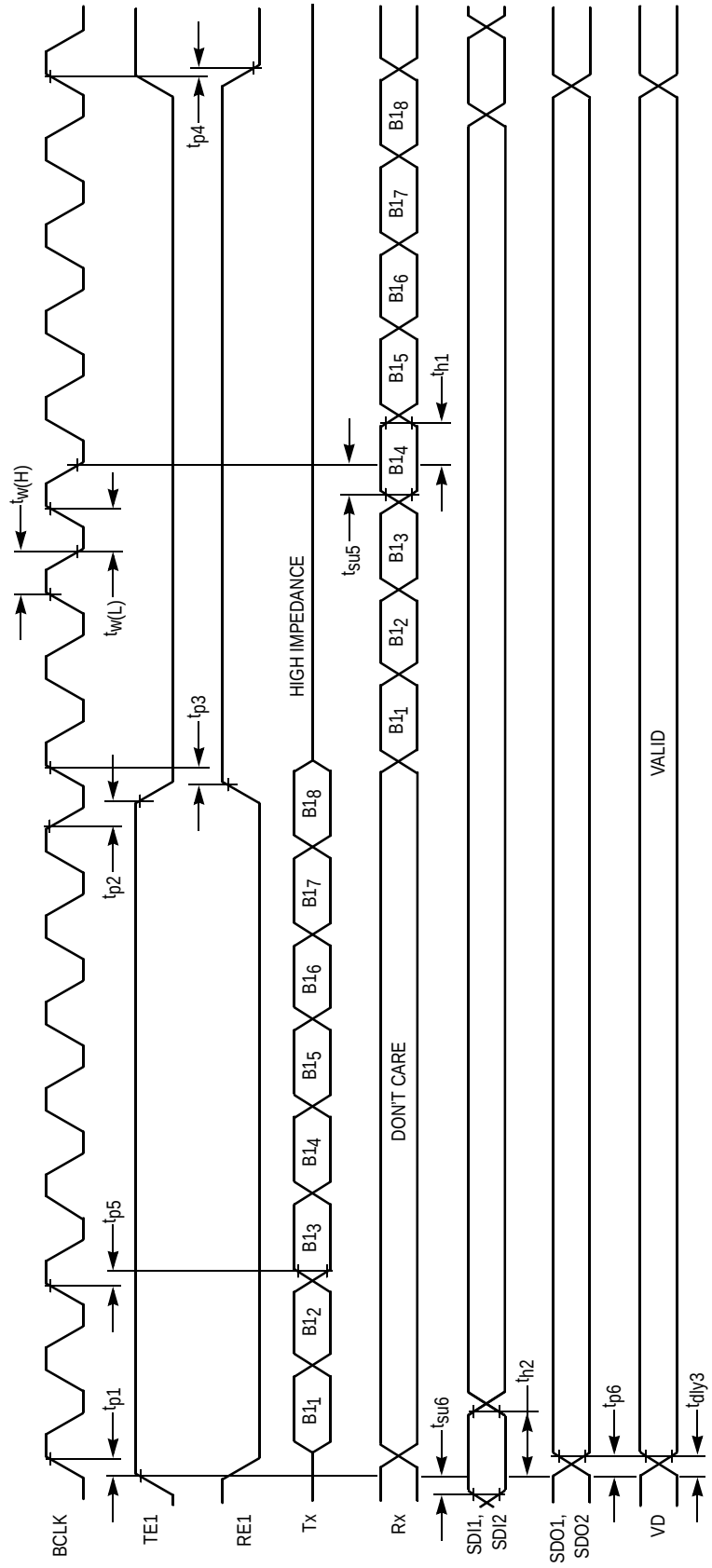


Figure 1. UDLT-1 Slave Timing Nonsynchronous

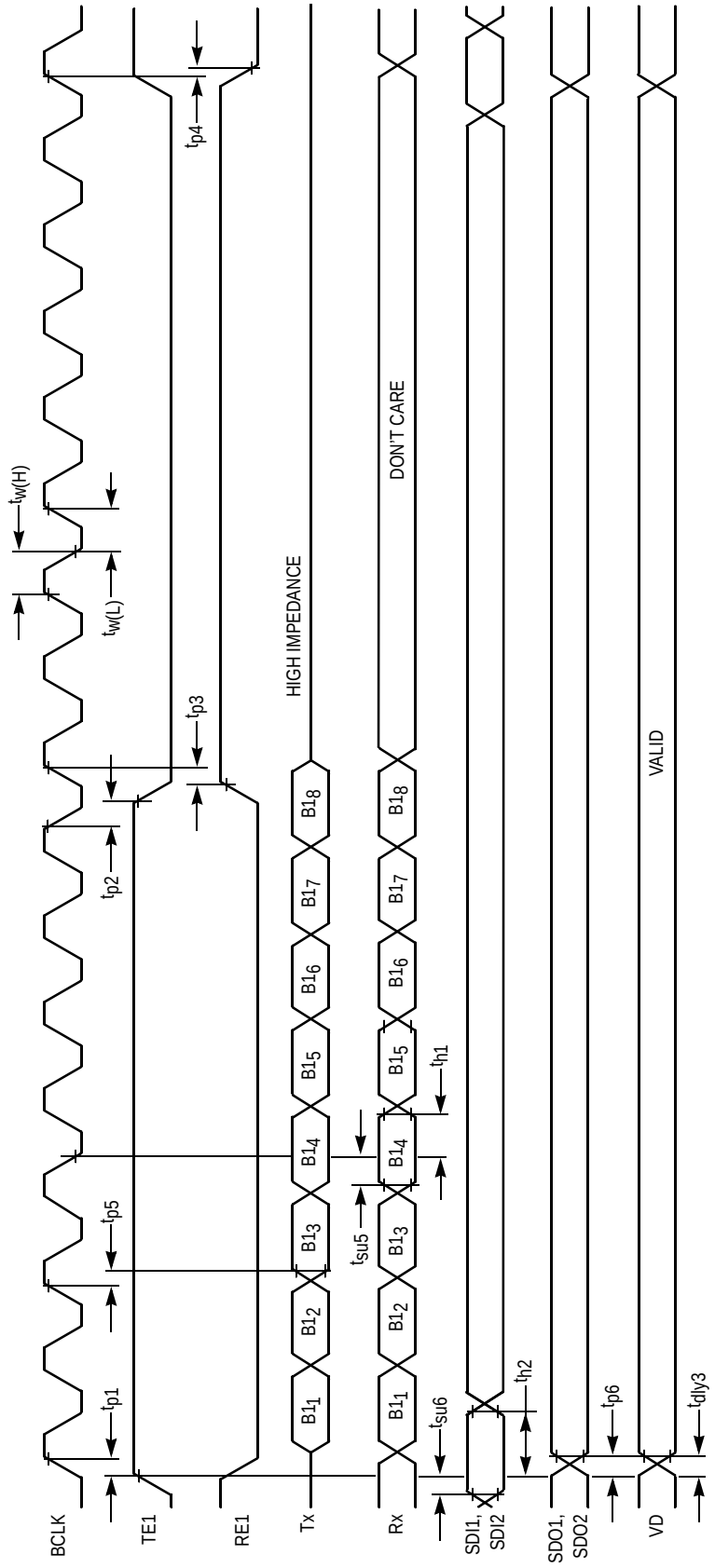


Figure 2. UDLT-1 Slave Timing Synchronous

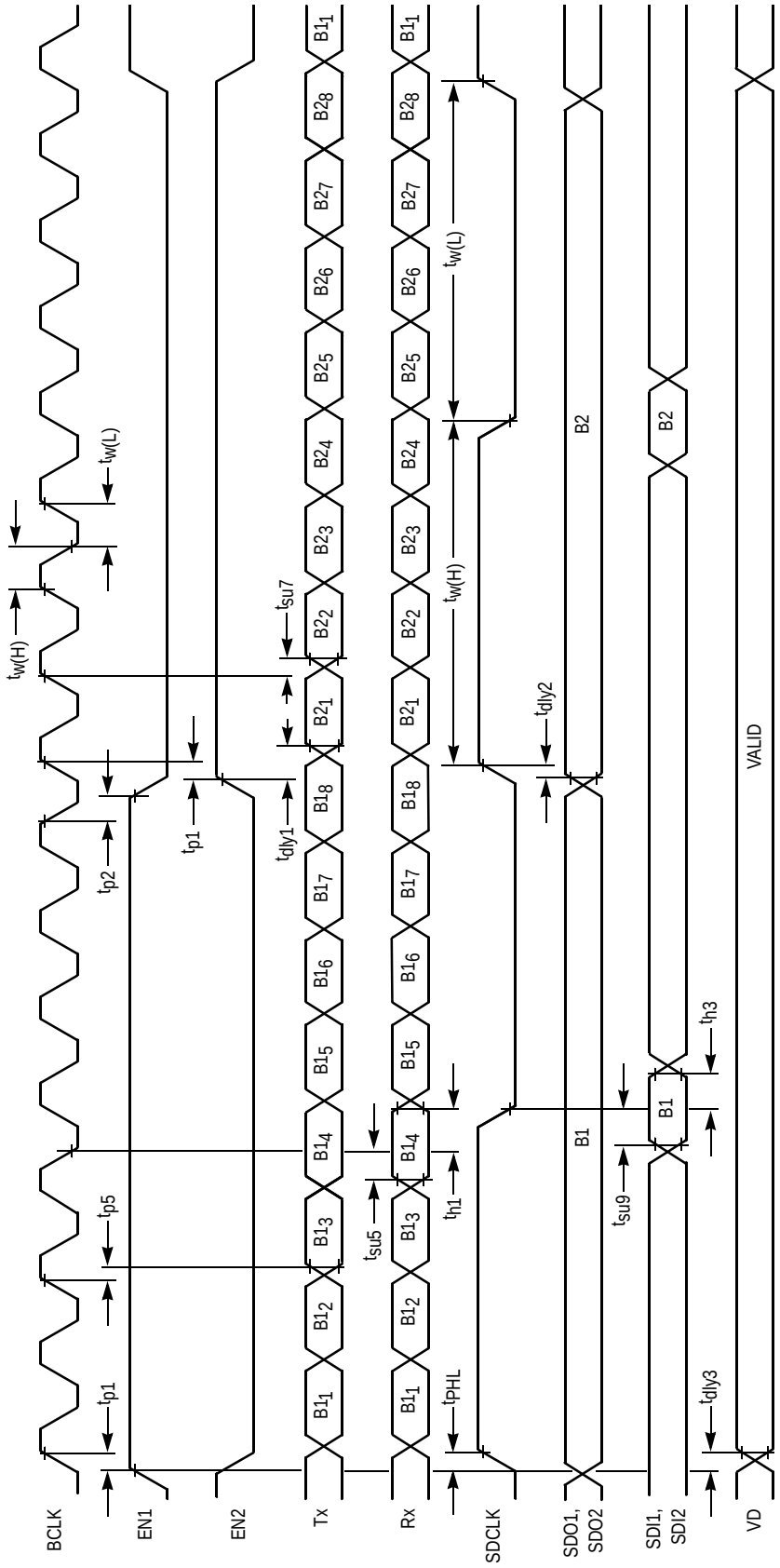


Figure 3. UDLT-2 Slave Timing

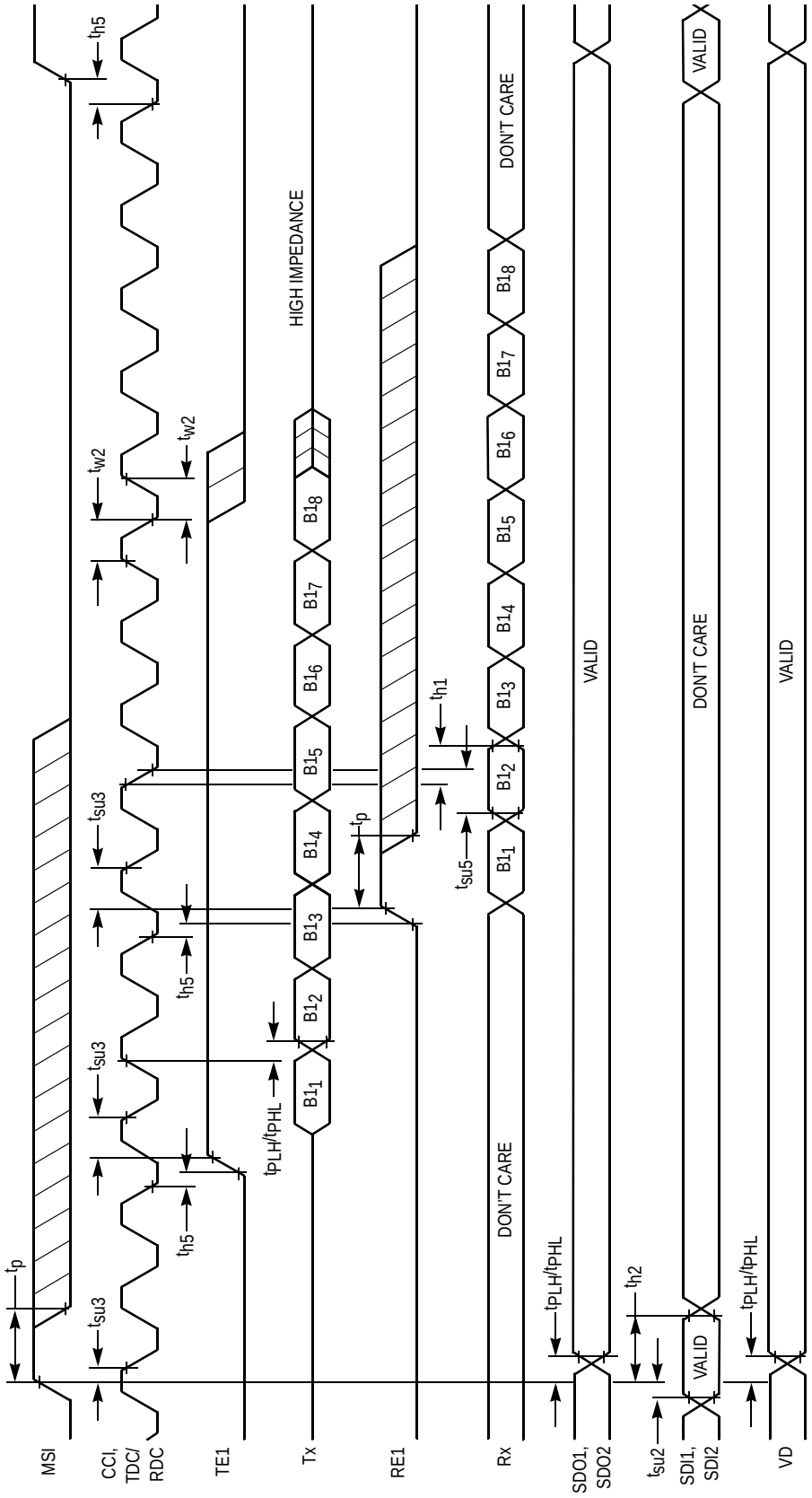


Figure 4. UDLT-1 Master Timing

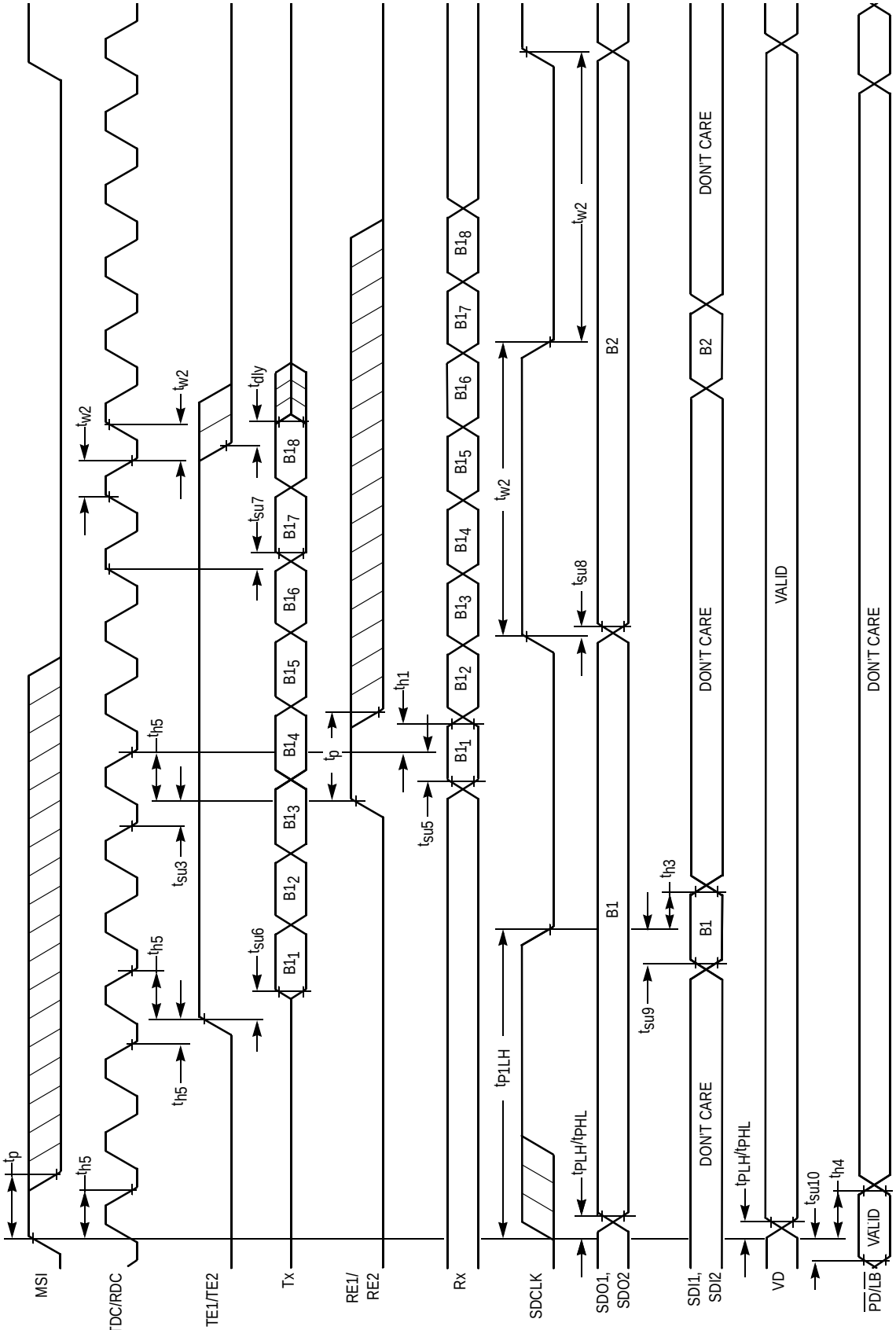


Figure 5. UDLT-2 Master Timing

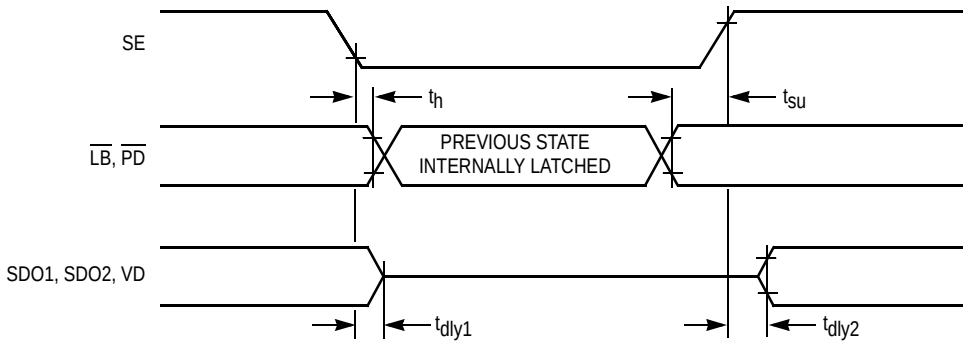


Figure 6. SE Pin Timing

SOIC PACKAGE PINOUT COMPARISON

UDLT-3 PINOUT VERSUS MC145421DW/22DW/25DW/26DW (UDLT-1/UDLT-2 MASTER/SLAVE) PINOUT

UDLT-3 MC145423		UDLT-1 Master MC145422		UDLT-1 Slave MC145426		UDLT-2 Master MC145421		UDLT-2 Slave MC145425	
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**	**Pin No.**	**Pin Name**
1	V_{SS}	1	V_{SS}	1	V_{SS}	1	V_{SS}	1	V_{SS}
2	V_{ref}	2	V_{ref}	2	V_{ref}	2	V_{ref}	2	V_{ref}
3	LI	3	LI	3	LI	3	LI	3	LI
4	$\overline{LB}$	5	$\overline{LB}$	5	$\overline{LB}$	4	$\overline{LB}$	4	$\overline{LB}$
5	VD	6	VD	6	VD	5	VD	5	VD
6	SDI1	7	SI1	7	SI1	6	D1I	6	DI1
7	SDI2	9	SI2	9	SI2	7	D2I	7	DI2
8	FRAME 10/20	Logic 0		Logic 0		Logic 1		Logic 1	
9	SDCLK/8kHz	High Impedance		SDCLK		8	DCLK	8	DCLK
10	SDO1	8	SO1	8	SO1	9	D1O	9	D1O
11	SDO2	10	SO2	10	SO2	10	D2O	10	D2O
12	SE/(Mu/A)	11	SE	11	Mu/A	11	SE	11	(Mu/A)
13	$\overline{PD}$	12	$\overline{PD}$	12	$\overline{PD}$	12	$\overline{PD}$	12	$\overline{PD}$
14	MOD TRI/SQ	Logic 0		Logic 0		Logic 1		Logic 1	
15	Tx	16	Tx	15	Tx	13	Tx	13	Tx
16	EN2-TE2/SIE/ B1B2	14	SIE	B1B2 Logic 0		14	TE2	14	EN2
17	EN1-TE1	15	TE1	14	TE1	15	TE1	15	EN1
18	MSI/TONE	13	MSI	13	(Tone) TE	16	MSI	16	TONE
19	CCI/$XTAL_{in}$	17	CCI	16	($XTAL_{in}$) X1	17	CCI	17	($XTAL_{in}$) CCI
20	TDC-RDC/ $XTAL_{out}$	18	TDC/RDC	17	($XTAL_{out}$) X2	18	TDC/RDC	18	($XTAL_{out}$) XTL
21	LI SENS/ 2.048 MHz	Logic 0 LI SENS		2.048 MHz Out		Logic 0 LI SENS		2.048 MHz Out	
22	RE1/CLKOUT	20	RE1	20	RE1	19	RE1	19	CLKOUT
23	RE2/BCLK	High Impedance		18	(BCLK) CLK	20	RE2	20	BCLK
24	Rx	19	Rx	19	Rx	21	Rx	21	Rx
25	LO2	22	LO2	22	LO2	22	LO2	22	LO2
26	LO1	23	LO1	23	LO1	23	LO1	23	LO1
27	MASTER/ SLAVE	Logic 0		Logic 1		Logic 0		Logic 1	
28	V_{DD}	24	V_{DD}	24	V_{DD}	24	V_{DD}	24	V_{DD}

MC145423 UDLT-3 PIN STATES FOR UDLT-1 SLAVE MODE

MC145423			UDLT-1 Slave Mode Powered-Up		UDLT-1 Slave Mode Powered-Down			
					TONE = 0, Off		TONE = 1, On	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**
1	V_{SS}	Power	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd
2	V_{ref}	Analog Ref	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$
3	LI	Input	Analog In	Analog In	Analog In	Analog In	Analog In	Analog In
4	$\overline{\text{LB}}$	Input	1	0	Don't Care	Don't Care	Don't Care	Don't Care
5	VD	Output	Digital Out	Digital Out	VD = 0	VD = 1	VD = 0	VD = 1
6	SDI1	Input	8 kbps Data In	8 kbps Data In	Don't Care	Don't Care	Don't Care	Don't Care
7	SDI2	Input	8 kbps Data In	8 kbps Data In	Don't Care	Don't Care	Don't Care	Don't Care
8	FRAME 10/20	Input	0	0	0	0	0	0
9	SDCLK/ 8kHz	Output	SDCLK/8kHz	SDCLK/8kHz	High-Z, Not Used	High-Z, Not Used	High-Z, Not Used	High-Z, Not Used
10	SDO1	Output	8 kbps Data Out	8 kbps Data Out	Data Not Changed	8 kbps Data Out	Data Not Changed	8 kbps Data Out
11	SDO2	Output	8 kbps Data Out	8 kbps Data Out	Data Not Changed	8 kbps Data Out	Data Not Changed	8 kbps Data Out
12	SE/(Mu/A)	Input	1= Mu, 0 = A	1= Mu, 0 = A	1= Mu, 0 = A	1= Mu, 0 = A	1= Mu, 0 = A	1= Mu, 0 = A
13	$\overline{\text{PD}}$	I/O	1	1	0	0	0	0
14	MOD TRI/SQ	Input	0	0	0	0	0	0
15	Tx	Output	64 kbps Data Out	64 kbps Data Out	High Impedance	64 kbps Data Out	64 kbps PCM Tone	64 kbps PCM Tone
16	EN2-TE2/ SIE/B1B2	Input	1/0 B1B2	1/0 B1B2	1/0 B1B2	1/0 B1B2	1/0 B1B2	1/0 B1B2
17	EN1-TE1	Output	EN1 = 8 kHz	EN1 = 8 kHz	EN1 = 0	EN1 = 8 kHz	EN1 = 8 kHz	EN1 = 8 kHz
18	MSI/ TONE	Input	1/0 TONE	1/0 TONE	TONE = 0	TONE = 0	TONE = 1	TONE = 1
19	CCI/ $XTAL_{in}$	Input	$XTAL_{in}$ 4.096 MHz	$XTAL_{in}$ 4.096 MHz	$XTAL_{in}$ 4.096 MHz	$XTAL_{in}$ 4.096 MHz	$XTAL_{in}$ 4.096 MHz	$XTAL_{in}$ 4.096 MHz
20	TDC-RDC/ $XTAL_{out}$	Output	$XTAL_{out}$ 4.096 MHz	$XTAL_{out}$ 4.096 MHz	$XTAL_{out}$ 4.096 MHz	$XTAL_{out}$ 4.096 MHz	$XTAL_{out}$ 4.096 MHz	$XTAL_{out}$ 4.096 MHz
21	LI SENS/ 2.048 MHz	Output	2.048 MHz	2.048 MHz	2.048 MHz	2.048 MHz	2.048 MHz	2.048 MHz
22	RE1/ CLKOUT	Output	RE1 = 8 kHz	RE1 = 8 kHz	RE1 = 1	RE1 = 8 kHz	RE1 = 8 kHz	RE1 = 8 kHz

MC145423 UDLT-3 PIN STATES FOR UDLT-1 SLAVE MODE (continued)

MC145423			UDLT-1 Slave Mode Powered-Up		UDLT-1 Slave Mode Powered-Down			
					TONE = 0, Off		TONE = 1, On	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**
23	RE2/ BCLK	Output	BCLK = 128 kHz	BCLK = 0	BCLK = 128 kHz	BCLK = 128 kHz	BCLK = 128 kHz	BCLK = 128 kHz
24	Rx	Input	64 kbps Data In	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care
25	LO2	Output	Modulator Out	Modulator Out	LO2 = LO1	LO2 = LO1	LO2 = LO1	LO2 = LO1
26	LO1	Output	Modulator Out	Modulator Out	LO1 = LO2	LO1 = LO2	LO1 = LO2	LO1 = LO2
27	MASTER/ SLAVE	Input	1	1	1	1	1	1
28	V_{DD}	Power	+V	+V	+V	+V	+V	+V

MC145423 UDLT-3 PIN STATES FOR UDLT-1 MASTER MODE

MC145423			UDLT-1 Master Mode Powered-Up			UDLT-1 Master Mode Powered-Down	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**SE Low**	**Normal**	**SE Low**
1	V_{SS}	Power	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd
2	V_{ref}	Analog Ref	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$
3	LI	Input	Analog In	Don't Care	Analog In	Analog In	Analog In
4	$\overline{\text{LB}}$	Input	1	0	State Latched	Don't Care	Don't Care
5	VD	Output	Digital out	Digital out	High Impedance	Digital out	High Impedance
6	SDI1	Input	8 kbps Data In	8 kbps Data In	State Latched	8 kbps Data In	State Latched
7	SDI2	Input	8 kbps Data In	8 kbps Data In	State Latched	8 kbps Data In	State Latched
8	FRAME 10/20	Input	0	0	0	0	0
9	SDCLK	Don't Care	High Impedance	High Impedance	High Impedance	High Impedance	High Impedance
10	SDO1	Output	8 kbps Data Out	8 kbps Data Out	High Impedance	8 kbps Data Out	High Impedance
11	SDO2	Output	8 kbps Data Out	8 kbps Data Out	High Impedance	8 kbps Data Out	High Impedance
12	SE/(Mu/A)	Input	1	1	0	1	0
13	$\overline{\text{PD}}$	Input	1	1	State Latched	0	State Latched
14	MOD TRI/SQ	Input	0	0	0	0	0
15	Tx	Output	64 kbps Data Out	64 kbps Data Out	64 kbps Data Out	64 kbps Data Out	64 kbps Data Out
16	EN2-TE2/ SIE/B1B2	Input	SIE Digital In	SIE Digital In	SIE Digital In	SIE Digital In	SIE Digital In

MC145423 UDLT-3 PIN STATES FOR UDLT-1 MASTER MODE (continued)

MC145423			UDLT-1 Master Mode Powered-Up			UDLT-1 Master Mode Powered-Down	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**SE Low**	**Normal**	**SE Low**
17	EN1-TE1	Input	TE1 8 kHz	TE1 8 kHz	TE1 8 kHz	TE1 8 kHs	TE1 8 kHz
18	MSI/TONE	Input	MSI 8 kHz	MSI 8 kHz	MSI 8 kHz	MSI 8 kHz	MSI 8 kHz
19	CCI/ $XTAL_{in}$	Input	CCI 2.048 MHz	CCI 2.048 MHz	CCI 2.048 MHz	CCI 2.048 MHz	CCI 2.048 MHz
20	TDC-RDC/ $XTAL_{out}$	Input	TDC-RDC Data Clk	TDC-RDC Data Clk	TDC-RDC Data Clk	TDC-RDC Data Clk	TDC-RDC Data Clk
21	LI SENS/ 2.048 MHz	Input	Digital In LI Sensitivity	Digital In LI Sensitivity	Digital In LI Sensitivity	Digital In LI Sensitivity	Digital In LI Sensitivity
22	RE1/ CLKOUT	Input	RE1 8 kHz	RE1 8 kHz	RE1 8 kHz	RE1 8 kHz	RE1 8 kHz
23	RE2/ BCLK	Don't Care	High Impedance	High Impedance	High Impedance	High Impedance	High Impedance
24	Rx	Input	64 kbps Data In	64 kbps Data In	64 kbps Data In	Don't Care	Don't Care
25	LO2	Output	Modulator Out	LO2 = LO1	No Effect	LO2 = LO1	LO2 = LO1
26	LO1	Output	Modulator Out	LO1 = LO2	No Effect	LO1 = LO2	LO1 = LO2
27	MASTER/ SLAVE	Input	0	0	0	0	0
28	V_{DD}	Power	+V	+V	+V	+V	+V

MC145423 UDLT-3 PIN STATES FOR UDLT-2 SLAVE MODE

MC145423			UDLT-2 Slave Mode Powered-Up		UDLT-2 Slave Mode Powered-Down			
					TONE = 0, Off		TONE = 1, On	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**
1	V_{SS}	Power	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd
2	V_{ref}	Analog Ref	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$
3	LI	Input	Analog In	Analog In	Analog In	Analog In	Analog In	Analog In
4	$\overline{\text{LB}}$	Input	1	0	Don't Care	Don't Care	Don't Care	Don't Care
5	VD	Output	Digital Out	Digital Out	VD = 0	VD = 1	VD = 0	VD = 1
6	SDI1	Input	16 kbps Data In	16 kbps Data In	Don't Care	Don't Care	Don't Care	Don't Care
7	SDI2	Input	16 kbps Data In	16 kbps Data In	Don't Care	Don't Care	Don't Care	Don't Care
8	FRAME 10/20	Input	1	1	1	1	1	1
9	SDCLK	Output	16 kHz	16 kHz	16 kHz	16 kHz	16 kHz	16 kHz

MC145423 UDLT-3 PIN STATES FOR UDLT-2 SLAVE MODE (continued)

MC145423			UDLT-2 Slave Mode Powered-Up		UDLT-2 Slave Mode Powered-Down			
					TONE = 0, Off		TONE = 1, On	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**	**No Valid Burst Rec'd**	**Valid Burst Rec'd**
10	SDO1	Output	16 kbps Data Out	16 kbps Data Out	Data Not Changed	16 kbps Data Out	Data Not Changed	16 kbps Data Out
11	SDO2	Output	16 kbps Data Out	16 kbps Data Out	Data Not Changed	16 kbps Data Out	Data Not Changed	16 kbps Data Out
12	SE/ (Mu/A)	Input	1/0 Mu/A	1/0 Mu/A	1/0 Mu/A	1/0 Mu/A	1/0 Mu/A	1/0 Mu/A
13	$\overline{\text{PD}}$	I/O	1	1	0	0	0	0
14	MOD TRI/SQ	Input	1	1	1	1	1	1
15	Tx	Output	128 kbps Data Out*	128 kbps Data Out*	High Impedance	64 kbps Data Out	500 Hz Tone Out	500 Hz Tone Out
16	EN2-TE2/ SIE/B1B2	Output	EN2 8 kHz	EN2 8 kHz	EN2 = 0	EN2 = 0	EN2 8 kHz	EN2 8 kHz
17	EN1-TE1	Output	EN1 8 kHz	EN1 8 kHz	EN1 = 0	EN1 = 0	EN1 8 kHz	EN1 8 kHz
18	MSI/ TONE	Input	1/0 Tone	1/0 Tone	0 No Tone	0 No Tone	1 No Tone	1 Tone
19	CCI/ $XTAL_{in}$	Input	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz
20	TDC-RDC/ $XTAL_{out}$	Output	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz	XTAL 8.192 MHz
21	LI SENS/ 2.048 MHz	Output	2.048 MHz	2.048 MHz	2.048 MHz	2.048 MHz	2.048 MHz	2.048 MHz
22	RE1/ CLKOUT	Output	RE1 8 kHz	RE1 8 kHz	RE1 0	RE1 0	RE1 8 kHz	RE1 8 kHz
23	RE2/ BCLK	Output	BCLK 128 kHz	BCLK = 0	BCLK 128 kHz	BCLK 128 kHz	BCLK 128 kHz	BCLK 128 kHz
24	Rx	Input	128 kbps Data In	Don't Care	Don't Care	Don't Care	128 kbps Data In	128 kbps Data In
25	LO2	Output	Modulator Out	Modulator Out	LO2 = LO1	LO2 = LO1	LO2 = LO1	LO2 = LO1
26	LO1	Output	Modulator Out	Modulator Out	LO2 = LO1	LO2 = LO1	LO1 = LO2	LO1 = LO2
27	MASTER/ SLAVE	Input	1	1	1	1	1	1
28	V_{DD}	Power	+V	+V	+V	+V	+V	+V

* Tx is high impedance when TE1 and TE2 are both low, simultaneously.
Tx is undefined when TE1 and TE2 are both high, simultaneously.

MC145423 UDLT-3 PIN STATES FOR UDLT-2 MASTER MODE

MC145423			UDLT-2 Master Powered-Up			UDLT-2 Master Powered-Down	
Pin No.	**Pin Name**	**In/out**	**Normal**	**$\overline{\text{LB}}$ Low**	**SE Low**	**Normal**	**SE Low**
1	V_{SS}	Power	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd	Power Supply Gnd
2	V_{ref}	Analog Ref	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$	AGND $V_{DD}/2$
3	LI	Input	Analog In	Don't Care	Analog In	Analog In	Analog In
4	$\overline{\text{LB}}$	Input	1	0	State Latched	Don't Care	Don't Care
5	VD	Output	Digital Out	Digital Out	High Impedance	Digital Out	High Impedance
6	SDI1	Input	16 kbps Data In	16 kbps Data In	State Latched	16 kbps Data In	State Latched
7	SDI2	Input	16 kbps Data In	16 kbps Data In	State Latched	16 kbps Data In	State Latched
8	FRAME 10/ 20	Input	1	1	1	1	1
9	SDCLK	Input	16 kHz	16 kHz	16 kHz	16 kHz	16 kHz
10	SDO1	Output	16 kbps Data Out	16 kbps Data Out	High Impedance	16 kbps Data Out	High Impedance
11	SDO2	Output	16 kbps Data Out	16 kbps Data Out	High Impedance	16 kbps Data Out	High Impedance
12	SE/(Mu/A)	Input	1	1	0	1	0
13	$\overline{\text{PD}}$	Input	1	1	State Latched	0	State Latched
14	MOD TRI/SQ	Input	1	1	1	1	1
15	Tx	Output	128 kbps* Data Out	128 kbps* Data Out	128 kbps* Data Out	128 kbps* Data Out	128 kbps* Data Out
16	EN2-TE2/ SIE/B1B2	Input	TE2 8 kHz	TE2 8 kHz	TE2 8 kHz	TE2 8 kHz	TE2 8 kHz
17	EN1-TE1	Input	TE1 8 kHz	TE1 8 kHz	TE1 8 kHz	TE1 8 kHz	TE1 8 kHz
18	MSI/TONE	Input	8 kHz	8 kHz	8 kHz	8 kHz	8 kHz
19	CCI/$XTAL_{in}$	Input	CCI 4.096 MHz	CCI 4.096 MHz	CCI 4.096 MHz	CCI 4.096 MHz	CCI 4.096 MHz
20	TDC-RDC/ $XTAL_{out}$	Input	TDC-RDC Data Clk	TDC-RDC Data Clk	TDC-RDC Data Clk	TDC-RDC Data Clk	TDC-RDC Data Clk
21	LI SENS/ 2.048 MHz	Input	Digital In Sensitivity	Digital In Sensitivity	Digital In Sensitivity	Digital In Sensitivity	Digital In Sensitivity
22	RE1/ CLKOUT	Input	RE1 8 kHz	RE1 8 kHz	RE1 8 kHz	RE1 8 kHz	RE1 8 kHz
23	RE2/BCLK	Input	RE2 8 kHz	RE2 8 kHz	RE2 8 kHz	RE2 8 kHz	RE2 8 kHz
24	Rx	Input	128 kbps Data In	128 kbps Data In	128 kbps Data In	Don't Care	Don't Care
25	LO2	Output	Modulator Out	LO2 = LO1	No Effect	LO2 = LO1	LO2 = LO1
26	LO1	Output	Modulator Out	LO1 = LO2	No Effect	LO1 = LO2	LO1 = LO2
27	MASTER/ SLAVE	Input	0	0	0	0	0
28	V_{DD}	Power	+V	+V	+V	+V	+V

* Tx is high impedance when TE1 and TE2 are both low, simultaneously.
Tx is undefined when TE1 and TE2 are both high, simultaneously.

PIN DESCRIPTIONS

V_{SS}
Negative Supply (Pin 1)

This is the most negative power pin, and should be tied to system ground (0 V).

V_{ref}
Voltage Reference Output (Pin 2)

This is the output from the internal reference supply (mid-supply) and should be bypassed to both V_{SS} and V_{DD} with 0.1 μF capacitors. This pin usually serves as an analog ground reference for transformer coupling of the device's incoming bursts from the line. No external load should be placed on this pin.

LI
Line Input (Pin 3)

This pin is the input to the demodulator for the incoming bursts. This input has an internal 240 kΩ resistor tied to the V_{ref} pin, so an external capacitor or line transformer may be used to couple the input signal to the device with no dc offset.

$\overline{LB}$
Loopback Low Input (Pin 4)

Master Mode: A low on this pin ties the internal modulator output to the internal demodulator input, which loops the entire burst for testing purposes. During the loopback operation, the LI input is ignored, and the LO1 and LO2 outputs are driven to equal voltages. The state of the $\overline{LB}$ pin is internally latched if the SE pin is held low. This feature is only active when the $\overline{PD}$ input is high.

Slave Mode: When this pin is low and $\overline{PD}$ is high, the incoming B channels from the master are burst back to the master, instead of the Rx B channel input data. The SDI1 and SDI2 functions operate normally in this mode, and the BCLK (pin 23) is held low. Additionally, for both the UDLT-1 and UDLT-2 mode, when the TONE (pin 18) and loopback functions are active simultaneously, the loopback function overrides the TONE function.

VD
Valid Data Output (Pin 5)

A high level on this pin indicates that a valid line transmission has been demodulated. A valid line transmission burst is determined by proper synchronization and the absence of detected bit errors. VD is a CMOS output and is high impedance when SE is low.

Master Mode: VD changes state on the rising edge of MSI, when $\overline{PD}$ is high. When $\overline{PD}$ is low, VD changes state at the end of demodulation of a transmission burst and does not change again until three MSI rising edges have occurred, at which time it goes low, or until the next demodulation of a burst.

Slave Mode: If no transmissions from the master have been received within the last 250 μs, as determined by an internal oscillator, VD will go low.

SDI1 and SDI2
D Channel Signaling Data Bit Inputs 1 and 2 (Pins 6 and 7)

Master Mode (UDLT-1): These inputs are the 8 kbps serial data inputs in UDLT-1 mode. Data on these pins is loaded on the rising edge of MSI for transmission to the slave. The state of these pins is latched if SE is held low.

Slave Mode (UDLT-1): These inputs are the 8 kbps serial data inputs in UDLT-1 mode. Data on these pins is loaded on the rising edge of TE1 for transmission to the master. If no transmissions from the master are being received and $\overline{PD}$ is high, data on these pins will be loaded into the part on an internal signal. Therefore, data on these pins should be steady until synchronous communication with the master has been established, as indicated by the high on VD.

Master Mode (UDLT-2): These inputs are the 16 kbps serial data inputs in UDLT-2 mode. Two bits should be clocked into each of these inputs between the rising edges of the MSI frame reference clock. The first bit of each D channel is clocked into an intermediate buffer on the first falling edge of the SDCLK following the rising edge of MSI. The second bit of each D channel is clocked in on the next negative transition of the SDCLK. If further SDCLK negative edges occur, new information is serially clocked into the buffer replacing the previous data, one bit at a time. Buffered D channel bits are burst to the slave on the next rising edge of the MSI frame reference clock. The state of these pins is latched if SE is held low.

Slave Mode (UDLT-2): These inputs are the 16 kbps serial data inputs in UDLT-2 mode. The D channel data bits are clocked in serially on the negative edge of the 16 kbps SDCLK output pin.

FRAME 10/20
(Pin 8)

The UDLT series of transceivers are designed to operate using a ping-pong transmission scheme with an 8 kHz burst rate. Each frame the master device "pings" a burst of data to the slave, which responds with a "pong" burst of data. This pin selects whether this 8 kHz frame will have a 10-bit data burst for UDLT-1 compatibility or a 20-bit data burst for UDLT-2 compatibility.

A logic low (0 V) selects the UDLT-1 (MC145422/MC145426) mode. This sets the device to operate with one 64 kbps voice/data channel and two 8 kbps signaling channels. A logic high (V_{DD}) on this pin selects the UDLT-2 (MC145421/MC145425) mode. This sets the device to operate with two 64 kbps channels and two 16 kbps channels (2B+2D).

SDCLK
D Channel Signaling Data Clock Input (Pin 9)

Master Mode (UDLT-2): This is the transmit and receive data clock input for both D channels. See SDO1 and SDO2 pin descriptions for more information.

Master Mode (UDLT-1): High impedance.

Slave Mode (UDLT-2): This is the transmit and receive data clock output for both D channels. It starts on demodulation of a burst from the master device. This signal is rising-edge aligned with the EN1 and BCLK signals. After the demodulation of a burst, the SDCLK line completes two cycles and then remains low until the next burst from the master is demodulated. In this manner, synchronization with the master is established and any clock slip between master and slave is absorbed each frame.

Slave Mode (UDLT-1): This pin outputs 8 kHz equivalent to TE1.

SDO1 and SDO2
D Channel Signaling Data Outputs 1 and 2 (Pins 10 and 11)

Master Mode (UDLT-2): These serial outputs provide the 16 kbps D channel signaling information from the incoming burst. Two data bits should be clocked out of each of these two outputs between the rising edges of the MSI frame reference clock. The rising edge of MSI produces the first bit of each D channel on its respective pin. Circuitry then searches for a negative D channel clock edge. This tells the D channel data shift register to produce the second D channel bit on the next rising edge of the SDCLK. Further rising edges of the SDCLK recirculate the D channel output buffer information.

Master Mode (UDLT-1): These outputs are received signaling bits from the slave UDLT and change state on the rising edge of MSI, if $\overline{PD}$ is high; or at the end of demodulation, if $\overline{PD}$ is low.

Slave Mode (UDLT-2): These two pins are the outputs for the 16 kbps D channels. These pins are updated on the rising edges of the slave SDCLK output pin.

Slave Mode (UDLT-1): These outputs are received signaling bits from the master UDLT and change state on the rising edge of TE1.

SE/(Mu/A)
Signaling Enable Input or Tone Format Input (Pin 12)

Master Mode (SE): A low on this pin causes the state of $\overline{LB}$, $\overline{PD}$, SDI1, and SDI2 to be stored. Additionally, output pins VD, SDO1, and SDO2 will be high impedance. This allows the device to be bussed with other UDLTs using a common control bus. A high on this pin returns the device to normal operation.

Slave Mode (Mu/A): This pin allows the user to select the PCM code format for the pacifier tone. A high on this pin selects Mu-Law. A low on this pin selects A-Law. The state of this pin determines the PCM code sequence for the 500 Hz square wave tone generated when the TONE pin input is high.

$\overline{PD}$
Power Down Low (Pin 13)

Master Mode: When this pin is held low, the device powers down, except for the circuitry necessary to demodulate an incoming burst and to output VD and the B and D channel data bits. When this pin is brought high, the device waits for three positive MSI edges or until the end of an incoming transmission from the slave and then begins transmitting every MSI period to the slave UDLT on the next rising edge of MSI.

Slave Mode: This is a bidirectional pin with a weak output driver that can be externally overdriven. When this pin is floating and a burst from the master is demodulated, the weak output drivers will try to force $\overline{PD}$ high. The drivers will try to force $\overline{PD}$ low, if

250 µs have elapsed without a burst from the master being successfully demodulated. This allows the slave device to self power-up and power-down in demand powered loop systems. When held low, the device powers down and the only active circuitry, is that which is necessary for the demodulation of data. When held high, the device is powered up and transmits normally in response to received bursts from the master.

MOD TRI/SQ
Modulation Select (Pin 14)

A logic low (0 V) on this pin selects the MDPSK modulation which has a slew controlled voltage output for reduced EMI/RFI. This output looks like a triangle waveform that is modulated with different angles for the peaks. A logic high (V_{DD}) on this pin, selects square wave output for maximum power to the line.

Tx
Transmit Data Output (Pin 15)

Master Mode (UDLT-1): This pin is high impedance when TE1 is low. When TE1 is high, this pin presents new 8-bit B channel data on rising edges of TDC-RDC.

Slave Mode (UDLT-1): B channel data is output on this pin on the rising edge of BCLK, while TE1 is high. This pin is high impedance when TE1 is low.

Master Mode (UDLT-2): This pin is high impedance when both TE1 and TE2 are low. This pin serves as an output for B channel information received from the slave device. The B channel data is under control of TE1 and TE2 and TDC-RDC.

Slave Mode (UDLT-2): This pin is an output for the B channel data received from the master.
B channel 1 data is output on the first eight cycles of the BCLK output when EN1 is high. B channel 2 data is output on the next eight cycles of the BCLK, when EN2 is high. B channel data bits are clocked out on the rising edge of the BCLK output pin.

EN2-TE2/SIE/B1B2
B Channel 2 Enable Output or
Signal Insert Enable (Pin 16)

Master Mode (SIE UDLT-1): In this mode, this pin functions as SIE. When held high, this pin causes signal bit 2, as received from the slave, to be inserted into the LSB of the outgoing PCM word at the Tx pin. The SDI2 pin will be ignored, and in its place, the LSB of the incoming word at the Rx pin will be transmitted to the slave. The PCM word to the slave will have LSB forced low in this mode. In this manner, signal bit 2 to/from the slave UDLT is inserted into the PCM words the master sends and receives from the backplane, for routing through the PABX for simultaneous voice/data communication. The state of this pin is internally latched if the SE pin is brought and held low.

Slave Mode (UDLT-1): In this mode, this pin is an input and selects the timeslot used for transferring the receive data word. When this pin is low, the device uses the RE1 pin timing the same as the MC145426 UDLT-1 slave. When this pin is a logic 1, the receive word is latched in during the TE1 timeslot, simultaneously with the transmit word transfer. The RE1 pin timing is not affected by this selection.

Master Mode (EN2-TE2 UDLT-2): In this mode, this pin functions as EN2-TE2. This pin, along with TE1 pin-17 control the output of data for their respective B-channel on the Tx output pin. When both TE1 and TE2 are low, the Tx pin is high impedance. The rising edge of the respective enable produces the first bit of the selected B-channel data on the Tx pin. Internal circuitry then scans for the next negative transition of the TDC-RDC clock. Following this event, the next seven bits of the selected B-channel data are output on the next seven rising edges of the TDC-RDC data clock. When TE1 and TE2 are high simultaneously, data on the Tx pin is undefined. TE1 and TE2 should be approximately leading-edge aligned with the TDC-RDC data clock. To keep the Tx pin out of the high impedance state, these enable lines should be high while the respective B channel data is being output.

Slave Mode (EN2-TE2 UDLT-2): Functioning as EN2-TE2, this pin is an output and serves as an 8 kHz enable signal for the input and output of the B channel 2 data. While EN2 is high, B channel 2 data is clocked out on the Tx pin on the eight rising edges of the BCLK. During this same time, B channel 2 input data is clocked in on the Rx pin, on the eight falling edges of the BCLK.

EN1-TE1
B Channel 1 Enable Output (Pin 17)

This pin is the logical inverse of EN2-TE2, and serves to control B channel 1 data. See the above pin description for more information. EN1 serves as the slave device's 8 kHz frame reference signal. The VD

pin is also updated on the rising edge of the EN1 signal.

MSI/TONE
Master Sync Input or Tone Enable Input (Pin 18)

Master Mode (MSI): This pin is the master 8 kHz frame reference input. The rising edge of MSI loads B and D channel data, which had been input during the previous frame, into the modulator section of the device, and initiates the outbound burst onto the twisted pair cable. The rising edge of MSI also initiates the buffering of the B and D channel data demodulated during the previous frame. MSI should be approximately leading edge aligned with the TDC-RDC data clock input signal.

Slave Mode (TONE): A high on this pin causes a 500 Hz square wave PCM tone to be inserted in place of the demodulated data. This feature allows the designer to provide audio feedback for telset keyboard depressions.

CCI/$XTAL_{in}$
Convert Clock Input or Crystal Input (Pin 19)

Master Mode (CCI UDLT-1): A 2.048 MHz clock signal should be applied to this pin. This signal is used for internal sequencing and control. This signal should be frequency and phase coherent with MSI for optimum performance.

Slave Mode ($XTAL_{in}$ UDLT-1): A 4.096 MHz crystal is tied between this pin and $XTAL_{out}$ (pin 20). A 10 MΩ resistor across this pin and $XTAL_{out}$ and 25 pF capacitors from this pin and $XTAL_{out}$ to V_{SS} are required for stability and to ensure start-up. This pin may be driven from an external source. $XTAL_{out}$ should be left open if an external signal is used on this input.

Master Mode (CCI UDLT-2): An 8.192 MHz clock should be supplied to this input. The 8.192 MHz input should be 50% duty cycle. This signal may free run with respect to all other clocks without performance degradation.

Slave Mode ($XTAL_{in}$ UDLT-2): Normally, an 8.192 MHz crystal is tied between this pin and the $XTAL_{out}$ (pin 20). A 10 MΩ resistor between $XTAL_{in}$ and $XTAL_{out}$ and 25 pF capacitors from $XTAL_{in}$ and $XTAL_{out}$ to V_{SS} are required to ensure stability and start-up. $XTAL_{in}$ may also be driven with an external 8.192 MHz signal if a crystal is not desired. $XTAL_{out}$ should be left open if an external signal is used on this input.

TDC-RDC/$Xtal_{out}$
Transmit and Receive Data Clock or Crystal Output (Pin 20)

Master Mode (TDC-RDC): This input is the transmit and receive data clock for the B channel data. Output data changes state on the rising edge of this signal, and input data is read on the falling edges of this signal. TDC-RDC should be roughly leading edge aligned with MSI.

Slave Mode ($XTAL_{out}$): This pin is the crystal out pin. It is capable of driving one external CMOS input and 15 pF of additional capacitance. See pin description for $XTAL_{in}$ (pin 19).

LI SENS/2.048 MHz
Line Input Sensitivity or 2.048 MHz Output (Pin 21)

Master Mode: By applying a logic 1 on this pin, the sensitivity of LI is reduced by 15 dB. This reduces the effects of crosstalk, and false detects that would be picked up and demodulated when the LI pin is connected to an open loop.

Slave Mode: This pin outputs a 2.048 MHz signal for use with a PCM codec-filter. All other device clocks are generated from the rising edge of this clock. The 8 kHz enables are derived by dividing this 2.048 MHz clock by a nominal ratio of 256. Phase synchronization to the master UDLT's burst is achieved by dividing this clock by the ratios of either 255, 256, or 257.

RE1/CLKOUT
Receive Data Enable 1 Input or Clock Output (Pin 22)

Master Mode (RE1 UDLT-1): A rising edge on this pin will enable data on the Rx pin to be loaded into the receive data register on the next eight falling edges of the TDC-RDC data clock. RE1 and TDC-RDC should be approximately leading edge aligned.

Slave Mode (RE1 UDLT-1): This B series CMOS output is the inverse of TE1 (see TE1 pin description).

Master Mode (RE1 UDLT-2): This input along with RE2 (pin 23) control the input of B channel data on the Rx pin. The rising edge of the respective enable signal causes the device to load the selected receive

data buffer with data from the Rx pin on the next eight falling edges of the TDC-RDC clock. The RE1 and RE2 enables should be roughly leading edge aligned with the TDC-RDC data clock. These enables are rising edge sensitive and need not be high for the entire B channel input period.

Slave Mode (CLKOUT UDLT-2): This pin serves as a buffered output of the crystal frequency divided by two.

RE2/BCLK
Receive Data Enable Input 2 or B Channel Data Clock Output (Pin 23)

Master Mode (UDLT-1): This pin is high impedance.

Master Mode (RE2 UDLT-2): See pin description for RE1 (pin 22).

Slave Mode (BCLK UDLT-1 and UDLT-2): This output provides the data clock for the telset codec-filter. This clock signal is 128 kHz and begins operating upon the successful demodulation of a burst from the master. At this time, EN1-TE1 goes high and BCLK starts toggling. BCLK remains active for 16 periods, at the end of which time it remains low until another burst is received from the master. In this manner, synchronization between the master and slave is established and any clock slippage is absorbed each frame. If TONE (pin 18) is brought high, then EN1-TE1/RE1 are generated from an internal oscillator until TONE is brought low, or an incoming burst from the master is received. BCLK is disabled when $\overline{LB}$ is held low.

Rx
Receive Data Input (Pin 24)

Master Mode (UDLT-1): The 8-bit B channel data is clocked into the device on this pin, on the falling edges of TDC-RDC, under the control of RE1.

Slave Mode (UDLT-1): The 8-bit B channel data from the telset PCM codec-filter is input on this pin on the eight falling edges of BCLK after RE1 goes high, when EN2-TE2/SIE/B1B2, pin 16 is low. When EN2-TE2/SIE/B1B2, pin16 is high, the receive data word is latched in during the high period of EN1-TE1, pin 17 which is simultaneous with the transfer of the transmit word. See the pin descriptions for EN2-TE2/SIE/B1B2 and EN1-TE2 for more information.

Master Mode (UDLT-2): B channel data is input on this pin and controlled by the RE1, RE2, and TDC-RDC pins.

Slave Mode (UDLT-2): This pin is an input for the B channel data. B channel 1 data is clocked in on the first eight falling edges of the BCLK output following the rising edge of the EN1 output. B channel 2 data is clocked in on the next eight falling edges of the BCLK following the rising edge of the EN2 output.

LO2
Line Drive Output (Pin 25)

The LO2 pin, along with LO1 (pin 26) form a push-pull output, to drive the twisted pair transmission line. The UDLT-1 drives the twisted pair with a 10-bit, 256 kHz modified DPSK (MDPSK) burst, or a square wave (set by pin 14 MOD TRI/SQ) burst, each 125 µs. The UDLT-2 drives the twisted pair with a 20-bit 512 kHz modulated burst. When these pins are idle and set for square wave modulation, they rest at the positive power supply voltage. When these pins are idle and set for MDPSK, they rest at V_{ref}. For power supply voltages less than 4.5 V, squarewave modulation must be used.

LO1
Line Driver Output (Pin 26)

See the pin description for LO2 (pin 25).

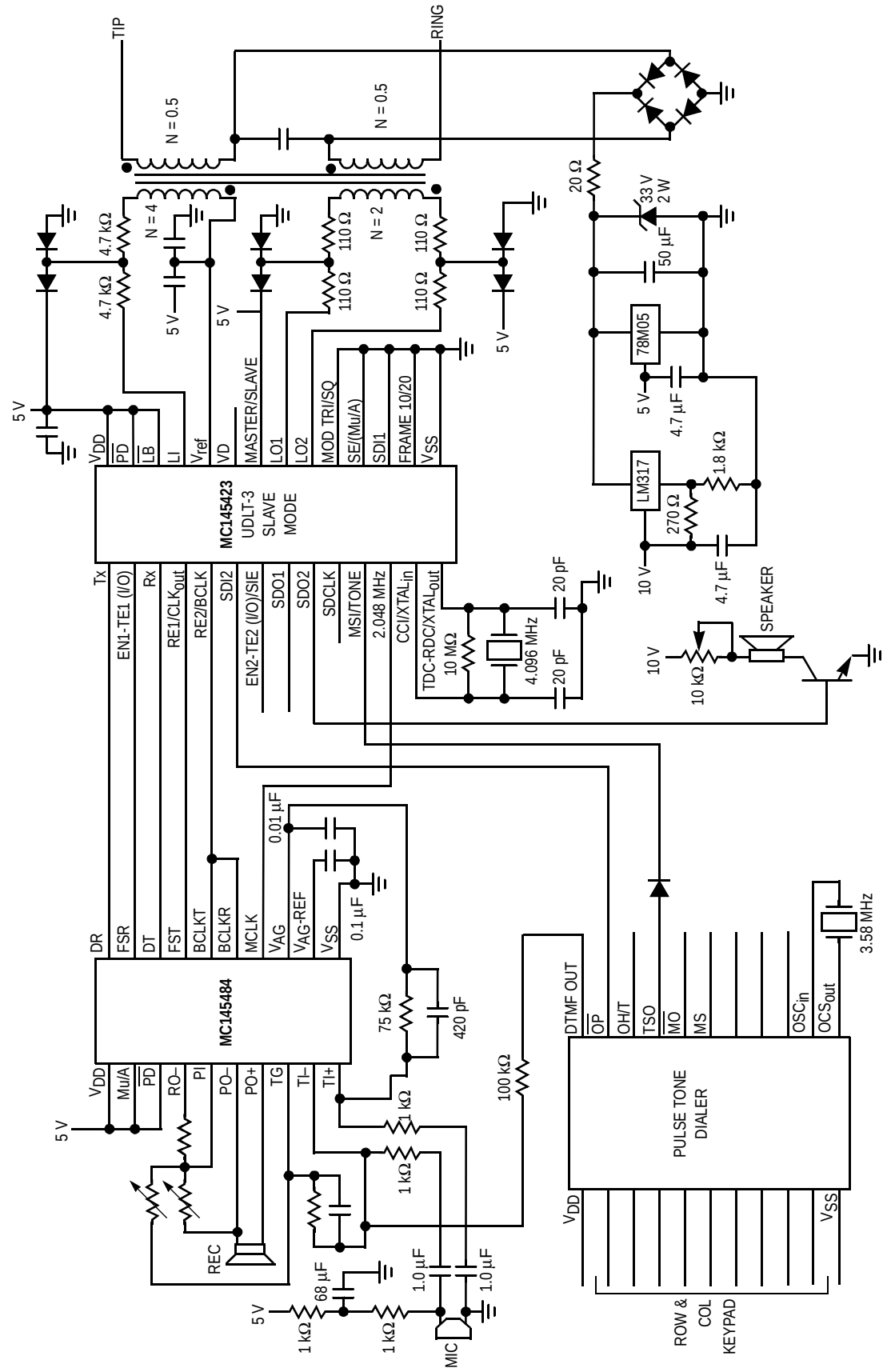
MASTER/SLAVE
Master/Slave Mode (Pin 27)

A logic low (0 V) on this pin selects master and a logic high (V_{DD}) selects slave.

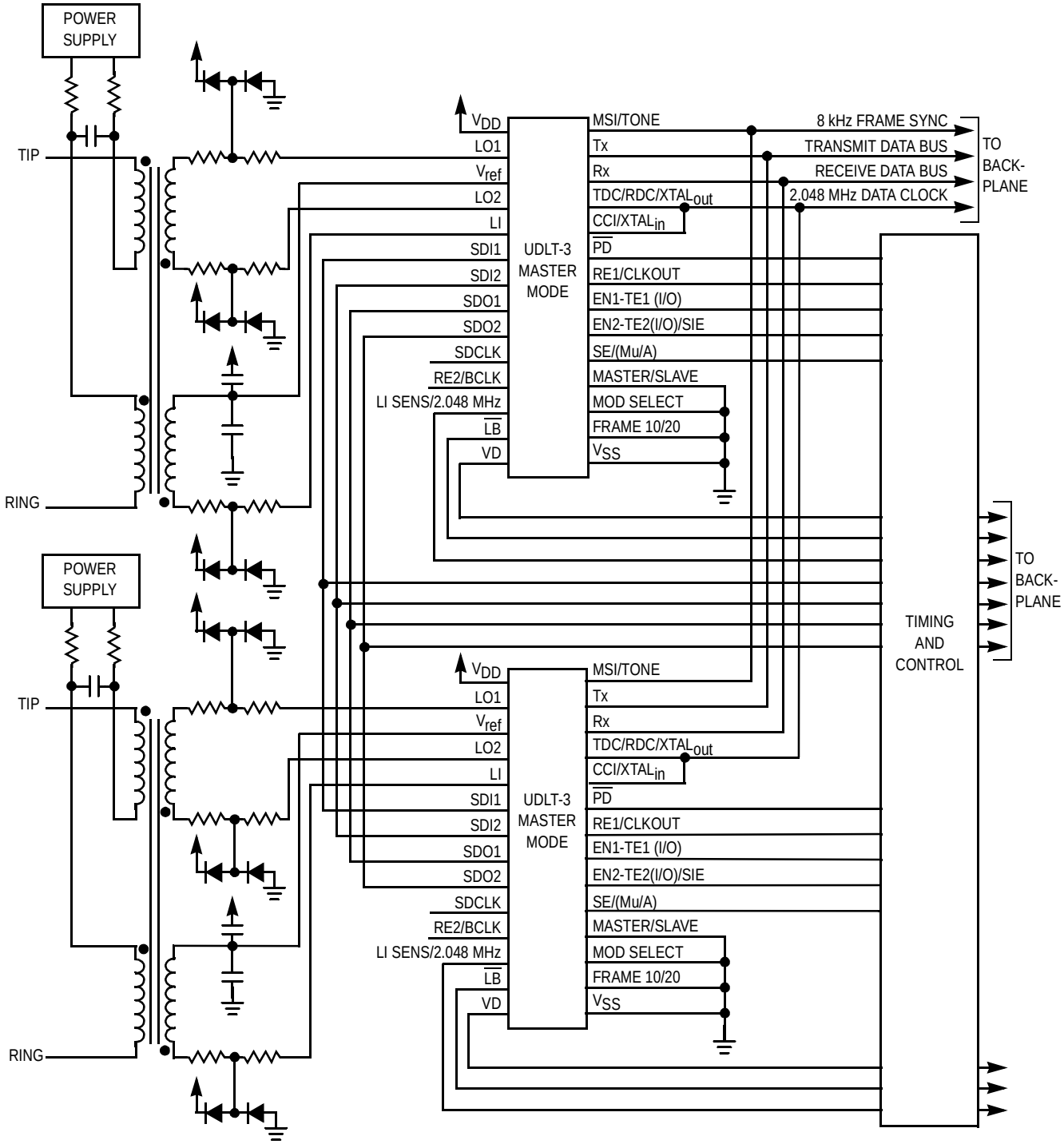
V_{DD}
Positive Supply (Pin 28)

This is the most positive power supply pin. Acceptable operating voltages are from 4.5 V to 5.5 V.

BASIC DIGITAL TELSET

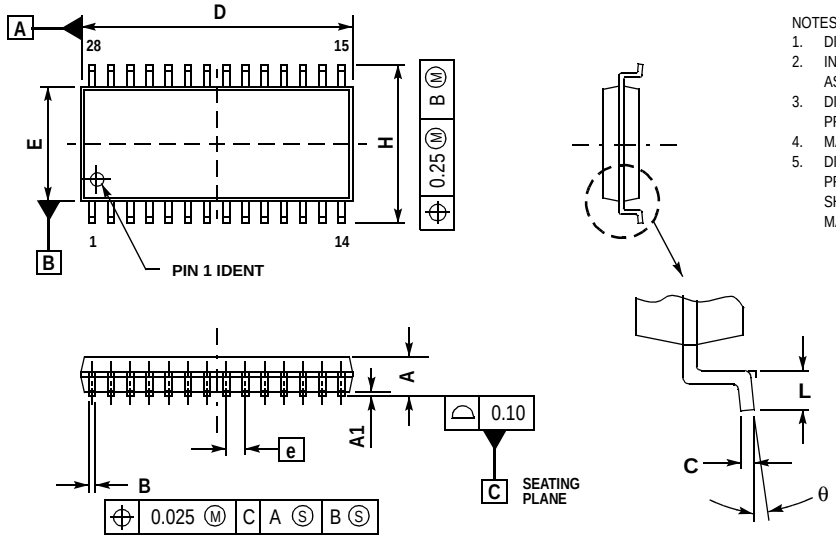


MULTICHANNEL DIGITAL LINE CARD



PACKAGE DIMENSIONS

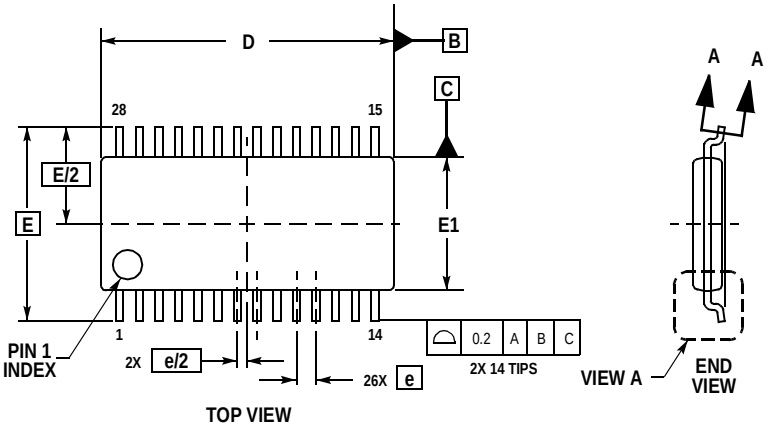
DW SUFFIX
SOIC PACKAGE
CASE 751F-05



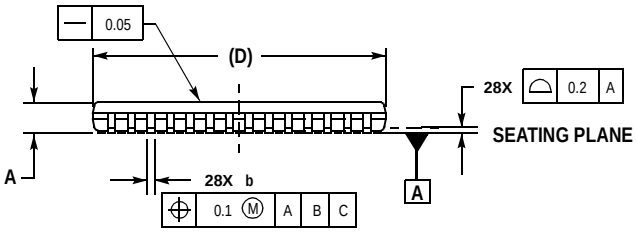
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

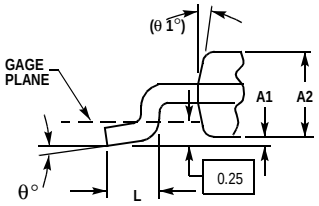
DT SUFFIX
TSSOP PACKAGE
CASE 1168-01



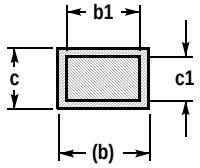
TOP VIEW



SIDE VIEW



VIEW A



SECTION A-A

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.
4. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR MOLD PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.38.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	9.60	9.80
e	0.65 BSC	
E	6.40 BSC	
E1	4.30	4.50
L	0.50	0.70
θ	0°	8°
θ1	14° REF	

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