MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33285

Product Preview

Automotive Dual High Side TMOS Driver

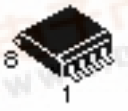
HIGH SIDE TMOS DRIVER
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC33285 is a dual high side TMOS driver designed for use in the harsh automotive switching applications.

The purpose of the MC33285 is to drive two power n-channel FETs in a high side application with an inductive load. The application in an automotive environment requires the capability of withstanding high voltages and load dump transients. The MC33285 is able to withstand reverse battery conditions at selected pins.

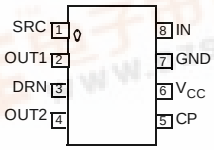
It protects the n-channel power FET on OUT1 under over current condition. This device has one input to control both stages on or off.

- Temperature Range from -40°C to +125°C
- PWM Capability
- Power TMOS # 1 Over-Current and Short-Circuit Protection
- Voltage Range 7V to 40V
- Extended Temperature Range from -40°C to 125°C
- Load Dump Protected
- Over Voltage Detection and Activation of OUT2 during Overvoltage
- Single Input Control for both Output Stages
- Capacitor Value of 100nF Connected to Pin CP
- Analog Input Control Measurement Detection
- OUT1 LOAD leakage measurement detection



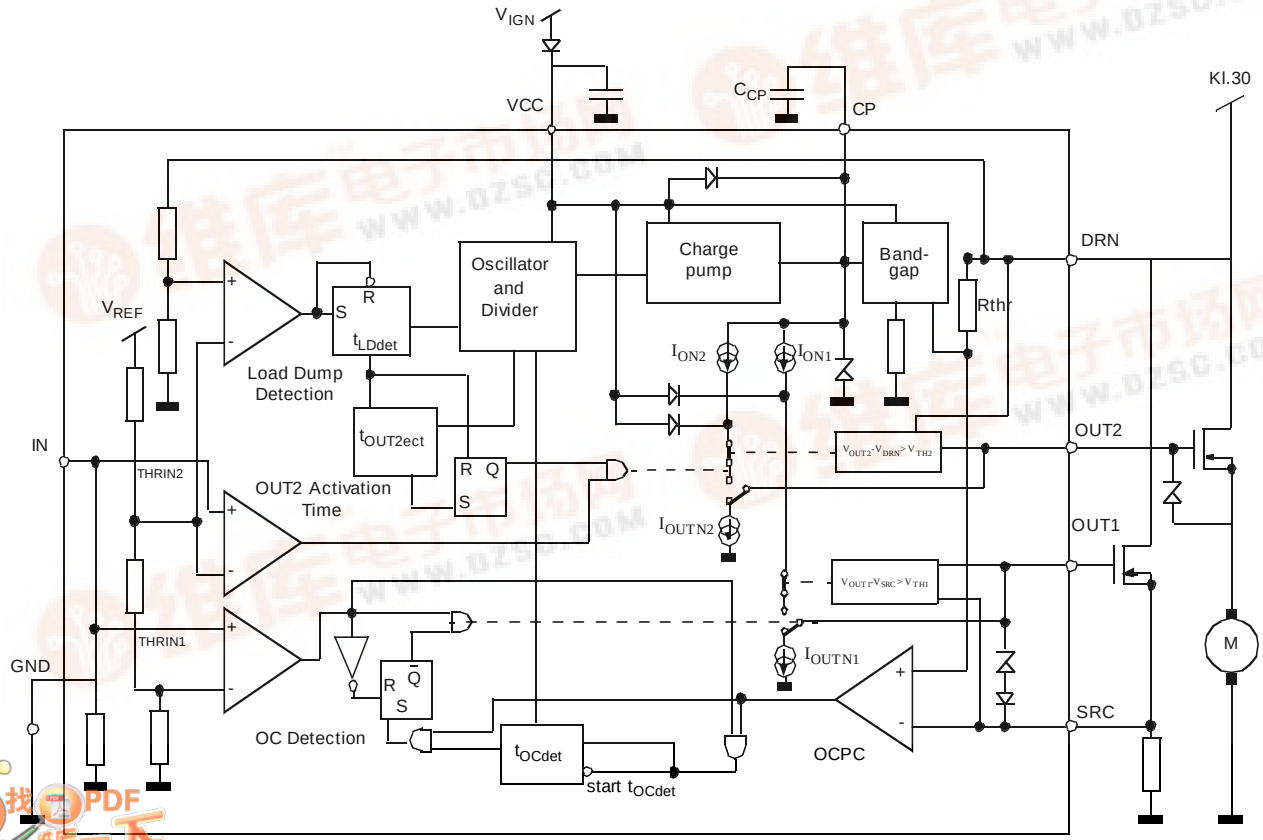
D SUFFIX
PLASTIC PACKAGE
CASE 751-02
SO-8

PIN CONNECTIONS



ORDERING INFORMATION		
Device	Temperature Range	Package
MC33285D	-40°C to +125°C	SO8

Block Diagram And Typical Application



MAXIMUM RATING

Rating	Symbol	Value	Unit
Maximum voltage at pins OUT1 OUT2	V_{OUT}	V_{VCC} + 20	V
Maximum voltage at pin CP	V_{CP}	50	V
Input voltage V_i at DRN	V_{DRN}	-2 ; 40	V
Input voltage V_i at SRC	V_{SRC}	-5 ; 40	V
Input voltage at pin V_{CC}	V_{CC}	-2 to 40	V
Input Voltage at pin IN. Condition : -2V<V_{VCC}<40V	V_{IN}	-2 to V_{VCC}	V
Operational voltage V_{VCC} at pin V_{CC}	V_{VCC}	7 to V_i	V

THERMAL RATINGS

Rating	Symbol	Value	Unit
Storage Temperature	T_{stg}	-40 to +150	°C
Operating ambient temperature	T_a	-40 to +125	°C

ELECTRICAL CHARACTERISTICS. (T_A from -40°C to +125°C, Vcc from 7V to 20V, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OVERVOLTAGE AND OVERCURRENT					
Load Dump Detection Time	tLD_{det}	250	400	550	µs
Load Dump Activation Time	tOUT2act	300	460	620	ms
Error Voltage Threshold	VDRN - VSRC	1.12		1.44	V
Overcurrent Detection Time	tOCdet	520	800	1080	µs
SRC PIN 1					
Leakage Current	ILC_{det}	15	30	50	mA
Leakage Current Detection Time	tLC_{det}	130	200	270	µs
DRN PIN 3					
Operating Current (7V<V_{DRN}<20V)	I_{DRN}			1.5	mA
Leakage current (0V<V_{DRN}<20V, V_{VCC}<4V)	I_{leak_DRN}	-5		5	µA
OUT1 PIN2, OUT 2 PIN 4					
Output On Voltage. Charge Pump ON	Von			Vcc+15	V
Turn off current, Vout >0.5V	Ioutoff	66	110	154	µA
Turn On Time, OUT1: 8nF,10µA ; OUT2: 16nF,10µA - 7V < Vcc < 10V, Vout > Vcc+7 - 10V < Vcc < 20V, Vout > Vcc+11	ton			 1.5 1.5	ms
VCC PIN 6					
Supply Voltage Range	Vcc	7		40	V
Quiescent Supply Current at Vcc = 20V	Icc			10	mA
IN PIN 8					
Input Low Voltage OUT1	Vil			0.7	V
Input High Voltage OUT1	Vih	1.7			V
Input Hysteresis OUT1, OUT2	Vhys	0.4			V
Input Pull Down Current, 0.7V<Vin<6V	Iin	7.5	15	16.5	µA
Open Input Voltage	Viop			0.7	V
Input Low Voltage OUT2	Vil2			3	V
Input High Voltage OUT2	Vih2	3.9			V

Turn On Characteristics

The power FETs are turned on by charging their gate capacities with a current flowing out of pin OUT1 and OUT2. During PWM, the values of table below are guaranteed. They are measured with 8nF on OUT1 and 16nF on OUT2.

- test condition : V_{IN} : ramp 0V to 2.5V or 2.5V to 5V.

Figure 1. Turn-on Behaviour

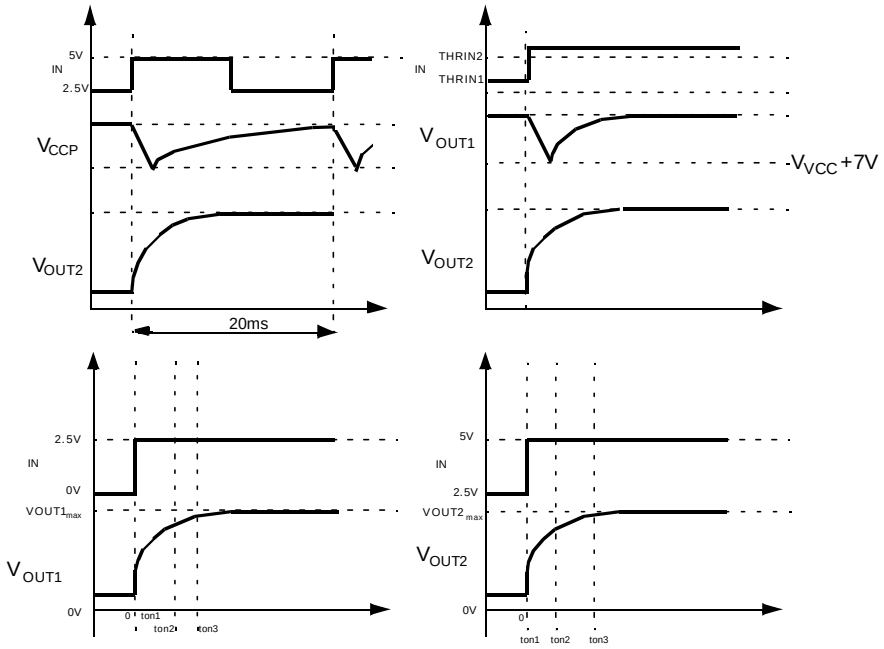


Table 1 Turn on behaviour

Voltage V_{VCC}	**Minimum $V_{OUT1,OUT2}$ after t_{on1} = 100µsec**	**Minimum $V_{OUT1,OUT2}$ after t_{on2} = 1.0msec**	**Minimum $V_{OUT1,OUT2}$ after t_{on3} = 1.5msec**
$7V < V_{VCC} < 10V$	V_{VCC} - 0.7V	V_{VCC} + 5.95V	V_{VCC} + 7V
$10V < V_{VCC} < 20V$	V_{VCC} - 0.7V	V_{VCC} + 9.35V	V_{VCC} + 11V
$20V < V_{VCC} < 40V$	V_{VCC} - 0.7V		

The output voltages at OUT1 and OUT2 are limited by controlling the current sources I_{on1}, I_{on2} to avoid currrent flowing through the external or the internal zener diode .

If Vcc + Vth (threshold voltage) is reached , the current sources are turned off.

- threshold V_{TH1} for OUT1 output voltage control : $7V < V_{TH1} < Vz$
- threshold VTH2 for OUT2 output voltage control : $7V < V_{TH2} < 15V$

Turn off characteristics

The power FETs on OUT1 and OUT2 are turned off by discharging the gate capacity with the constant discharge current I_{OUToff} .

- discharge current $I_{OUTxoff}$: IOUTxoff = 110µA

condition : $V_{OUT}x > 0.5V$ ($V_{IN} < V_{THRxIN}$)

Test conditions for switching off the power FETs :

- 1. IN open
- 2. Stages disabled via pin IN
- 3. Stage OUT1 disabled by an over current error

FUNCTIONNAL DESCRIPTION

Introduction

The MC33285 contains only one charge pump for two outputs.The outputs OUT1 and OUT2 are switched on and off by the input IN .There are three ways to control the outputs: OUt1 can be switched alone , they can be switched together or OUT2 can be switched when OUT1 is already on .In the last case , the voltage drop on OUT1 when charging OUT2 is limited .

The external capacitor C_{CP} connected to pin CP is used to store the charge continuously delivered by the charge pump . The voltage on this pin is limited to a maximum value V_{CPmax} . Both outputs are sourced with a constant current from C_{CP} to switch them on . In addition , the gates of the power FETs are precharged from VCC to prevent C_{CP} from being discharged by a voltage on OUT1 or OUT2 which is still lower than V_{VCC}.The values of the output voltages are limited to $V_{OUT1max}$ and $V_{OUT2max}$

The power FET on OUT1 is protected againts an exceeded gate-source voltage by an internal zener diode.

Channel 1 allows to protect the n-channel power FET on OUT1 under over current condition. The drain-source voltage of the FET on OUT1 will be checked, if the channel 1 is switched on. The internal error voltage threshold determines the maximum drain-source voltage that allows the power FET to stay in the on state. If the measured drain-source voltage exceeds the internal error voltage threshold, the output of the Over Current Protection Comparator (OCPC) is enabled. If the output of the OCPC is active longer than t_{OCdet} , the output OUT1 is switched off .

After switching off the power FET on OUT1 by an over current condition, the power FET can only be turned on again by the input IN.

When switching off the power FETs their gate capacities are discharged by a constant currennt I_{OUToff}

IF the input IN is disconnected, the MC33285 outputs OUT1 and OUT2 are in the off state.

If overvoltage occurs on pin DRN for a time period longer than t_{LDdet} , then OUT2 is switched on for the time $t_{OUT2act}$. In overvoltage condition OUT1 is off if IN is below Vih.

Internal Zener Diode

An on-chip zener diode is placed between OUT1 and SRC. Design guarantees that $V_Z > V_{TH1}$

- zener clamping voltage between OUT1 and SRC :

$V_{TH1} < V_Z < 20V$

PWM capability

The CPIC2 is PWM capable on OUT2. The loss of charge on Ccp when switching on OUT2 is refreshed until the start on the next PWM cycle to a value which is sufficient to guarantee the specified turn on behaviour.

The PWM capability is measured with a test circuit and load conditions

- PWM cycle : period T = 20ms ; OUT2 is switched on from 10% to 90% of T .

- Test condition : V_{IN} : ramps 2.5V to 5V according to PWM cycle defined above.

Crosstalk between OUT1 and OUT2

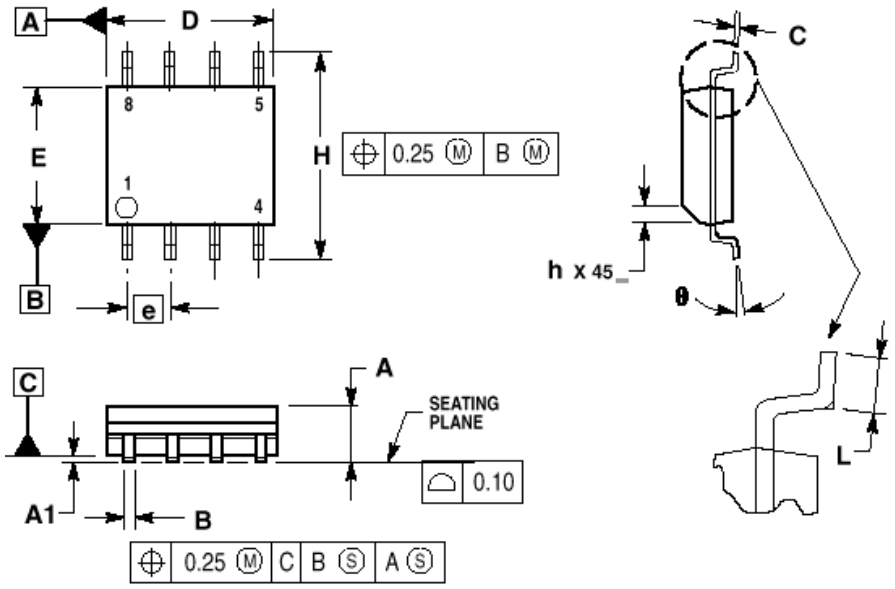
If output OUT2 is switched on while OUT1 is already on, the voltage drop that occurs on OUT1 is limited.

Voltage drop on OUT1 :

$10V < V_{VCC} < 20V$: OUT1 not below $V_{VCC} + 7V$

$7V < V_{VCC} < 20V$: OUT1 not below $V_{VCC} + 7V$

Each time OUT1 is switched on, a current ILCdet is sourced out of pin SRC for the time tLCdet to check if there is an external leakage current on that node in the application. The high side switch on OUT1 is turned on only if the test is successful."



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0_	7_