MOTOROLA
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Rev 2, 08/2002

Preliminary Information

6.0 A H-Bridge with Enable

33887

6.0 A H-BRIDGE WITH ENABLE

The 33887 is a monolithic H-Bridge with a Sleep Mode feature ideal for fractional horsepower DC-motor and bi-directional thrust solenoid control. The IC incorporates internal control logic, charge pump, gate drive, and low $R_{DS(ON)}$ MOSFET output circuitry. The 33887 is able to control continuous inductive DC load currents of 6.0 A. Output loads can be Pulse Width Modulation (PWM) controlled at frequencies to 10 kHz. An internal output current monitoring circuit provides a proportional (1/375th) feedback current output for the microcontroller to monitor the output current and provide closed-loop control.

A Fault Status output reports undervoltage, overcurrent, and overtemperature conditions. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two disable inputs force the H-Bridge outputs to tristate (exhibit high impedance).

The 33887 is parametrically specified over a temperature range of -40°C ≤ T_A ≤ 125°C, 5.0 V ≤ V_{PWR} ≤ 28 V, and is available in three different surface mount packages.

Features

- 5.0 V to 36 V Operation
- 120 mΩ $R_{DS(ON)}$ H-Bridge Switches
- TTL/CMOS Compatible Inputs
- PWM Frequencies to 10 kHz
- Automatic PWM Overcurrent Limiting
- Output Short Circuit Protection
- Overtemperature Output Current Reduction with Shutdown
- Undervoltage Shutdown
- Fault Status Reporting
- High-Side Current Feedback Output Provides Real-Time Current Monitoring

DH SUFFIX
20-LEAD HSOP
CASE 979C

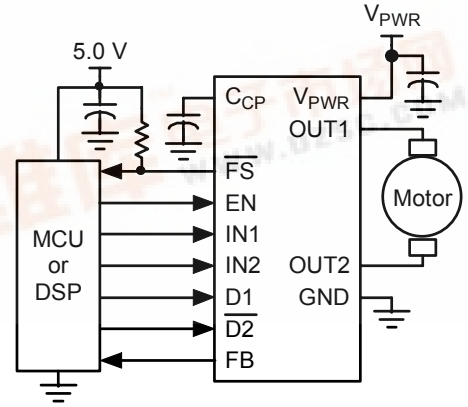
FC SUFFIX
44-LEAD QFN
CASE 1310

DWB SUFFIX
54-LEAD SOIC-EP
CASE 1377

PIN CONNECTIONS

HSOP		QFN				SOIC	
1	AGND	1	FB	23	IN2	1	PGND
2	FS	2	PGND	24	EN	2	PGND
3	IN1	3	PGND	25	NC	3	PGND
4	V_{PWR}	4	PGND	26	NC	4	PGND
5	V_{PWR}	5	PGND	27	V_{PWR}	5	NC
6	OUT1	6	PGND	28	V_{PWR}	6	NC
7	OUT1	7	PGND	29	V_{PWR}	7	NC
8	FB	8	PGND	30	V_{PWR}	8	D2
9	PGND	9	PGND	31	NC	9	NC
10	PGND	10	D2	32	NC	10	OUT2
11	PGND	11	OUT2	33	AGND	11	OUT2
12	PGND	12	OUT2	34	FS	12	OUT2
13	D2	13	NC	35	IN1	13	OUT2
14	OUT2	14	NC	36	V_{PWR}	14	NC
15	OUT2	15	NC	37	V_{PWR}	15	V_{PWR}
16	V_{PWR}	16	NC	38	OUT1	16	V_{PWR}
17	C_{CP}	17	OUT2	39	OUT1	17	V_{PWR}
18	D1	18	OUT2	40	NC	18	V_{PWR}
19	IN2	19	V_{PWR}	41	OUT1	19	NC
20	EN	20	V_{PWR}	42	OUT1	20	NC
		21	C_{CP}	43	NC	21	NC
		22	D1	44	NC	22	NC
						23	C_{CP}
						24	D1
						25	IN2
						26	EN
						27	NC
						28	NC
						29	NC
						30	AGND
						31	FS
						32	IN1
						33	NC
						34	NC
						35	NC
						36	NC
						37	V_{PWR}
						38	V_{PWR}
						39	V_{PWR}
						40	V_{PWR}
						41	NC
						42	OUT1
						43	OUT1
						44	OUT1
						45	OUT1
						46	NC
						47	FB
						48	NC
						49	NC
						50	NC
						51	PGND
						52	PGND
						53	PGND
						54	PGND

33887 Simplified Application Diagram



ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
PC33887DH/R2	-40 to 125°C	20 HSOP
PC33887FC/R2	-40 to 125°C	44 QFN
PC33887DWB/R2	-40 to 125°C	54 SOIC-EP

This document contains information on a product under development.
Motorola reserves the right to change or discontinue this product without notice.

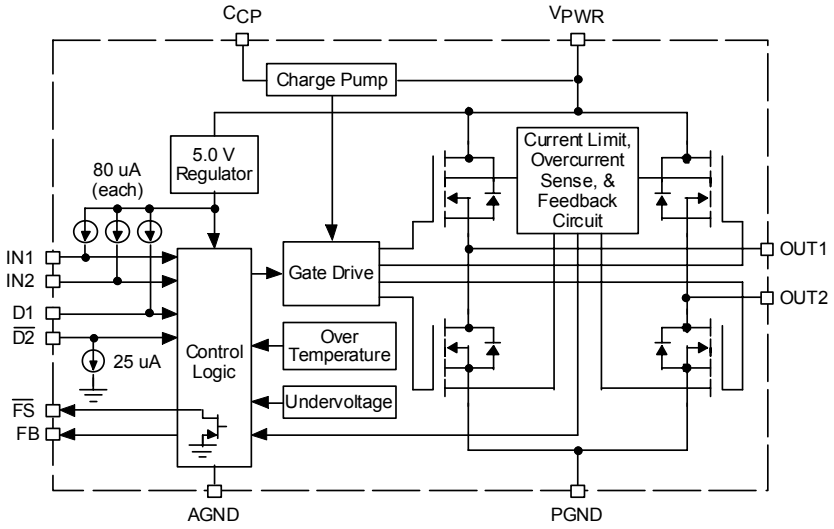


Figure 1. 33887 Internal Block Diagram

PIN FUNCTION DESCRIPTION

HSOP	QFN	SOIC	Pin Name	Description
1	33	30	AGND	Low current Analog signal ground.
2	34	31	$\overline{FS}$	Open drain active LOW Fault Status output requiring a pull-up resistor to 5.0 V.
3	35	32	IN1	True Logic input control of OUT1 (i.e., IN1 logic HIGH = OUT1 HIGH).
4, 5, 16	19, 20, 27–30	15–18, 37–40	V_{PWR}	Positive power source connection.
6, 7	38, 39, 41, 42	42–45	OUT1	H-Bridge output 1.
8	1	47	FB	Current sensing feedback output providing ground referenced 1/375th (0.00266) of H-Bridge high-side output current.
9–12	2–9, 36, 37	1–4, 51–54	PGND	Device high current power ground.
13	10	8	$\overline{D2}$	Active LOW input used to simultaneously tristate disable both H-Bridge outputs. When $\overline{D2}$ is Logic LOW, both outputs are tristate.
14, 15	11, 12, 17, 18	10–13	OUT2	H-Bridge output 2.
17	21	23	C_{CP}	External reservoir capacitor connection for internal Charge Pump.
18	22	24	D1	Active HIGH input used to simultaneously tristate disable both H-Bridge outputs. When D1 is Logic HIGH, both outputs are tristate.
19	23	25	IN2	True Logic input control of OUT2 (i.e., IN2 logic HIGH = OUT2 HIGH).
20	24	26	EN	True Logic input Enable control of device (i.e., EN logic High = Full Operation, EN logic LOW = Sleep Mode).
–	13–16, 25, 26, 31, 32, 40, 43, 44	5–7, 9, 14, 19–22, 27–29, 33–36, 41, 46, 48–50	NC	No internal connection to this pin.

MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Power Supply Voltage Normal Operation (Steady-State) Transient (Note 1)	 $V_{PWR(SS)}$ $V_{PWR(t)}$	 36 40	V
Input Voltage (Note 2)	V_{IN}	7.0	V
$\overline{FS}$ Status Output (Note 3)	$V_{\overline{FS}}$	7.0	V
Continuous Output Current (Note 4)	$I_{OUT(CONT)}$	6.0	A
ESD Voltage Human Body Model (Note 5) Machine Model (Note 6)	 V_{ESD1} V_{ESD2}	 TBD 200	V
Storage Temperature	T_{STG}	-65 to 150	°C
Ambient Temperature (Note 7)	T_A	-40 to 125	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Lead Soldering Temperature (Note 8)	T_{SOLDER}	260	°C
Approximate Junction-to-Board Thermal Resistance (Note 9) HSOP QFN SO-EP	$R_{\theta J-B}$	 ~5.0 ~18 ~12	°C/W

Notes:

1. Device will survive the transient overvoltage indicated for a maximum duration of 500 ms.
2. Exceeding the input voltage on IN1, IN2, EN, D1, or $\overline{D2}$ may cause a malfunction or permanent damage to the device.
3. Exceeding the pull-up resistor voltage on the open Drain $\overline{FS}$ pin may cause permanent damage to the device.
4. Continuous output current capability so long as junction temperature is $\leq$ 150°C.
5. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
6. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 100 pF, R_{ZAP} = 0 Ω).
7. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
8. Lead soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
9. Exposed heat sink pad plus the power and ground terminals comprise the main heat conduction paths. The actual $R_{\theta J-B}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply					
Operating Voltage Range (Note 10)					
Steady-State	$V_{PWR(SS)}$	5.0	–	36	V
Transient (t < 500 ms) (Note 11)	$V_{PWR(t)}$	–	–	40	V
Sleep State Supply Current (Note 12)	$I_{PWR(sleep)}$				
V_{EN} = 0 V, I_{LOUT} = 0 A		–	25	50	μA
Standby Supply Current	$I_{PWR(standby)}$				
I_{LOUT} = 0 A, V_{EN} = 5.0 V		–	–	20	mA
Threshold Supply Voltage					
Switch-OFF	$V_{PWR(thres-OFF)}$	4.15	4.4	4.65	V
Switch-ON	$V_{PWR(thres-ON)}$	4.5	4.75	5.0	V
Hysteresis	$V_{PWR(hys)}$	150	–	–	mV
Charge Pump					
Charge Pump Voltage					
V_{PWR} = 4.15 V	V_{CP} - V_{PWR}	3.35	–	–	V
V_{PWR} < 40 V		–	–	20	V
Control Inputs					
Input Voltage (IN1, IN2, D1, $\overline{D2}$)					
Threshold HIGH	V_{IH}	3.5	–	–	V
Threshold LOW	V_{IL}	–	–	1.4	V
Hysteresis	V_{HYS}	0.7	1.0	–	V
Input Current (IN1, IN2, D1)					
V_{IN} - 0.0 V	I_{IN}	-200	-80	–	μA
Input Current ($\overline{D2}$, EN)					
$V_{\overline{D2}}$ = 5.0 V	$I_{\overline{D2}}$	–	25	100	μA

Notes:

10. Parameter is guaranteed by design but not production tested.
11. Device will survive the transient overvoltage indicated for a maximum duration of 500 ms.
12. $I_{PWR(sleep)}$ is with sleep mode function Enabled.

STATIC ELECTRICAL CHARACTERISTICS (continued)
Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Outputs (OUT1, OUT2)					
Output-ON Resistance (Note 13)	R_{OUT}				
5.0 V < V_{PWR} < 28 V, T_J = 25°C		–	120	–	mΩ
8.0 V < V_{PWR} < 28 V, T_J = 150°C		–	–	225	mΩ
5.0 V < V_{PWR} < 8.0 V, T_J = 150°C		–	–	300	mΩ
Output Latch-OFF Current	$I_{LATCH-OFF}$	6.0	7.0	8.5	A
Output Latch-OFF Time	t_a	15	20.5	26	μs
Output Blanking Time	t_b	12	16.5	21	μs
High-Side Overcurrent Detection	$I_{OCD(H)}$	11	–	–	A
Low-Side Overcurrent Detection	$I_{OCD(L)}$	9.0	–	–	A
Leakage Current (Note 14)	$I_{OUT(leak)}$				
V_{OUT} = V_{PWR}		–	100	200	μA
V_{OUT} = GND		–	30	60	μA
Free-Wheeling Diode Forward Voltage Drop (Note 15)	V_F				
I_{OUT} = 3.0 A		–	–	2.0	V
Free-Wheeling Diode Reverse Recovery Time (Note 15)	t_{rr}	100	–	–	ns
Switch-OFF					
Thermal Shutdown	T_{LIM}	175	–	–	°C
Hysteresis	T_{HYS}	10	–	30	°C

Notes:
13. Output-ON resistance as measured from output to V_{PWR} and GND.
14. Outputs switched OFF with D1 or $\overline{D2}$.
15. Parameter is guaranteed by design but not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)
Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
High-Side Current Sense Feedback					
Feedback Current	I_{FB}				
I_{LOAD} = 0 mA		–	–	600	μA
I_{LOAD} = 500 mA		1.07	-1.33	1.60	mA
I_{LOAD} = 1.5 A		3.6	4.0	4.4	mA
I_{LOAD} = 3.0 A		7.2	8.0	8.8	mA
I_{LOAD} = 6.0 A		14.4	16.0	17.6	mA
Fault Status (Note 16)					
Fault Status Leakage Current (Note 17) $V_{\overline{FS}}$ = 5.0 V	$I_{\overline{FS}(leak)}$	–	–	10	μA
Fault Status SET Voltage (Note 18) $I_{\overline{FS}}$ = 300 μA	$V_{\overline{FS}(LOW)}$	–	–	1.0	V

Notes:
16. Fault Status output is an open Drain output requiring a pull-up resistor to 5.0 V.
17. Fault Status Leakage Current is measured with Fault Status HIGH and *not* SET.
18. Fault Status Set Voltage is measured with Fault Status LOW and SET with $I_{\overline{FS}}$ = 300 μA.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 5.0 V ≤ V_{PWR} ≤ 28 V and -40°C ≤ T_A ≤ 125°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Timing Characteristics					
PWM Frequency (Note 19)	f_{PWM}	–	–	10	kHz
Maximum Switching Frequency During Current Limit (Note 20)	f_{MAX}	–	–	20	kHz
Output ON Delay (Note 21) V_{PWR} = 14 V	$t_{d(ON)}$	–	–	18	μs
Output OFF Delay (Note 21) V_{PWR} = 14 V	$t_{d(OFF)}$	–	–	18	μs
Output Rise and Fall Time (Note 22) V_{PWR} = 14 V, I_{out} = 3.0 A	t_f, t_r	2.0	5.0	8.0	μs
Disable Delay Time (Note 23)	$t_{d(disable)}$	–	–	8.0	μs
Over-Current/Temperature Turn-OFF Time (Note 24)	t_{FAULT}	–	4.0	–	μs
Power-OFF Delay Time (Note 25)	t_{pod}	–	1.0	5.0	ms

Notes:

19. The outputs can be PWM controlled from an external source. The PWM Frequency is the externally induced output switching frequency, the maximum frequency of which is limited by the internal charge pump.
20. The Maximum Switching Frequency during Current Limit is internally implemented. The internal control produces a constant OFF-time PWM of the output. The output load current effects the Maximum Switching Frequency.
21. Output Delay is the time duration from the midpoint of the IN1 or IN2 input signal to the 10% or 90% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from the midpoint of the input signal to the 90% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from the midpoint of the input signal to the 10% point of the output response signal. See Figure 3.
22. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal. See Figure 4.
23. Disable Delay Time is the time duration from the midpoint of the D (disable) input signal to 10% of the output tristate response. See Figure 3.
24. Increasing output currents will become limited at 6.5 A. Hard shorts will breach the 6.5 A limit, forcing the output into an immediate tristate latch-OFF. See Figure 5 and Figure 6. Output current limiting will cause junction temperatures to rise. A junction temperature above 160°C will cause the output current limit to progressively "fold-back" or decrease to 2.5 A typical at 175°C where thermal latch-OFF will occur. See Figure 7.
25. This parameter has been characterized but is not production tested.

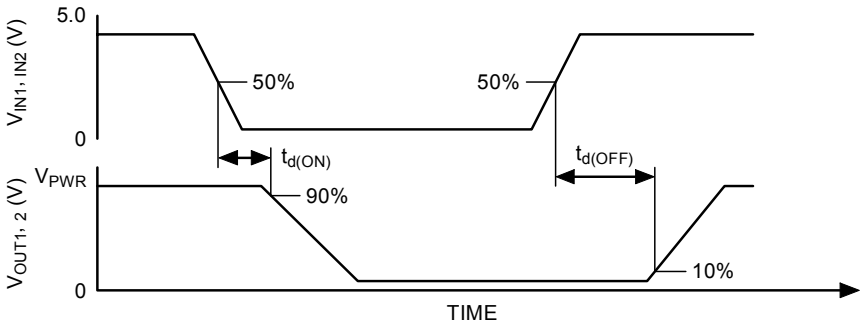


Figure 2. Output Delay Time

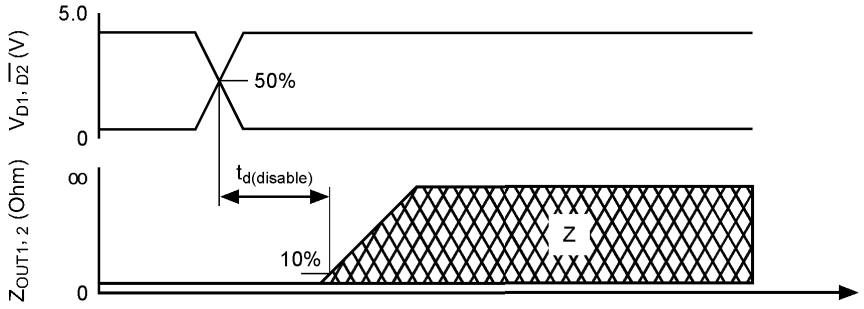


Figure 3. Disable Delay Time

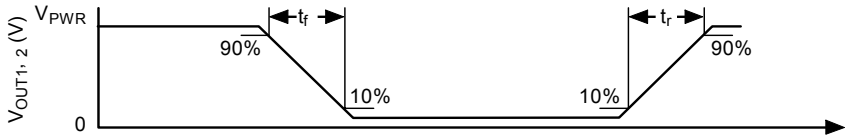


Figure 4. Output Switching Time

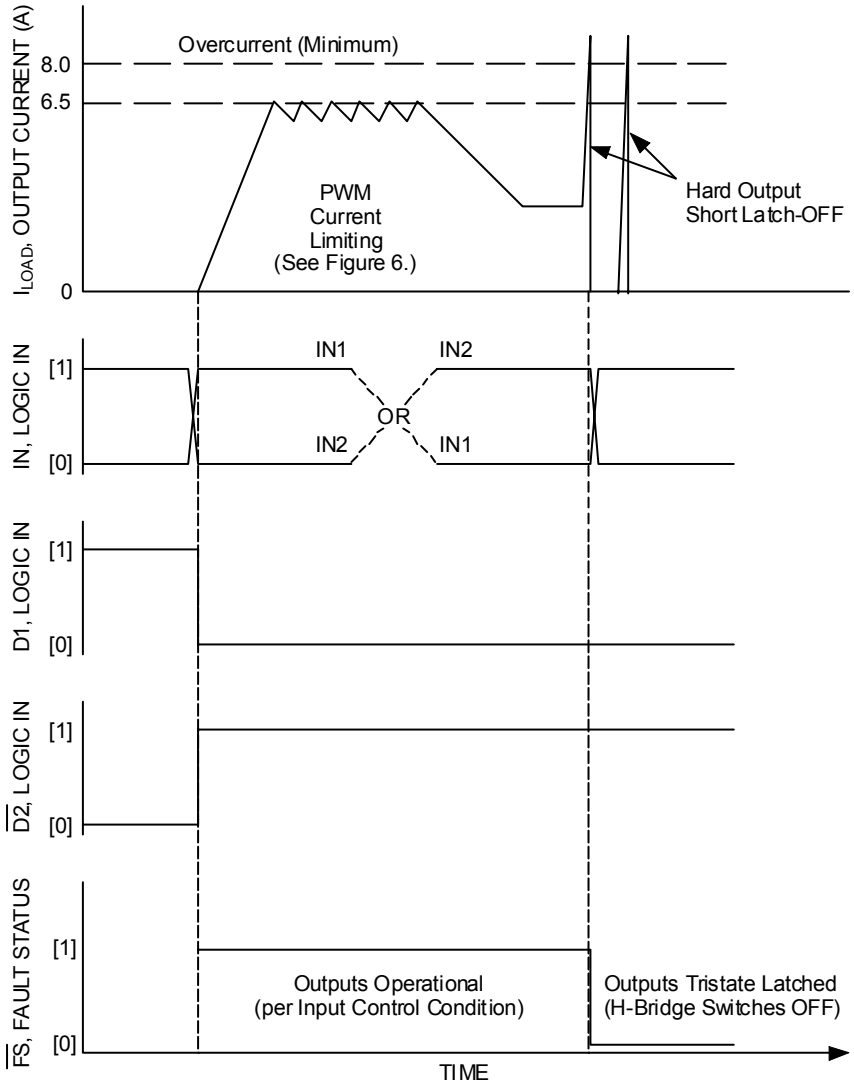


Figure 5. Output Load Current Limiting Versus Time

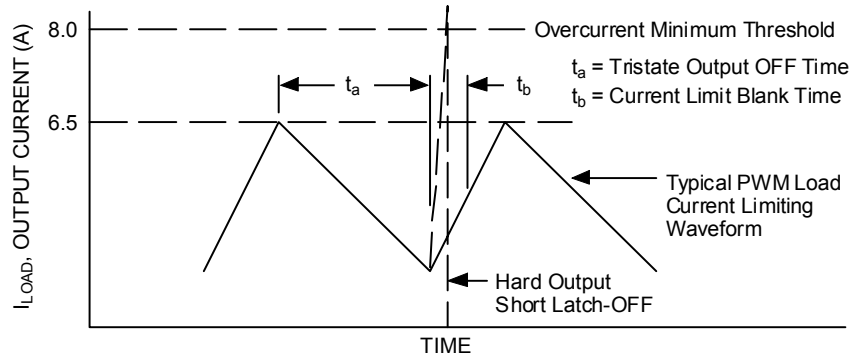


Figure 6. PWM Current Limiting Detail

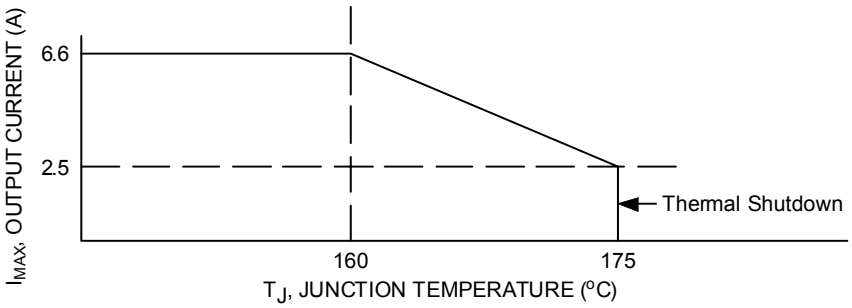


Figure 7. Maximum Output Current Limiting Versus Temperature

Table 1. Truth Table

The tristate conditions and the fault status are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = Low, H = High, X = High or Low, and Z = High impedance (all output power transistors are switched off).

Device State	EN	**Input Conditions**				**Status**	**Outputs**	
		D1	$\overline{D2}$	IN1	IN2	$\overline{FS}$	OUT1	OUT2
Forward	H	L	H	H	L	H	H	L
Reverse	H	L	H	L	H	H	L	H
Free Wheeling Low	H	L	H	L	L	H	L	L
Free Wheeling High	H	L	H	H	H	H	H	H
Disable 1 (D1)	H	H	X	X	X	L	Z	Z
Disable 2 ($\overline{D2}$)	H	X	L	X	X	L	Z	Z
IN1 Disconnected	H	L	H	Z	X	H	H	X
IN2 Disconnected	H	L	H	X	Z	H	X	H
D1 Disconnected	H	Z	X	X	X	L	Z	Z
$\overline{D2}$ Disconnected	H	X	Z	X	X	L	Z	Z
Undervoltage (Note 26)	H	X	X	X	X	L	Z	Z
Overtemperature (Note 27)	H	X	X	X	X	L	Z	Z
Overcurrent (Note 27)	H	X	X	X	X	L	Z	Z
Sleep Mode EN	L	X	X	X	X	H	Z	Z
EN Disconnected	Z	X	X	X	X	H	Z	Z

Notes:

26. In the case of an undervoltage condition, the outputs tristate and the fault status is SET logic LOW. Upon undervoltage recovery, fault status is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
27. When an overcurrent or overtemperature condition is detected, the power outputs are tristate latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

Numerous protection and operational features (speed, torque, direction, dynamic breaking, PWM control, and closed-loop control), in addition to the 6.0 A output current capability, make the 33887 a very attractive cost-effective solution for controlling a broad range of fractional horsepower DC-motors. A pair of 33887 devices can be used to control bipolar stepper motors in both directions. In addition, the 33887 can be used to control permanent magnet solenoids in a push-pull variable force fashion using PWM control. The 33887 can also be used to excite transformer primary windings with a switched square wave to produce secondary winding AC currents.

As shown in Figure 1, Internal Block Diagram, the 33887 is a fully protected monolithic H-Bridge with Enable, Fault Status reporting, and High-Side current sense feedback to accommodate closed-loop PWM control. For a DC-motor to run the input conditions need be as follows: Enable input logic HIGH, D1 input logic LOW, $\overline{D2}$ input logic HIGH, $\overline{FS}$ flag cleared (logic HIGH), with one IN logic LOW and the IN other logic HIGH to define output polarity. The 33887 can execute Dynamic Breaking by simultaneously turning-ON either the two High-Side or the two Low-Side H-Bridge switches; e.g., IN1 and IN2 logic HIGH or IN1 and IN2 logic LOW.

The 33887 outputs are capable of providing a continuous DC load current of 6.0 A from a 36 V V_{PWR} source. An internal charge pump supports PWM frequencies to 10 kHz. An external pull-up resistor is required for the open drain $\overline{FS}$ pin for fault status reporting. The 33887 has a current feedback output (FB) for "real time" monitoring of output current to facilitate closed-loop operation for motor speed and torque control.

Two independent inputs (IN1 and IN2) provide control of the two totem-pole half-bridge outputs. Two disable inputs (D1 and $\overline{D2}$) are for forcing the H-Bridge outputs to a high impedance state (all H-Bridge switches OFF). An EN pin controls an enable function that allows the 33887 to be placed in a power-conserving sleep mode.

The 33887 has Undervoltage Shutdown with automatic recovery, Output Current Limiting, Output Short-Circuit Latch-OFF, and Overtemperature Latch-OFF. An Undervoltage Shutdown, Output Short-Circuit Latch-OFF, or Overtemperature Latch-OFF fault condition will cause the outputs to turn-OFF (tristate) and the fault output flag to be set LOW. Either of the D inputs or V_{PWR} must be "toggled" to clear the fault flag. The Overcurrent/Overtemperature Shutdown scheme is unique and best described as using a junction temperature dependent output current "fold back" protection scheme. When an overcurrent condition is experienced, the current limited output is "ramped down" as the junction temperature increases above 160°C, until at 175°C the output current has decreased to about 2.5 A. Above 175°C, the Overtemperature Shutdown (Latch-OFF) occurs. This feature allows the device to remain in operation for a longer time with unexpected loads, but with regressive output performance at junction temperatures above 160°C.

FUNCTIONAL PIN DESCRIPTION

PGND and AGND

Power and analog ground pins. The power and analog ground pins should be connected together with a very low impedance connection.

V_{PWR}

V_{PWR} pins are the power supply inputs to the device. All V_{PWR} pins must be connected together on the printed circuit board with as short as possible traces offering as low impedance as possible between pins.

V_{PWR} pins have an undervoltage threshold. If the supply voltage drops below a V_{PWR} undervoltage threshold, the output power stage switches to a tristate condition and the fault status flag is SET and the Fault Status pin voltage switched to a logic LOW. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins and the fault status flag is automatically reset logic HIGH.

Fault Status ($\overline{FS}$)

This pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to 5.0 V. Refer to Table 1, Truth Table.

IN1, IN2, D1, $\overline{D2}$

These pins are input control pins used to control the outputs. These pins are 5.0 V CMOS-compatible inputs with hysteresis. The IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 and $\overline{D2}$ are complimentary inputs used to tristate disable the H-Bridge outputs.

When either D1 or $\overline{D2}$ is SET (D1 = logic HIGH or $\overline{D2}$ = logic LOW) in the disable state, outputs OUT1 and OUT2 are both tristate disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(standby)}$ current is reduced to a few milli-amperes. See Table 1, Truth Table, and STATIC ELECTRICAL CHARACTERISTICS (continued) table.

OUT1, OUT2

These pins are the outputs of the H-Bridge with integrated free-wheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and $\overline{D2}$ inputs. The outputs have Pulse Width

Modulated (PWM) current limiting above 6.5 A. The outputs also have thermal shutdown (tristate latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time t_b) incorporated to detect currents that are higher than current limit is activated at each output activation to facilitate detecting hard output short conditions. See Figure 6.

C_{CP}

Charge pump output pin. A filter capacitor (up to 33 nF) can be connected from the C_{CP} pin and PGND. The device can operate without the external capacitor, although the C_{CP} capacitor helps to reduce noise and allows the device to perform at maximum speed, timing, and PWM frequency.

EN

The EN pin is used to place the device in a sleep mode so as to consume very low currents. When the EN pin voltage is a logic LOW state, the device is in the sleep mode. The device is enabled and fully operational when the EN pin voltage is logic HIGH. An internal pull-down resistor maintains the device in sleep mode in the event EN is driven through a high impedance I/O or an unpowered microcontroller, or the EN input becomes disconnected.

FB

The device has a feedback output (FB) for “real time” monitoring of H-Bridge high-side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-Bridge high-side drivers. When running in the forward or reverse direction, a ground referenced 1/375th (0.00266) of load current is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can "read" the current proportional voltage with its analog to digital converter (ADC). This is intended to provide the user with motor current feedback for motor torque control. The accuracy is ± 20% at load currents <1.5 A and ± 10% at load currents >1.5 A.

If PWM-ing is implemented using the disable pin inputs (either D1 or $\overline{D2}$), a small filter capacitor (<1.0 μF) may be required in parallel with the external resistor to ground for fast spike suppression.

PERFORMANCE FEATURES

Short Circuit or Overcurrent Protection

If an output overcurrent condition is detected, the power outputs tristate latched-OFF independent of the input signal states and the fault status output flag is SET logic LOW. If the D1 voltage changes from logic HIGH to logic LOW or from logic LOW to logic HIGH on $\overline{D2}$, the output switches ON again and the fault status flag is reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and $\overline{D2}$), provided the device junction temperature is within the specified operating temperature.

PWM Current Limiting

The maximum current flow under normal operating conditions is limited to I_{MAX} (6.0 to 8.5 A). When the maximum current value is reached, the output stages are tristated for a fixed time (t_a) of 20 μs typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tristate duration until the next output ON cycle occurs. See Figure 6.

The PWM current limitation value is dependent upon the device junction temperature. When -40°C < T_J < 160°C, I_{MAX} is between 6.0 and 8.5 A. When T_J exceeds 160°C, the I_{MAX} current decreases linearly down to 2.5 A typical at 175°C typical (or where the device reaches T_{LIM}) and overtemperature shutdown occurs. See Figure 7. This feature allows the device to remain operational for a longer time but at a regressing output performance level at junction temperatures above 160°C.

Overtemperature Shutdown and Hysteresis

If an overtemperature condition occurs, the power outputs are tristate latched-OFF independent of the input signals and the fault status flag is SET logic LOW.

If the D1 voltage changes from logic HIGH to logic LOW or from logic LOW to logic HIGH on $\overline{D2}$, the output stage switches ON again, providing the temperature is below the overtemperature threshold limit minus the hysteresis. The fault status flag is reset (cleared) logic HIGH.

APPLICATIONS

A typical application schematic is shown in Figure 8. For precision high-current applications in harsh, noisy environments, the V_{PWR} by-pass capacitor may need to be substantially larger.

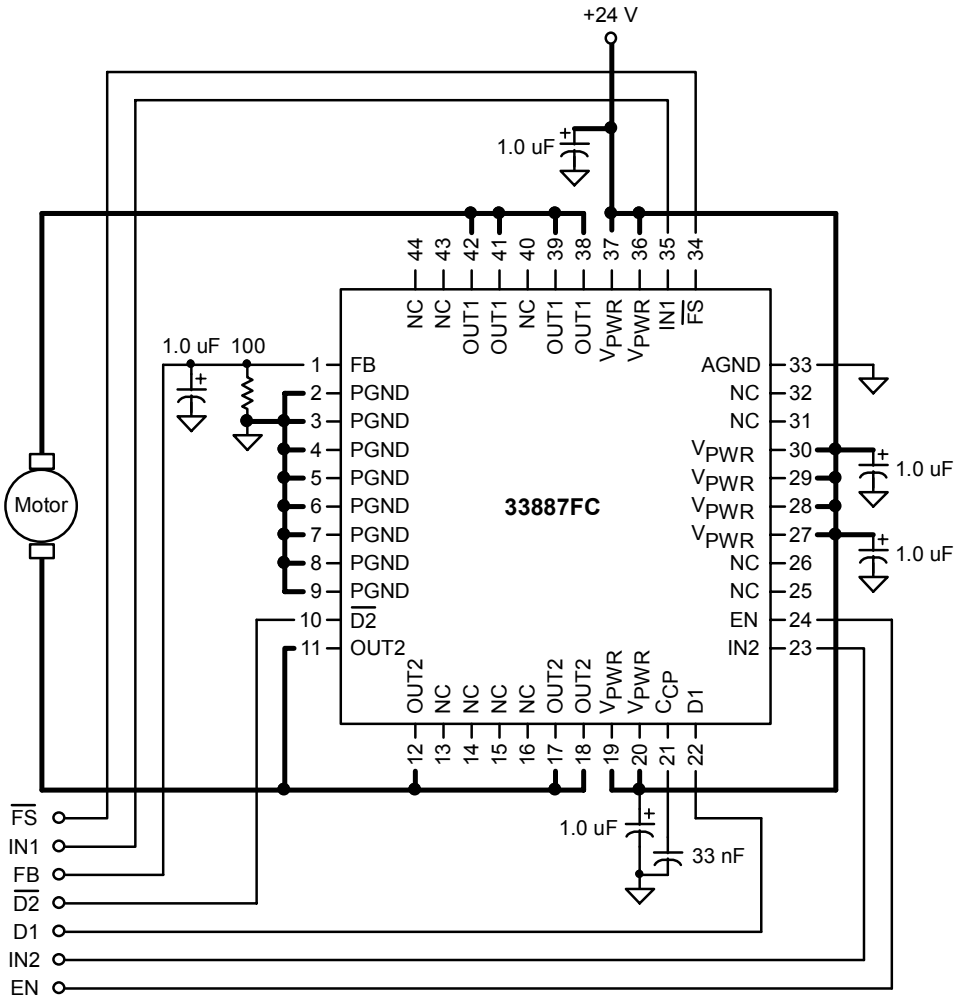
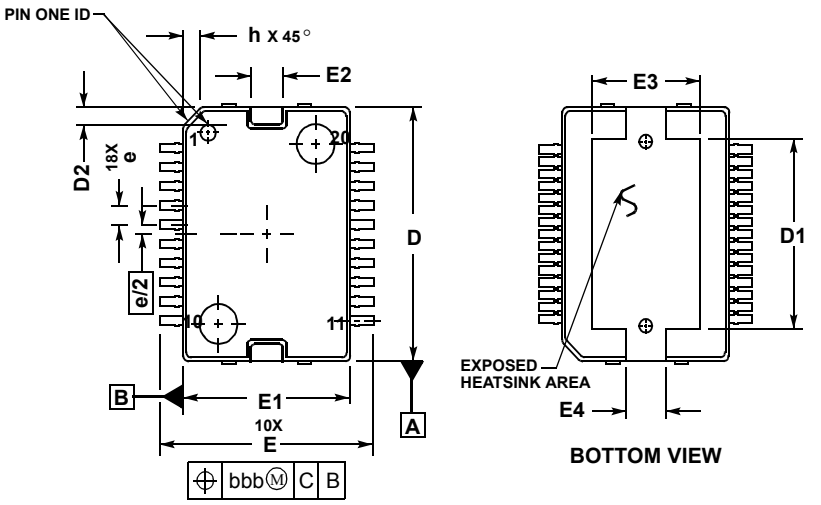


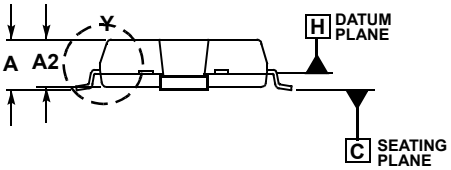
Figure 8. Typical Application Schematic

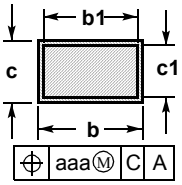
PACKAGE DIMENSIONS

DH SUFFIX
(20-LEAD HSOP)
PLASTIC PACKAGE
CASE 979C-02
ISSUE A

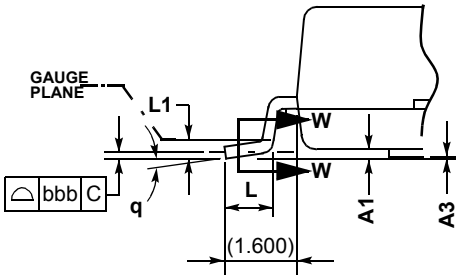


BOTTOM VIEW





SECTION W-W



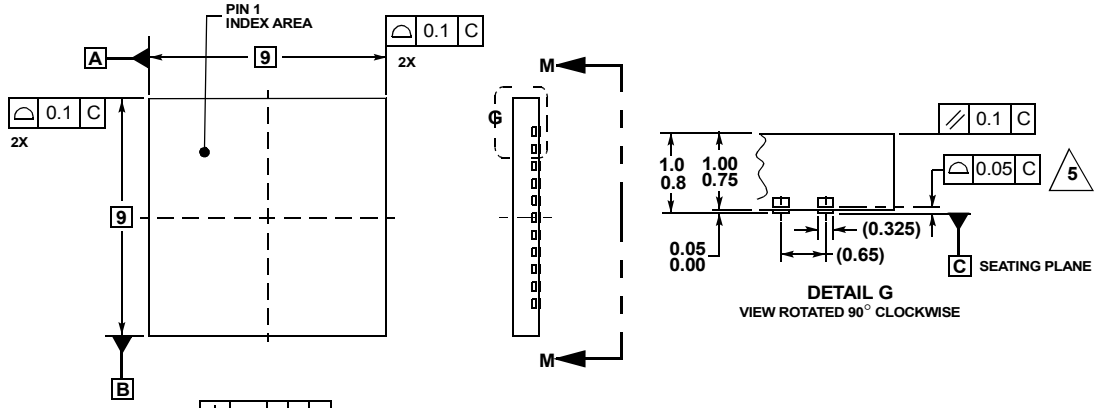
DETAIL Y

NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

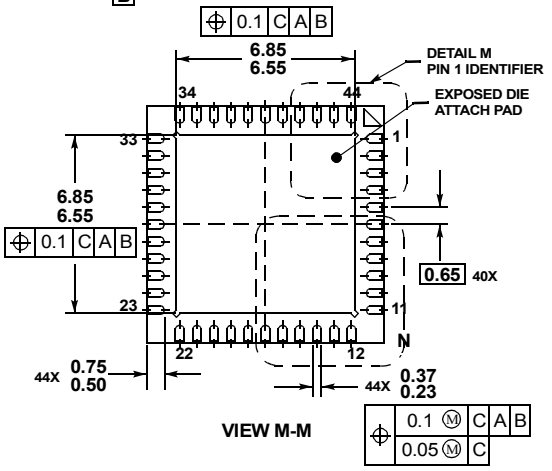
	MILLIMETERS	
DIM	MIN	MAX
A	3.000	3.400
A1	0.100	0.300
A2	2.900	3.100
A3	0.00	0.100
D	15.800	16.000
D1	11.700	12.600
D2	0.900	1.100
E	13.950	14.450
E1	10.900	11.100
E2	2.500	2.700
E3	6.400	7.200
E4	2.700	2.900
L	0.840	1.100
L1	0.350 BSC	
b	0.400	0.520
b1	0.400	0.482
c	0.230	0.320
c1	0.230	0.280
e	1.270 BSC	
h	---	1.100
q	0°	8°
aaa	0.200	
bbb	0.100	

PACKAGE DIMENSIONS

FC SUFFIX
(44-LEAD QFN)
PLASTIC PACKAGE
CASE 1310-01
ISSUE D

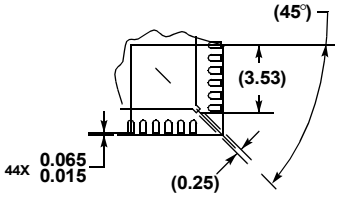


DETAIL G
VIEW ROTATED 90° CLOCKWISE



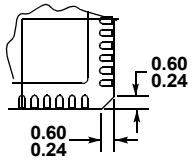
VIEW M-M

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
5. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
6. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLE IS 12.



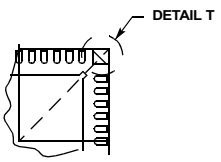
DETAIL N
PREFERRED CORNER CONFIGURATION

4

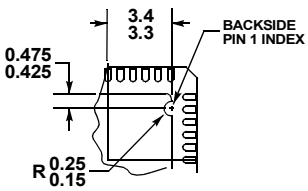


DETAIL N
CORNER CONFIGURATION OPTION

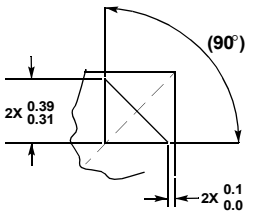
4



DETAIL M
PREFERRED BACKSIDE PIN 1 INDEX



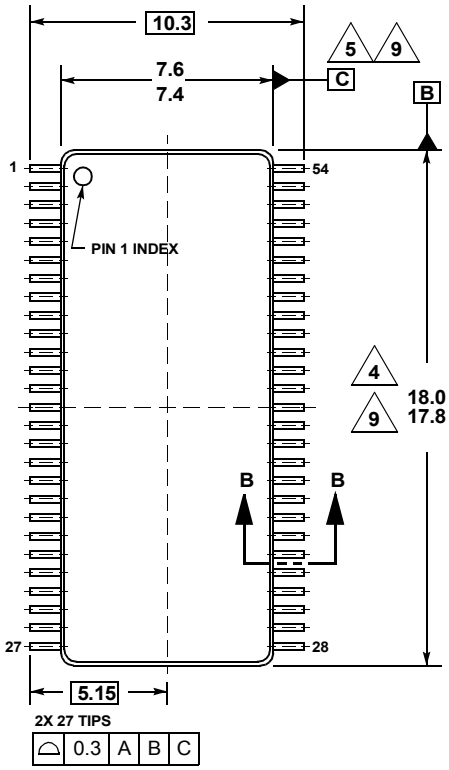
DETAIL M
BACKSIDE PIN 1 INDEX OPTION

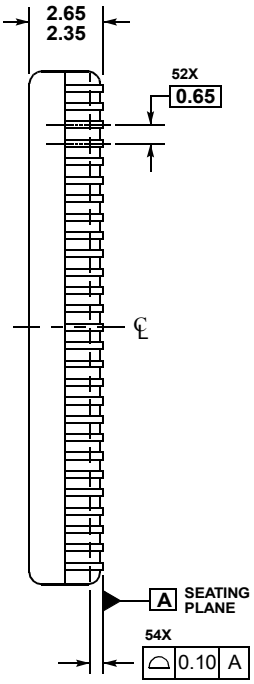


DETAIL T
PREFERRED BACKSIDE PIN1 INDEX

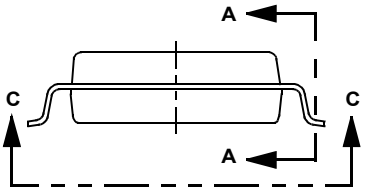
PACKAGE DIMENSIONS

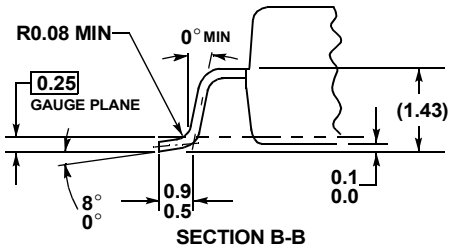
DWB SUFFIX
(54-LEAD SOIC EXPOSED PAD)
PLASTIC PACKAGE
CASE 1377-01
ISSUE B



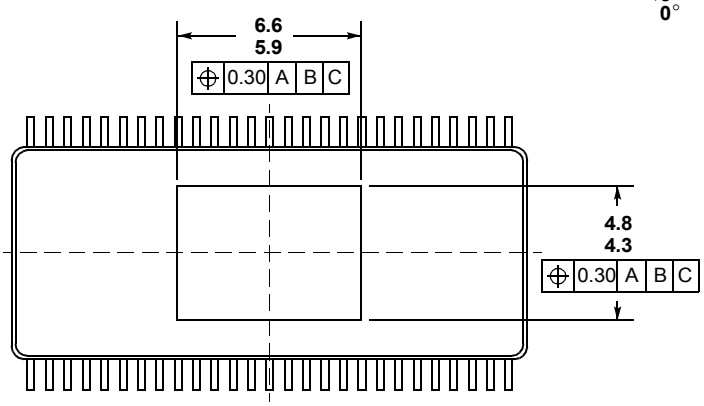


NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 MM.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.3 MM FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER-LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

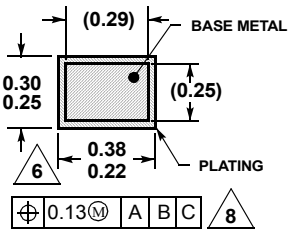




SECTION B-B



VIEW C-C



SECTION A-A
ROTATED 90° CLOCKWISE

NOTES

NOTES

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