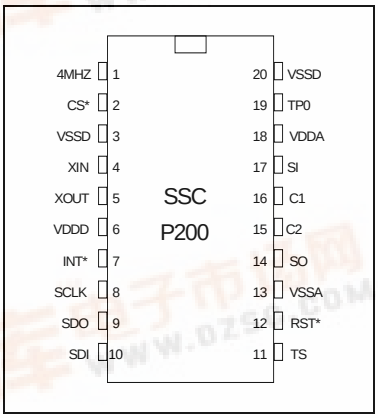
Intellon
CONNECTING THE FUTURE™

Technical Data Sheet **SSC P200 PL Network Interface Controller**

Features

- Enables Low-cost Networking Products
- EIA-600 (CEBus) Compatible Channel Access with Unacknowledged Services
- EIA-600 Physical Layer Transceiver
- Spread Spectrum Carrier™ Communication Technology
- SPI Host Processor Interface
- Single +5 Volt Power Supply Requirement
- 20 Pin SOIC Package

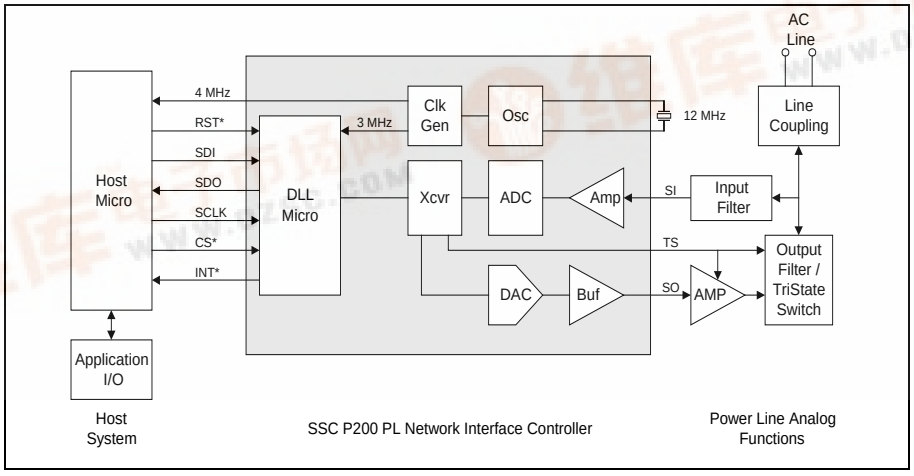


Introduction

The Intellon SSC P200 PL Network Interface Controller is a highly integrated spread spectrum communication transceiver and channel access interface for implementing low-cost networking products. The SSC P200 provides the Data Link Layer (DLL) control logic for EIA-600 channel access using unacknowledged services, a Spread Spectrum Carrier™ (SSC) transceiver, signal conditioning circuitry, and an SPI compatible host interface. A minimum of external circuitry is required to connect the SSC P200 to the AC power line, a twisted pair cable, or other communication medium. The SSC P200 is used with a host microcontroller to construct simple sensor and actuator devices for use in lighting control, process monitoring, access control, point-of-sale, telemetry and other systems requiring low-cost network capability.

The inherent reliability of SSC signaling technology and incorporation of basic data link functionality combine to provide substantial improvement in network and communication performance over other low-cost communication methods. The SSC P200 is the ideal basic communications element for a wide variety of low-cost networking applications.

SSC P200 Node Block Diagram



Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.3 to 7.0	V
V_{IN}	Input Voltage at any Pin	V_{SS}-0.3 to V_{DD}+0.3	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 seconds)	300	°C

Note:
Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages.

Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
V_{DD}	DC Supply Voltage	4.5	5.0	5.5	V
F_{OSC}	Oscillator Frequency		12 +/- 0.3%		MHz
T_A	Operating Temperature	-40	+25	+85	°C
	Humidity		non-condensing		

Electrical Characteristics

Conditions: V_{DD} = 4.5 to 5.5 V T= -40 to +85°C

Symbol	Parameter	Min	Typical	Max	Units
V_{OH}	Minimum High-level Output Voltage	2.4			V
V_{OL}	Maximum Low-level Output Voltage (1)			0.4	V
V_{IH}	Minimum High-level Input Voltage	2.0			V
V_{IL}	Maximum Low-level Input Voltage			0.8	V
Hys	Minimum Input Hysteresis	350			mV
I_{IL}	Maximum Input Leakage Current			+/-10	µA
v_{SO}	SSC Signal Output Voltage (2)		4		V_{P-P}
I_{DD}	Total Power Supply Current		25		mA

Notes:
1. I_{OL} = 2 mA
2. Z_L = 2K Ω || 10 pF

SSC P200 Control Timing

Symbol	Parameter	Min	Typical	Max	Unit
t_{RL}	RST* Pulse Width	150			nsec
t_{RESET}	Power-on Reset to Host Interface Active	10			msec

SSC P200 Pin Assignments

Pin	Mnemonic	Name	Description
1	4MHZ	4 MHz Clock Out	4 MHz clock output available for host microcontroller.
2	CS*	Chip Select	Digital input, active low. Enables serial peripheral interface.
3	VSS_D	Digital Ground	Digital ground reference.
4	XIN	Crystal Input	Connected to external crystal to excite the IC's internal oscillator and digital clock.
5	XOUT	Crystal Output	Connected to external crystal to excite the IC's internal oscillator and digital clock.
6	VDD_D	Digital Supply	5.0 VDC +/- 10% digital supply voltage with respect to VSS_D.
7	INT*	Interrupt	Digital output, active low. Attention request to host microcontroller.
8	SCLK	SPI Data Clock	Serial peripheral interface clock input from host microcontroller.
9	SDO	SPI Data Out	Data output to host microcontroller serial peripheral interface. SDO is` tristate when CS* is false.
10	SDI	SPI Data In	Data input from host microcontroller serial peripheral interface.
11	TS	Tristate	Active low digital output signal driven from the same internal signal that enables the output amplifier.
12	RST*	Reset	Active low digital input.
13	VSS_A	Analog Ground	Analog ground reference.
14	SO	Signal Output	Analog signal output. Tristate enabled with internal TS signal.
15	C2	Capacitor 2	Connection for 680pF capacitor to ground.
16	C1	Capacitor 1	Connection for 680pF capacitor to ground.
17	SI	Signal Input	Analog signal input.
18	VDD_A	Analog Supply	5.0 VDC +/- 10% analog supply voltage with respect to VSS_A.
19	TP0	Test Point 0	Reserved pin for testing.
20	VSS_D	Digital Ground	Digital ground reference.

SSC P200 Node Overview

The SSC P200 may be used in a wide variety of applications. A typical power line node application using the SSC P200 is illustrated in Figure 1. Resource intensive Data Link functions and Physical layer services of the protocol are provided by the SSC P200. Specific DLL services include transmission and reception of unacknowledged (UNACK) EIA-600 compatible packets, byte-to-symbol conversion for transmitted packets, symbol-to-byte conversion for received packets, transmit channel access based on packet priority and EIA-600 access rules, and CRC generation for transmitted packets and error checking of received packets.

The Host Microcontroller generates and decodes device addresses, interprets commands and data for the User Application and performs end to end protocol functions.

Output signal amplification and filtering, input signal filtering, and coupling of the node to the power line are performed using external components.

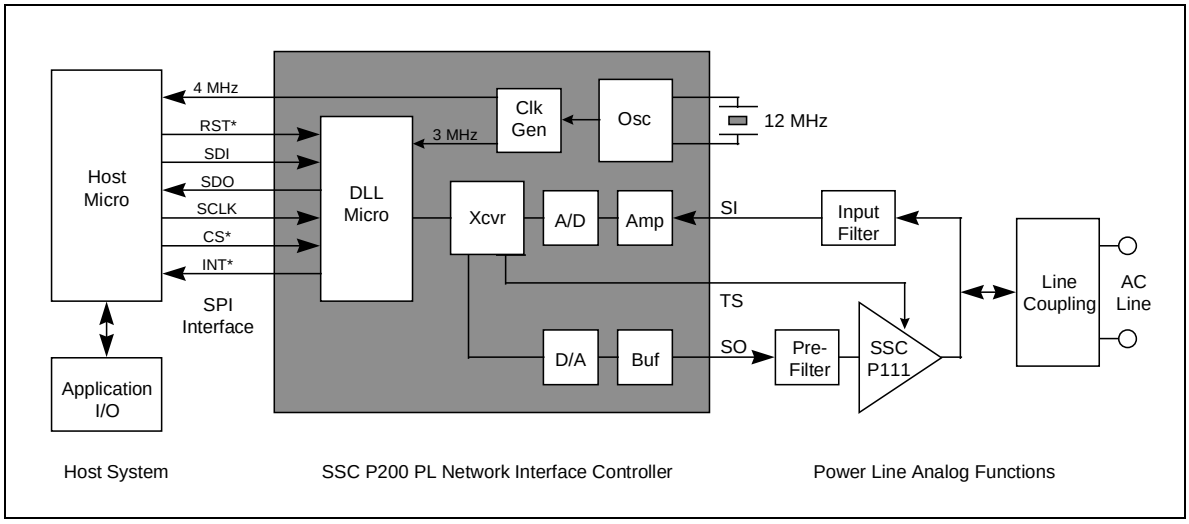


Figure 1. SSC P200 Power Line Node Application

SSC P200 Host Interface

SSC P200 interface to the Host system is supported through a Serial Peripheral Interface (SPI) using five I/O lines. A hardware, active-low, Reset (RST*) signal is also supplied by the Host. A simple protocol is used to transfer commands and data between the host and SSC P200. These commands and data include packets to be transmitted, received packets, status and configuration information.

SSC P200 Power Line Interface

Analog data is transferred between the AC power line and the SSC P200 over the P200 Signal In (SI) and Signal Out (SO) pins. In transmit mode, SSC “chirps” from the SSC P200 SO pin are filtered by the Pre-filter to remove harmonic energy (distortion) from the transmit signal and then amplified by the SSC P111 Power Line Media Interface IC. The SSC P111 is a high-efficiency amplifier and tri-state switch specifically designed for use in power line network systems. The amplifier is powered down and its output set to a high impedance condition when the SSC P200 TS signal is logic low, isolating the amplifier from the receive circuitry and reducing node power consumption during receive operation. When the SSC P200 TS signal is logic high, the communication signal is routed to the 60 Hz power line through the Power Line Coupling circuit. In receive mode, the communication signal passes through the Power Line Coupling Circuit and is filtered by the bandpass Input Filter. The resulting signal is then applied to the SSC P200 SI pin for processing.

P200 Host Interface Specification

Introduction

This section describes the functionality of the SSC P200 from the host's perspective. The services provided allow a host processor to optimally implement a network application, relying on the P200 for real-time network processing.

All SSC P200 system information is loaded by the host processor per the following description. All downloaded information is volatile and must be reloaded in the event of a power failure. Following verification of SSC P200 initialization (see Initialization Flow) system information (*Layer_Config_Info*) is written to the SSC P200 through a "write transaction" and the *Layer_Mgmt_Write* command (see Write Transaction Flow). The host may now transmit packets (*Packet*) using a "write transaction" and the *Packet_Transmit* command. Completion of the packet transmission and notification of the receipt of a packet are through an "attention sequence" (see Attention Sequence Flow) after which the host must determine the reason for the attention through a "read transaction" and the *Interface_Read* command (see Read Transaction Flow). Packets are retrieved through a "read transaction" and the *Packet_Receive* command. Details of the various data structures, commands and command protocol are indicated below.

Data Structures

Table 1. presents a map of the data structures accessible by the host. Subsequent sections describe the content of the structures.

Table1. Data Structures Map

Structure Name (full)	Structure Name (abbr.)	Bytes
Layer Configuration Information	*Layer_Config_Info*	7
Interface Flags	*Interface_Flags*	1
Node Control Flags	*Node_Control*	2
Status Information	*Status_Info*	6
DLL Link Access Control	*DLL_Access_Control*	1
Data Link Receive Link Status	*DLL_Rc_Link_Status*	1
Packet Format	*Packet*	41

Layer Configuration Information (*Layer_Config_Info*)

Table 2. presents a map of the read-write *Layer_Config_Info* structure which determines:

- The mode of operation.
- The maximum number of unsuccessful channel accesses due to backoffs per transmit attempt (*Max_Restarts*).

Table 2. Layer_Config_Info

Byte	Name	Use	Reset State
0	Mode_Control	Defines operating mode and *Max_Restarts*	0x00
1-6	Reserved	Reserved	0x0000

Layer_Config_Info.Mode_Control

	Bit 7	6	5	4	3	2	1	0
	--	MR3	MR2	MR1	MR0	--	SL1	SL0
RESET:	0	0	0	0	0	0	0	0

MC7 Reserved for future use and must be set to 0.

MC6-MC3 ***Max_Restarts*** **(MR3-MR0)** specifies the maximum restarts allowable due to backoffs before a transmit attempt failure is determined (a value of 120 is recommended for moderately to heavily active networks).

MR3	MR2	MR1	MR0	*Max_Restarts*
0	0	0	0	0
0	0	0	1	8
0	0	1	0	16
0	0	1	1	24
0	1	0	0	32
0	1	0	1	40
0	1	1	0	48
0	1	1	1	56
1	0	0	0	64
1	0	0	1	72
1	0	1	0	80
1	0	1	1	88
1	1	0	0	96
1	1	0	1	104
1	1	1	0	112
1	1	1	1	120

MC2 Reserved for future use and must be set to 0.

MC1-MC0 ***Service_Level*** **(SL1-SL0)** determines mode of operation and must be set to 0x11.

SL1	SL0	*Service_Level*
0	0	Reserved
0	1	Reserved
1	0	Reserved
1	1	P200 mode

The P200 acts as a Medium Access device utilizing the EIA CEBus channel access protocol, transmit service, and packet format. The host is responsible for address recognition and may redefine the contents of the address fields within the header and the NPDU (see Packet Format (Packet)).

Packet Receive Received packets are transferred to the host without address detection, which requires the host to determine the address status of the packet. The receipt of a new *Receive_Header* is posted via *Interface_Flags.Rc_Except*. After retrieving the header via the *Read_Receive_Header* command the host must verify that the receive service is UNACK before determining if the packet is to be accepted or ignored based on the destination addresses. The host must issue *Node_Control.Rcv_Disposition* prior to the receipt of the packet's CRC such that appropriate action at the end of the packet can be performed. If *Node_Control.Rcv_Disposition* is not issued in time, the packet will be ignored. If the packet has been accepted, *Interface_Flags.Rc_Attn* will be posted. The *Receive_NPDU* can be retrieved via the *Read_Receive_Information* (preferred) or *Packet_Receive* command.

Packet Transmit The host establishes the addresses and NPDU for transmitted packets.

Only UNACK service is allowed. Transmission with other services will be ignored with an *Misc_Xmit* transmit error posted.

Interface Flags (*Interface_Flags*)

The read-only *Interface_Flags* register contains information relative to the state of the P200 including:

- The fact that a packet has been received and whether a receive exception exists.
- Whether a transmit has completed and whether a transmit exception exists.
- The presence of a physical layer failure or host interface error.
- The reset state of the device.

NOTE: All flags are cleared upon executing the *Interface_Read* command (see Table); therefore, it is the responsibility of the host to service all flags in *Interface_Flags* when read.

Interface_Flags

	Bit 7	6	5	4	3	2	1	0
	RA	TA	TEX	REX	PLF	IE	--	RES
RESET:	0	0	0	0	0	0	0	1

IF7 ***Rc_Attn*** **(RA)** indicates that a valid packet has been received.

0 No packet received.

1 Packet received (Attention sequence generated).

IF6 ***Tr_Attn*** **(TA)** indicates that a pending packet transmission is complete.

0 No packet transmitted.

1 Packet transmit completed (Attention sequence generated).

IF5 ***Tr_Except*** **(TEX)** indicates that the Preamble EOF of a transmission attempt has been successfully transmitted to the medium.

0 Preamble EOF not yet transmitted.

1 Preamble EOF transmitted (Attention sequence generated).

IF4 ***Rc_Except*** **(REX)** indicates that a complete header has been received.

0 No header received.

1 Header received (Attention sequence generated).

IF3 ***Physical_Layer_Failure*** **(PLF)** indicates an error was detected in the physical layer. *DLL_Rc_Link_Status.Phy_Layer_Fail_Status* may be read to determine cause for failure.

0 No physical layer exists.

1 Physical failure occurred (Attention sequence generated).

IF2 ***Interface_Error*** **(IE)** indicates an SPI protocol error occurred on the last attempted host command sequence.

0 No SPI protocol error occurred.

1 SPI protocol error detected.

IF1 Reserved for future use and will be read as 0.

IF0 ***IC_Reset*** **(RES)** indicates the P200 is in a reset condition. A *Layer_Mgmt_Write* command is required to initialize and activate.

0 P200 not reset (running).

1 P200 reset (waiting for *Layer_Mgmt_Write* command).

Node Control Flags (*Node_Control*)

The write-only *Node_Control* structure contains flags which control node operation including:

- Specifying general and specific host busy situations.
- Aborting the transmission of a packet.
- Controlling the receipt of packets.

Node_Control.Flag_0

	Bit 7	6	5	4	3	2	1	0
	RD2	RD1	RD0	--	HB	AT	ULB	--
RESET:	0	0	0	0	0	0	0	0

F0-7 - F0-5 ***Rcv_Disposition*** **(RD2-RD0)** determines the response to a received header and therefore the subsequent disposition of the received packet.

RD2	**RD1**	**RD0**	***Rcv_Disposition***
0	0	0	Ignore the packet.
0	0	1	Receive packet and generate *Interface_Flags.Rc_Attn* at packet end.
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

F0-4 Reserved for future use and must be set to 0.

F0-3 *Host_Busy* (HB) indicates host cannot process any attention requests at this time.

0 All attention requests generated.
1 No attention requests generated.

F0-2 ***Abort_Transmission*** **(AT)** aborts current packet transmission (if not already completed). Abort occurs prior to channel access or after transmission completes (i.e. fragments will not be produced).

0 No abort
1 Abort the current transmission.

F0-1 ***Upper_Layer_Busy*** **(ULB)** indicates host cannot process received packets at this time. No attention requests for received packets are generated (the first received packet is stored—subsequent received packets are refused/ignored). Other attention requests (including transmit complete) are generated normally. If an attention request is generated due to a non-"received packet" reason, but a packet has been received, it is the responsibility of the host to either process the received packet immediately or store the fact and process the received packet later. See description of *Interface_Flags* pertaining to processing all set flags.

0 All attention requests generated.
1 No attention requests generated for received packets.

F0-1-F0-0 Reserved for future use and must be set to 0.

Status Information (*Status_Info*)

The read-only *Status_Info* structure as shown in Table 3 contains flags including:

- The status of the last packet's transmission.
- The P200 device type and version.

Table 3. Status_Info

Byte	Name	Use	Reset State
0	Status_Flags	Contains various flags regarding transmit completion and statistics counter overflow conditions.	0x00
1	Reserved	Reserved	0x00
2	Reserved	Reserved	0x00
3	Reserved	Reserved	0x00
4	Reserved	Reserved	0x00
5	Device_ID	Contains device identifier and version control information.	Device Based

Status_Info.Status_Flags

	Bit 7	6	5	4	3	2	1	0
	--	--	--	--	TS3	TS2	TS1	TS0
RESET:	0	0	0	0	0	0	0	0

SF7-SF4 Reserved for future use and will be read as 0.

SF3-SF0 *Tx_Status_Code* (TS3-TS0) indicates the last packet's transmit completion status.

TS3	TS2	TS1	TS0	*Tx_Status_Code*
0	0	0	0	Success: packet transmit succeeded
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Excessive_Collisions: exceeded *Max_Restarts* attempts
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Misc_Xmit: detected unexpected packet termination or attempted to transmit ACK, ADRACK or ADRUNACK packet.
1	0	0	1	Physical_Failure: transceiver or medium failure detected.
1	0	1	0	Transmit_Aborted: host aborted transmission via *Node_Control.Flag_0.Abort_Transmission.*
1	0	1	1	Max_Retrans_Exceeded: could not complete transmission within Max_Retrans time.
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Status_Info. Device_ID

	Bit 7	6	5	4	3	2	1	0
	DT3	DT2	DT1	DT0	DV3	DV2	DV1	DV0
RESET:	0	0	1	1	x	x	x	x

DID7-DID4 ***Device_Type*** **(DT3-DT0)** indicates the network interface controller type.

DT3	DT2	DT1	DT0	*Device_Type*
0	0	0	0	CEThinx
0	0	0	1	P400
0	0	1	0	R400
0	0	1	1	P200
0	1	0	0	P300
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

DID3-DID0 ***Device_Version*** **(DV3-DV0)** indicates the device firmware version type.

DV3	DV2	DV1	DV0	*Device_Version*
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Data Link Access Control (*DLL_Access_Control*)

The write-only *DLL_Access_Control* register specifies the time between channel accesses:

DLL_Access_Control

	Bit 7	6	5	4	3	2	1	0
	--	--	CAP1	CAP0	--	--	--	--
RESET:	0	0	0	0	0	0	0	0

DAC7-DAC6 Reserved for future use and must be set to 0.

DAC5-DAC4 ***Ch_Access_Period*** **(CAP1-CAP0)** specifies the minimum required time in milliseconds between attempted transmit channel accesses and is used to limit the duty cycle of packet transmissions based on the device's power supply design.

CAP1	**CAP0**	***Ch_Access_Period***
0	0	0 ms
0	1	100 ms
1	0	200 ms
1	1	300 ms

DAC3-DAC0 Reserved for future use and must be set to 0.

Data Link Receive Link Status (*DLL_Rc_Link_Status*)

The read-only *DLL_Rc_Link_Status* register indicates the type of physical layer failure detected:

DLL_Rc_Link_Status

	Bit 7	6	5	4	3	2	1	0
	--	--	PLS2	PLS1	PLS0	--	--	--
RESET:	0	0	0	0	0	0	0	0

DLS7-DLS6 Reserved for future use and will be set to 0.

DLS7 - DLS5 ***Phy_Layer_Fail_Status*** **(PLS2-PLS0)** If *Interface_Flags.Physical_Layer_Failure* is TRUE, indicates cause of physical layer failure.

PLS2	**PLS1**	**PLS0**	***Phy_Layer_Fail_Status***
0	0	0	Unexpected end-of-packet was detected.
0	0	1	Transceiver interface error.
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

DLS2-DLS0 Reserved for future use and will be read as 0.

Packet Format (*Packet*)

The format of the *Packet* data structure conforms to EIA-600 and is included as a convenience and to aid in understanding the host command protocol (see Command Protocol). A *Packet* (Table 4) is comprised of a header (Tables 5 and 6) containing the data link control field and addressing fields, and the information to be transmitted, called a Network Layer Protocol Data Unit (NPDU).

Table 4. Packet

Bytes	Field
0-8	*Transmit_Header* OR *Receive_Header*
9-40	*Transmit_NPDU* OR *Receive_NPDU*

Table 5. Transmit_Header

Bytes	Field Name	Comments
0	Tr_Control_Field	Transmit *DLL_Control_Field*
1-2	Tr_Address_Field_0	Transmit address fields—see *DLL_Control_Field* for use.
3-4	Tr_Address_Field_1	
5-6	Tr_Address_Field_2	
7-8	Tr_Address_Field_3	

Table 6. Receive_Header

Bytes	Field Name	Comments
0	Rc_Control_Field	Receive *DLL_Control_Field*
1-2	Rc_Address_Field_0	Receive address fields—see *DLL_Control_Field* for use.
3-4	Rc_Address_Field_1	
5-6	Rc_Address_Field_2	
7-8	Rc_Address_Field_3	

DLL_Control_Field

	Bit 7	6	5	4	3	2	1	0
	--	CL	--	PR1	PR0	PT2	PT1	PT0
RESET:	0	0	0	0	0	0	0	0

CF7 Reserved

CF6 ***Service_Class*** **(CL)** indicates the service class bit value of the current packet.

0 Basic service (normal CEBus addressing)
1 Extended service

NOTE: *Service_Class* determines the network usage of the *Tr_Address_Field_n* and *Rc_Address_Field_n* in *Transmit_Header* and *Receive_Header*, respectively.

Transmit/Receive Address Field	***Service_Class*** **= Basic**	***Service_Class*** **= Extended**
Address_Field_0	CEBus destination address	Host determined
Address_Field_1	CEBus destination house code	
Address_Field_2	CEBus source address	
Address_Field_3	CEBus source house code	

CF5 Reserved

CF4-CF3 ***Packet_Priority*** **(PR1-PR0)** indicates the transmit priority field value of the current packet.

PR1	PR0	*Priority*
0	0	High
0	1	Standard
1	0	Deferred
1	1	Reserved

CF2-CF0 ***Packet_Type*** **(PT2-PT0)** indicates the packet type or transmit level field value of the current packet.[1]

PT2	PT1	PT0	*Packet_Type*
0	0	0	Reserved
0	0	1	Reserved
0	1	0	UNACK
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Table 7. Transmit_NPDU

Field Name	Bytes	Comments
Tr_NPDU	0-31	NPDU (Data Link Information Field) is stored for transmission in the order received from the host.

Table 8. Receive_NPDU

Field Name	Bytes	Comments
Rc_NPDU	0-31	NPDU (Data Link Information Field) is stored in the order received from the medium.

[1] EIA-600 allows other transmit levels (ACK, ADRACK and ADRUNACK) which are supported by Intellon's P300 and P400 products.

Host Commands

Command Descriptions

The host interface supports the commands given in Table 9 below.

Table 9. Commands

Cmd Value	Cmd Code	Command Name	Use
0x00	FIE	Force_Interface_Error	Forces interface error condition.
0x01	RST	Reset	Disables all functions and I/O except host interface. (Reset signal line is more reliable as it does not require that host interface be operational.) A *Layer_Mgmt_Write* command is necessary to initiate any activity subsequent to a reset.
0x02	LR	Layer_Mgmt_Read	Read *Layer_Config_Info*
0x03	LW	Layer_Mgmt_Write	Write *Layer_Config_Info*
0x04	IR	Interface_Read	Read *Interface_Flags*. All flags are cleared following the execution of this command.
0x05	CW	Control_Write	Write *Node_Control*
0x06	SR	Status_Read	Read *Status_Info*
0x07	--	Reserved	Reserved
0x08	PR	Packet_Receive	Read received *Packet*. Accesses buffered data link header (Control field, Destination Address and Source Address) and NPDU field. *Packet_Read* can always be used in response to *Interface_Flags.Rc_Attn*. However, host interface traffic can be reduced if, after reading a FALSE *DLL_Rc_Link_Status.Rc_Addr_DIff*, *Read_Receive_Information* is used to retrieve the *Receive_NPDU* (it is assumed that the *Receive_Header* has been retrieved previously via *Packet_Receive* or *Read_Receive_Header*).
0x09	PT	Packet_Transmit	Write *Packet* *Packet_Transmit* can always be used to transmit *Packet*. If multiple *Packets* are being sent to the same remote device, *Transmit_Header* can be set using *Packet_Transmit* or *Write_Transmit_Header*, and the *Transmit_NPDU* can be sent using *Write_Transmit_Invoke*. Issuing the *Packet_Transmit* command when a previous transmit is still in progress (*Interface_Flags.Tr_Attn* is FALSE and *Interface_Flags.Tr_Except* is TRUE) will result in the command being ignored and posting an *Interface_Flags.Interface_Error*.
0x0A	RRI	Read_Receive_Information	Read buffered *Receive_NPDU*. (See *Packet_Receive* command)

Cmd Value	Cmd Code	Command Name	Use
0x0B	WTI	Write_Transmit_Invoke	Write *Transmit_NPDU*. (See *Packet_Transmit* command) Issuing the *Write_Transmit_Invoke* command when a previous transmit is still in progress (*Interface_Flags.Tr_Attn* is FALSE and *Interface_Flags.Tr_Except* is TRUE) will result in the command being ignored and posting an *Interface_Flags.Interface_Error*.
0x0C	RRH	Read_Receive_Header	Read *Receive_Header*. This command accesses the unbuffered header. (See *Packet_Receive* command)
0x0D	WTH	Write_Transmit_Header	Write *Transmit_Header* for subsequent transmit packets. (See *Packet_Transmit* command) Issuing the *Write_Transmit_Header* command when a previous transmit is still in progress (*Interface_Flags.Tr_Attn* is FALSE and *Interface_Flags.Tr_Except* is TRUE) will result in the command being ignored and posting an *Interface_Flags.Interface_Error*. Completion of the *Write_Transmit_Header* command is posted via *Interface_Flags.Tr_Attn* and *Interface_Flags.Tr_Except*.
0x0E-0x45	--	Reserved	Reserved
0x46	WRS-46	Write_Register_46	Write *DLL_Access_Control*
0x47-0x83	--	Reserved	Reserved
0x84	RRS-4	Read_Register_4	Read *DLL_Rc_Link_Status*
0x85-0xFF	--	Reserved	Reserved

Command Protocol

Commands and data structures are conveyed between the host and the P200 via the Serial Peripheral Interface and a protocol sequence described in Table 10 below.

Table 10. Command Protocol

Cmd Code	Sequence From Host	Sequence From P200	Comments
FIE	[FIE]	[Length]	Length = 0
RST	[RST][Length]	--	Length = 0
LR	[LR]	[Length] [*Layer_Config_Info*]	All bytes in *Layer_Config_Info* are transferred (Length = 7).
LW	[LW][Length] [*Layer_Config_Info*]	--	Bytes 0..(Length-1) in *Layer_Config_Info* are transferred starting at *Layer_Config_Info.Mode_Control.*
IR	[IR]	[Length] [*Interface_Flags*]	*Interface_Flags* is transferred (Length = 1).
CW	[CW][Length] [*Node_Control*]	--	Bytes 0..(Length-1) in *Node_Control* are transferred.
SR	[SR]	[Length][*Status_Info*]	All bytes in *Status_Info* are transferred (Length = 6).
PR	[PR]	[Length] [*Packet*]	All received bytes in *Packet* are transferred preceded by Length which is the number of bytes following. (Length is determined by received packet)
PT	[PT][Length] [*Packet*]	--	All bytes in *Packet* are transferred preceded by Length which is the number of bytes following. NOTE: If Length=0, the previously transmitted packet is retransmitted.
RRI	[RRI]	[Length] [*Receive_NPDU*]	All received bytes in *Receive_NPDU* are transferred preceded by Length which is the number of bytes following. (Length is determined by received packet)
WTI	[WTI][Length] [*Transmit_NPDU*]	--	All received bytes in *Transmit_NPDU* are transferred preceded by Length which is the number of bytes following. NOTE: If Length=0, the previously transmitted packet is retransmitted.
RRH	[RRH]	[Length] [*Receive_Header*]	All bytes in *Receive_Header* are transferred (Length = 9).
WTH	[WTH][Length] [*Transmit_Header*]	--	All bytes in *Transmit_Header* are transferred (Length = 9)
WRS-46	[WRS-46][Length] [*DLL_Access_Control*]		*DLL_Access_Control* is transferred (Length = 1).
RRS-4	[RRS-4]	[Length] [*DLL_Rc_Link_Status*]	*DLL_Rc_Link_Status* is transferred (Length = 1).

Serial Peripheral Interface

Signal Description

The Serial Peripheral Interface (SPI) between the Host and P200 uses 5 unidirectional I/O lines. An additional interface line is Reset. See Table 11.

Table 11. SPI Mode Pin Descriptions

Mnemonic	Name	Direction	Use
INT*	Interrupt	Output	Active low. Used to indicate an attention request (packet received or transmit packet completed) or "ready for SPI byte transfer."
CS*	Chip Select	Input	Active low. Must be asserted during a read or write command operation ("transaction").
SCLK	Shift Clock	Input	Used to synchronize data transfer.
SDI	Serial Data In	Input	Serial data input (normally connected to host's SDO signal). Data is shifted MSB first.
SDO	Serial Data Out	Output	Serial data output (normally connected to host's SDI signal). Data is shifted MSB first.
RST*	Reset	Input	Reset signal line. The host may assert this signal low (open collector drive) to provide a hardware reset.

Host Interactions Description

Host interactions are of the following four basic types:

- Initialization
- Write Transaction
- Read Transaction
- Attention Sequence

Initialization Flow

Upon power-up, or following a *Reset* command, the P200 performs an internal diagnostic and setup sequence. Commands cannot be sent to the device until this sequence is complete. The following sequence of commands in Figure 2 may be used to check for the ready condition:

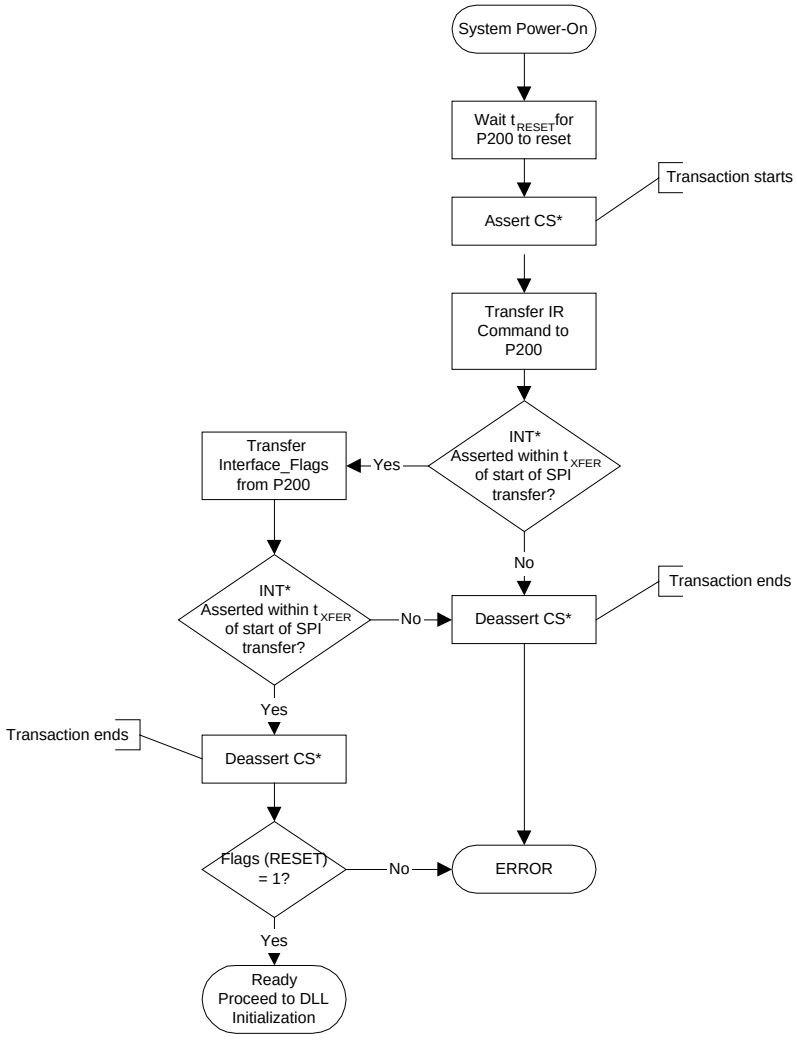


Figure 2. Initialization Flow Diagram

At this point, the host should set up the *Layer_Config_Info*, using the Write Transaction sequence described in the next section.

Write Transaction Flow

The following steps in Figure 3 should be taken to issue write commands and data and control to the P200:

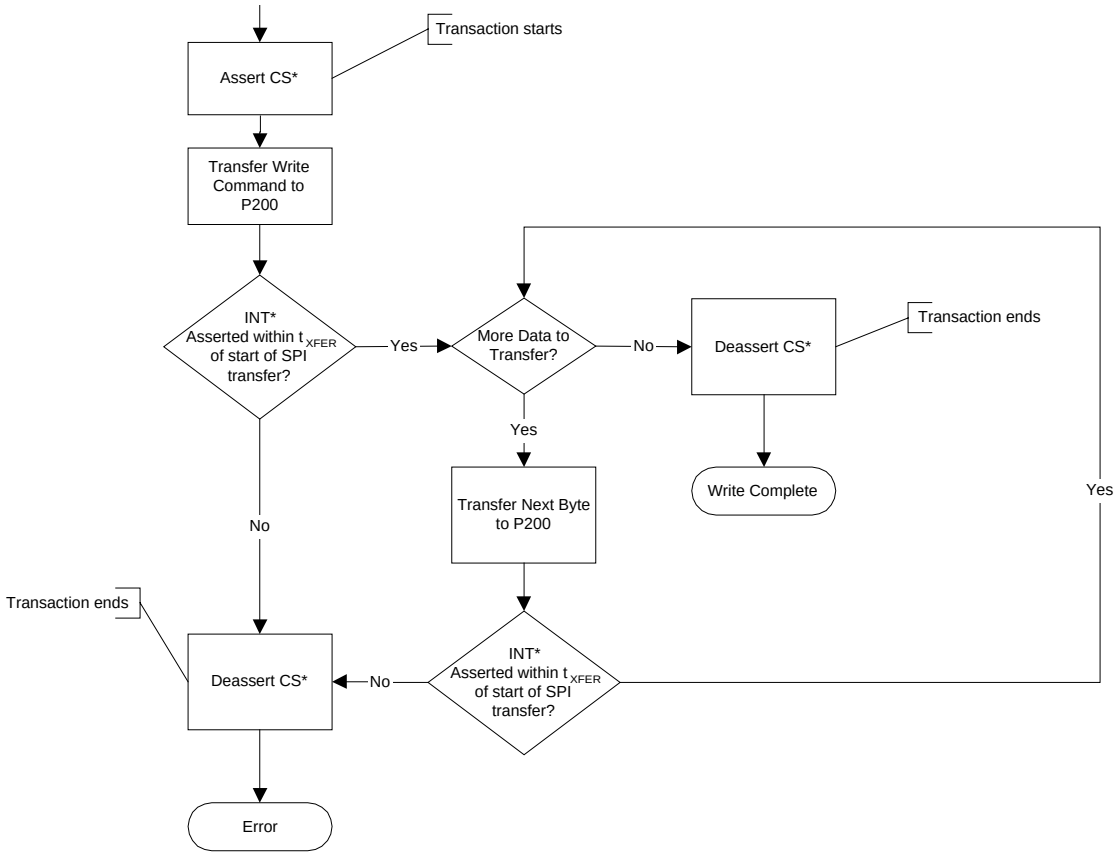


Figure 3. Write Transaction Flow Diagram

Read Transaction Flow

The following steps in Figure 4 should be taken to issue read commands and read data and status from the P200:

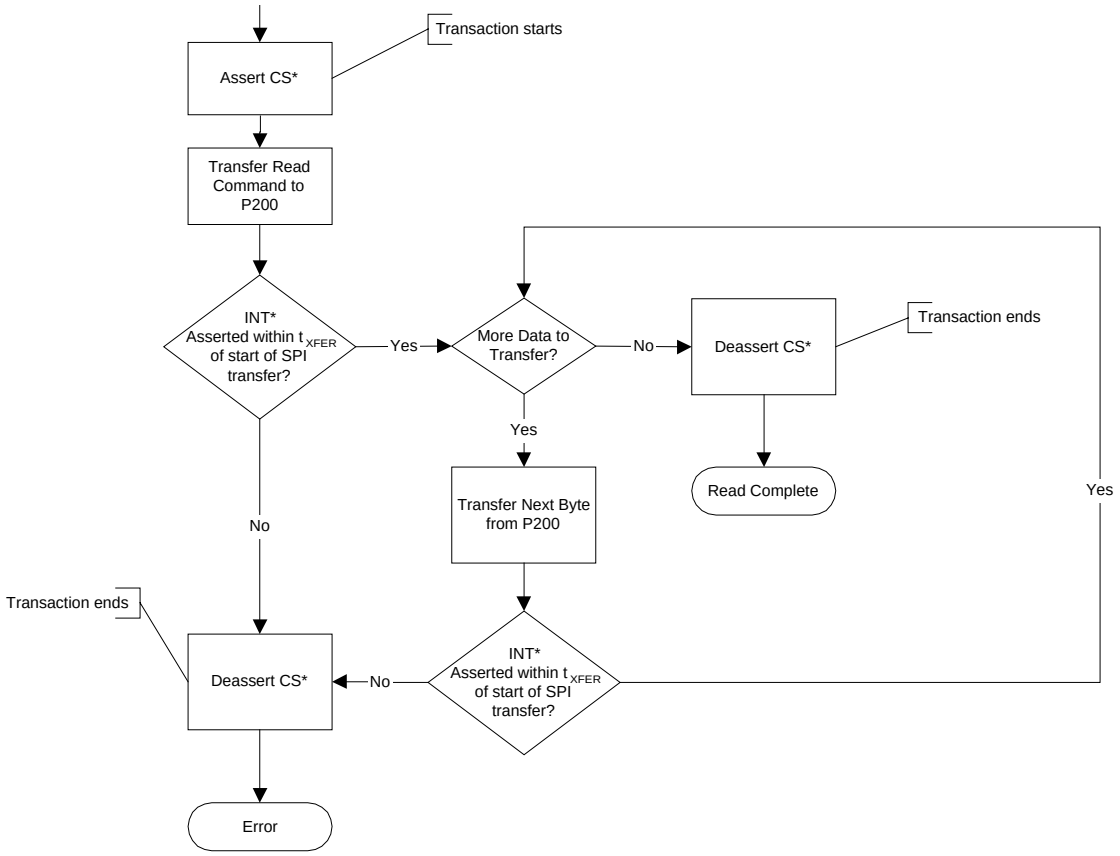


Figure 4. Read Transaction Flow Diagram

Attention Sequence Flow

An Attention request, as shown in Figure 5, is an unsolicited assertion of INT* and is used to inform the host that data or status is available:

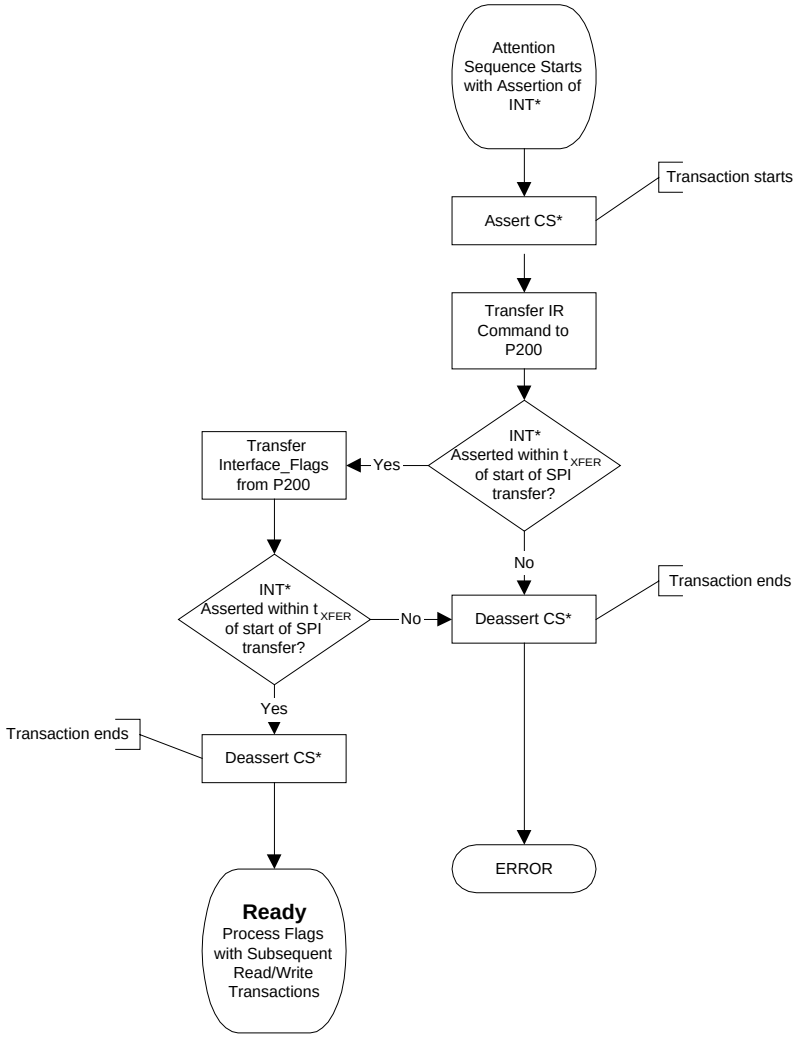


Figure 5. Attention Sequence Flow Diagram

Transaction Timing

Write Transaction Figures:

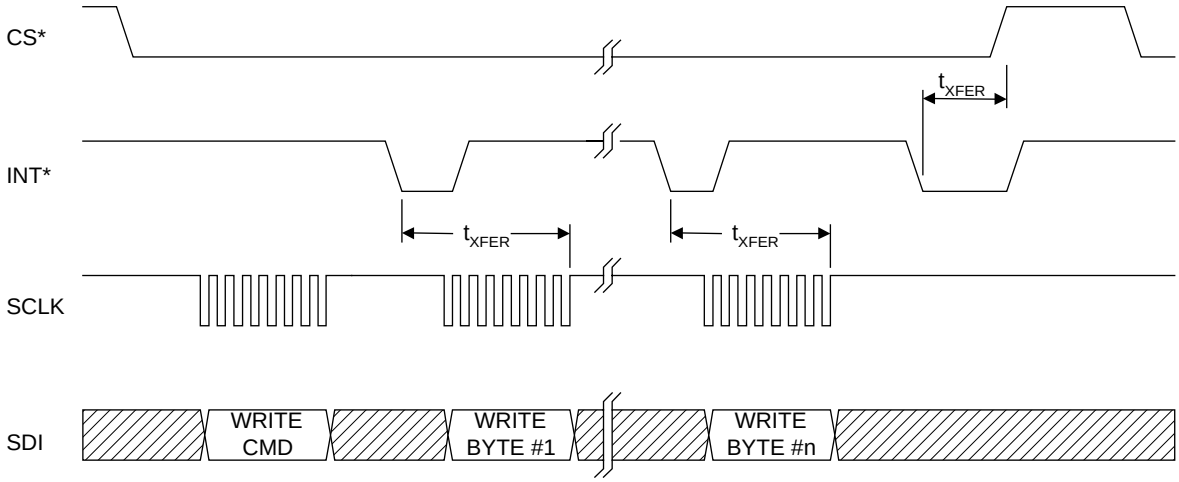


Figure 6. Write Transaction Timing Diagram

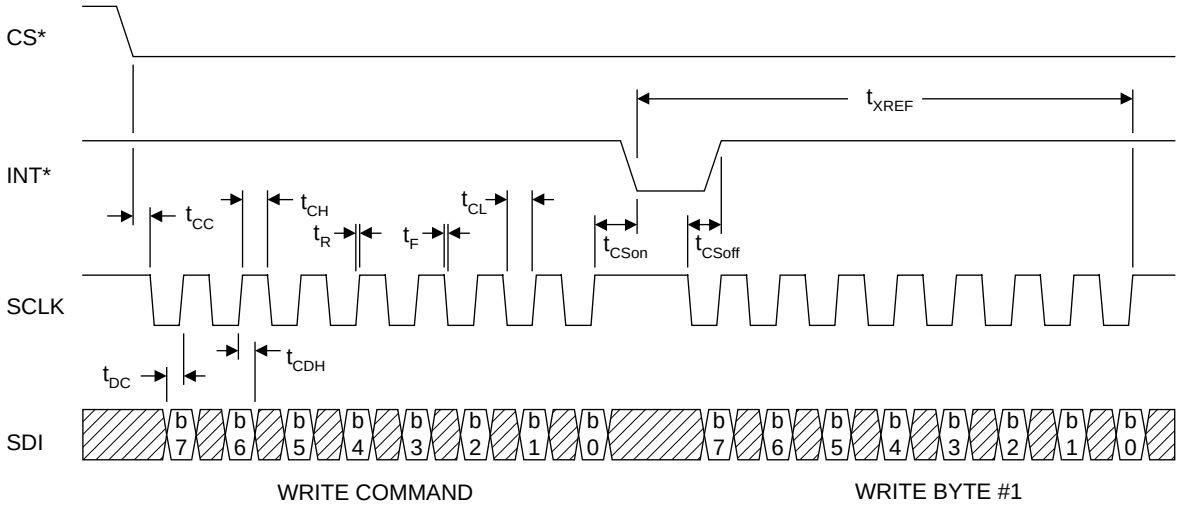


Figure 7. Write Byte #1 Timing Diagram

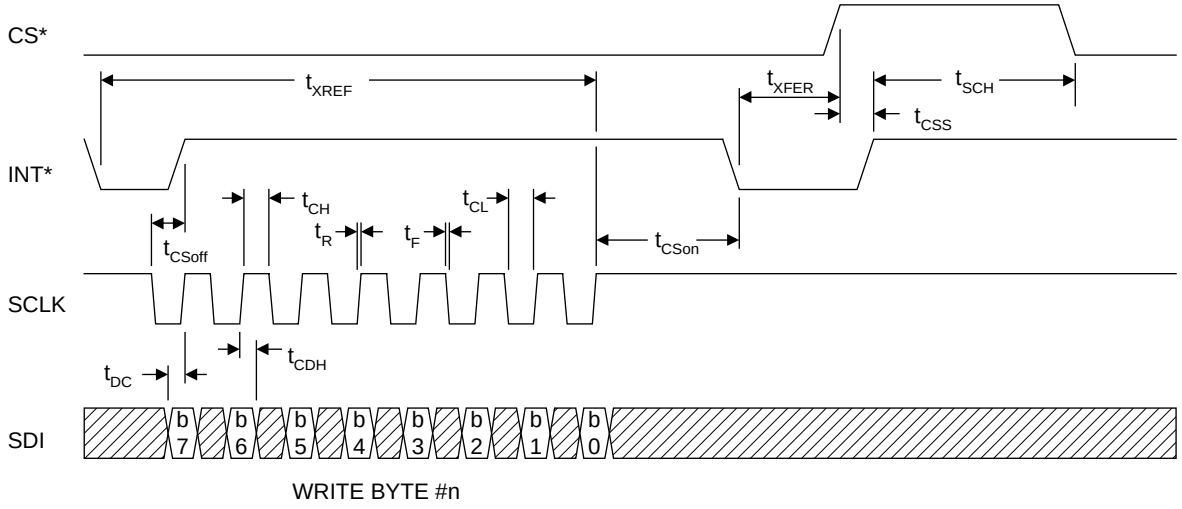


Figure 8. Write Byte #n Timing Diagram

Read Transaction Figures:

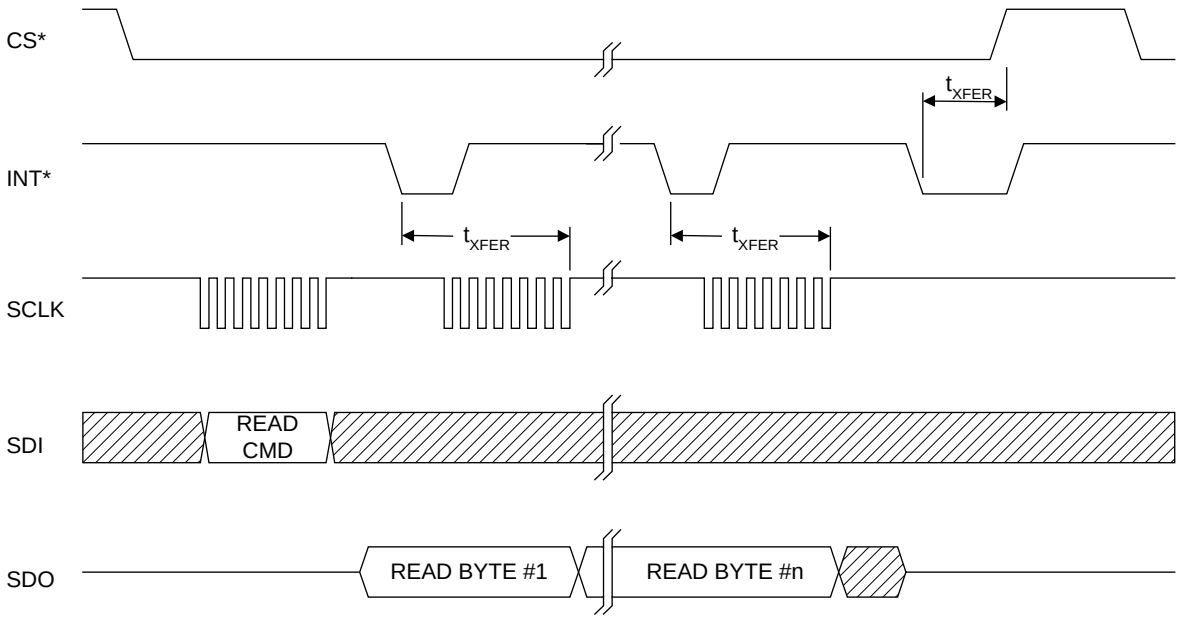


Figure 9. Read Transaction Timing Diagram

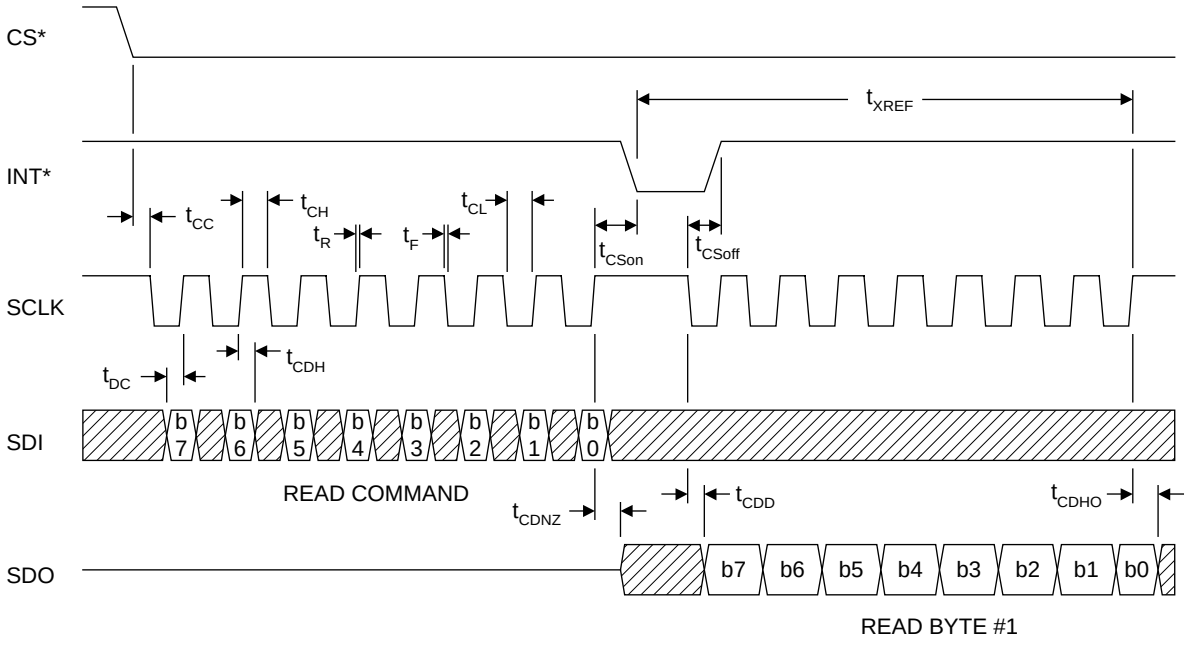


Figure 10. Read Byte #1 Timing Diagram

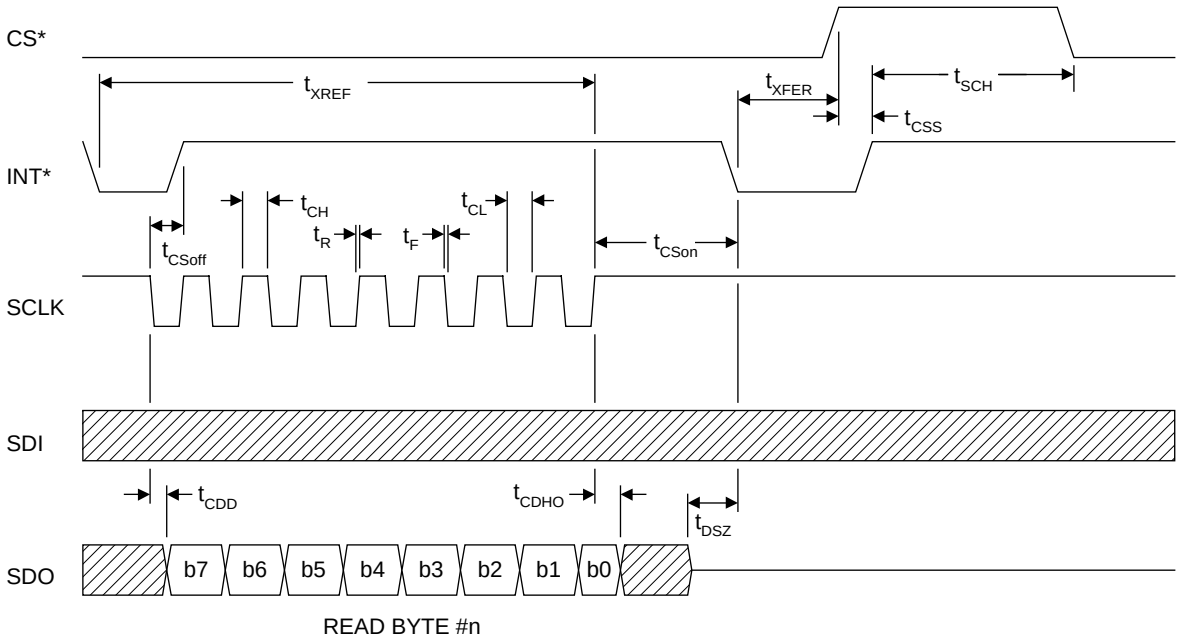


Figure 11. Read Byte #n Timing Diagram

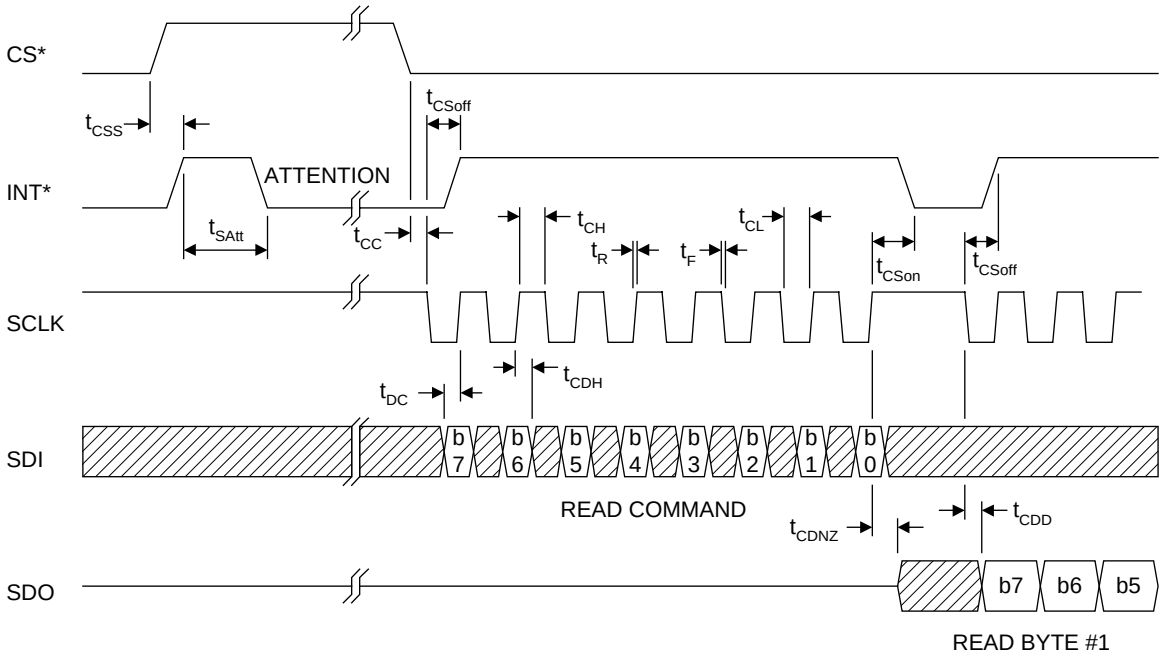


Figure 12. Attention/Read Byte #1 Timing Diagram

SPI Timing Parameters and Characteristics

Table 12. Timing Characteristics

(-40°C to 85°C; V_{CC}=5V)

Symbol	Parameter	Min	Max	Units	Notes
t_{RESET}	RESET to READY delay		10	msec	
t_{XFER}	Control Transfer Delay (1 msec typ.)		10	msec	
t_{SCH}	CS* Inactive Time	0		µsec	2
t_{CC}	CS* to SCLK Setup	50		nsec	2
t_{CL}	SCLK Low Time	250		nsec	2
t_{CH}	SCLK High Time	250		nsec	2
t_R, t_F	SCLK Rise and Fall		200	nsec	
t_{CSon}	SCLK to INT* Setup		500	µsec	1,2
t_{CSoff}	INT* to SCLK Delay		250	nsec	1,2
t_{DC}	SDI to SCLK Setup	50		nsec	1, 2
t_{CDH}	SCLK to SDI Hold	70		nsec	1, 2
t_{SAtt}	INT* Attention Delay	2		µsec	
t_{CSS}	CS* to INT* Delay		100	nsec	1, 2
t_{CDNZ}	SCLK to SDO Delay		500	µsec	1, 2, 3
t_{CDD}	SCLK to SDO Delay		100	nsec	1, 2, 3
t_{CDHO}	SCLK to SDO Hold	200		nsec	1, 2
t_{DSZ}	INT* to SDO High Z Setup		500	µsec	1, 2

NOTES:
1. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10msec rise maximum rise and fall time.
2. Measured with 50 pF load.
3. Measured at V_{OH}=2.4V or V_{OL}=0.4V.Modes

SSC P200 Mechanical Specifications

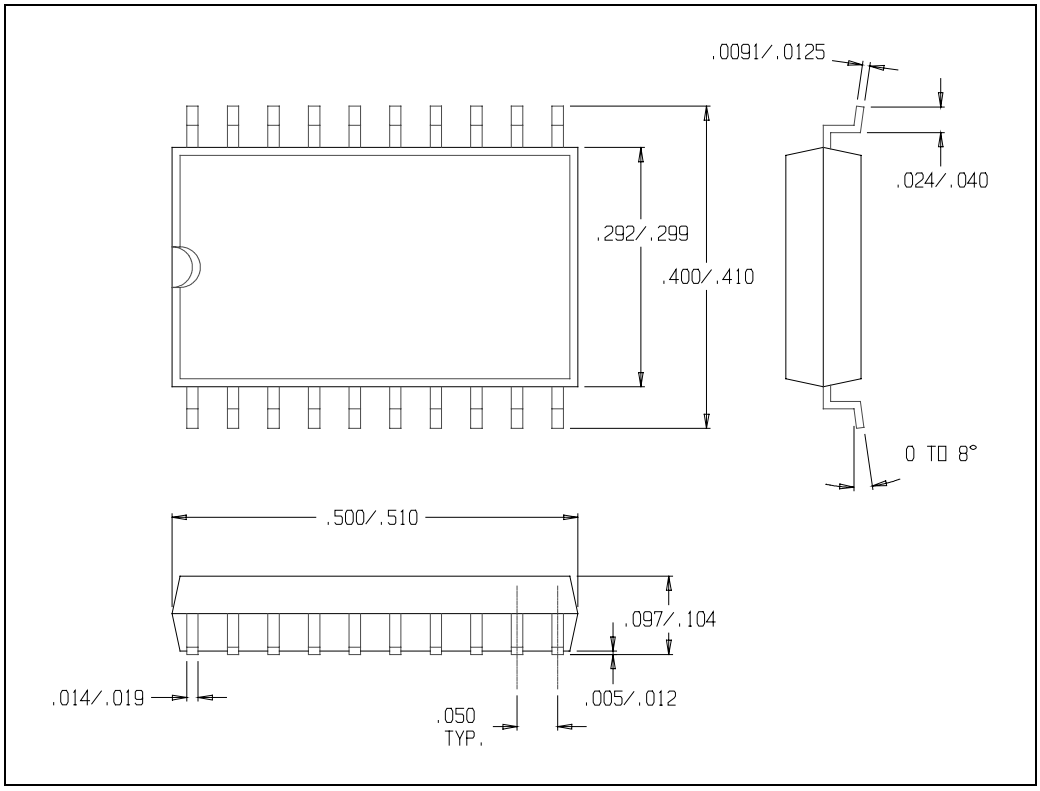


Figure 13. 20-Pin SOIC Package Outline

Ordering Information

SSC P200	PL Network Interface Controller

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