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MPC801

Product Brief

MPC801 Microprocessor

The MPC801 is derived from the MPC860 PowerQUICC™ integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It is a low-cost, general-purpose embedded PowerPC™ microprocessor that provides effective price/performance across a wide range of applications. The MPC801, like the MPC860, combines a high-performance PowerPC core with a multifaceted system integration package.

KEY FEATURES

The following is a list of the main features of the MPC801:

- Embedded PowerPC core with 52 MIPS at 40 MHz (using Dhrystone 2.1)
- Single-issue, 32-bit version of the embedded PowerPC core (fully compatible with the *PowerPC User Instruction Set Architecture (Book I)*) with 32 × 32-bit fixed-point registers
  - Embedded PowerPC core performs branch folding and branch prediction with conditional pre-fetch, but without conditional execution
  - 1K data cache and 2K instruction cache
  - Instruction and data caches are two way, set-associative, physical address, 4 word line burst, least recently used (LRU) replacement, lockable online granularity
  - MMUs with 8-entry TLB, fully associative instruction and data TLBs
  - MMUs support 4K, 16K, 512K and 8M page sizes; 16 virtual address spaces and 16 protection groups
  - Advanced on-chip emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8,16, and 32 bits controlled by memory controller)
- 26 external address lines
- Complete static design (0–40 MHz operation)
- Memory controller (eight banks)
  - Contains complete dynamic random-access memory (DRAM) controller
  - Each bank can be a chip-select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM single in-line memory modules (SIMMs), static random-access memory (SRAM), electrically programmable read-only memory (EPROM), and FLASH EPROM.
  - DRAM controller programmable to support a wide range of sizes and speed DRAM memory.
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32K to 256M)
  - Selectable write protection

- System integration unit
  - — Bus monitor
  - — Software watchdog
  - — Periodic interrupt timer
  - — Low-power stop mode
  - — Clock synthesizer
  - — On-chip bus arbitration logic
  - — PowerPC decrementer
  - — PowerPC timebase
  - — RTC
  - — Reset controller
  - — IEEE 1149.1 test access port (JTAG)
- Interrupts
  - — Eight external interrupt request (IRQ0-7) lines
  - — Internal interrupt sources: SPI, I2C, UART1, UART2, TB, PIT, and RTC
- UART support
  - — Two UARTs
  - — Standard baud rates of 300 bps to 115.2 kbps with 16× sample clock
  - — External 1× clock for high-speed synchronous communication
  - — Flexible 5-wire serial interface
  - — Direct support of IrDA physical layer protocol
  - — 8-byte FIFOs for transmit and receive
  - — Programmable data format
  - — Seven or eight data bits plus parity
  - — Odd, even, no parity, or force parity error
  - — One or two stop bits
  - — Programmable channel modes (normal and local loopback)
  - — Parity, framing, and overrun error detection
  - — Generation and detection of break
  - — Robust receiver data sampling with noise filtering
  - — Eight maskable interrupts
  - — Low-power idle mode
- I^2C support
  - — Two-wire interface (SDA and SCL)
  - — Full-duplex operation
  - — Master or slave I^2C mode support
  - — Multi-master environment support
  - — Clock rate support at a maximum of 520 KHz (assuming a 25-MHz system clock)
  - — Local loopback capability for testing
- SPI support
  - — Four-wire interface (SPIMOSI, SPIMISO, SPICLK, and $\overline{\text{SPISEL}}$)
  - — Full-duplex operation
  - — 8- and 1-bit data character operation
  - — Back-to-back character transmission and reception support
  - — Master or slave SPI modes support
  - — Multi-master environment support
  - — Clock rates support at a maximum of 6.25 MHz in master mode and 12.5 MHz in slave mode (assuming a 25-MHz system clock)
  - — Independent programmable baud rate generator

— Programmable clock phase and polarity
— Open-drain output pins support multi-master configuration
— Local loopback capability for testing

- Low-power support
  — Full on–all units fully powered
  — Doze–core functional units disabled except timebase decrementer, PLL, memory controller, and RTC in low-power standby
  — Sleep–all units disabled except RTC and PIT (PLL active for fast wake-up)
  — Deep sleep–all units disabled (including PLL), except RTC and PIT
- Debug interface
  — Eight comparators (four operate on instruction address, two operate on data address, and two operate on data)
  — Supports = ≠ < > conditions
  — Each watchpoint can generate a breakpoint internally
- 3.3 V operation with 5-V TTL compatibility
- 256-pin ball grid array (BGA) package

The MPC801 is a combination of the embedded PowerPC core and integrated peripherals brought together to meet the demands of various communications and networking products. The MPC801 is comprised of six modules that all use the 32-bit internal bus:

- Embedded PowerPC core
- System integration unit
- Two UARTs
- I^2C
- SPI

The MPC801 block diagram is illustrated in Figure 1 below.

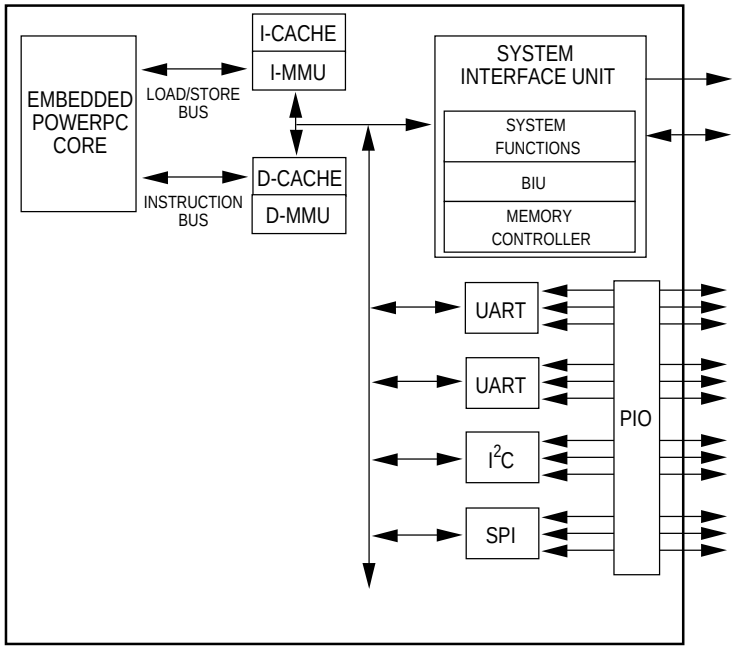

Figure 1. MPC801 Block Diagram

EMBEDDED POWERPC CORE

The embedded PowerPC core complies with the specifications discussed in *PowerPC User Instruction Set Architecture (Book I)*. The embedded PowerPC core has a fully static design that consists of two functional blocks—the integer block and load/store block. It executes all integer and load/store operations directly on the hardware. The core supports integer operations on a 32-bit internal data path with 32-bit arithmetic hardware. The interface to the internal and external busses is 32 bits.

The core uses a two instruction load/store queue, a four instruction prefetch queue, and a six instruction history buffer. It does branch folding and branch prediction with conditional pre-fetch, but does not support conditional execution. The core can operate on 32-bit external operands with one bus cycle. The PowerPC integer block supports 32×32-bit fixed-point general-purpose registers and executes one integer instruction per clock cycle.

The embedded PowerPC core is integrated with the MMUs as well with the 2K instruction cache and 1K data cache. Each MMU provides an 8-entry, fully associative instruction and data TLB, with 4K, 16K, 512K, and 8M page sizes. It supports 16 virtual address spaces with 16 protection groups. Three special registers are available as scratch registers to support software tablewalk and update.

The instruction cache is 2K, two way, set associative with physical addressing. It allows single cycle access on hit with no added latency for miss. It has four words per line supporting burst line fill using least recently used (LRU) replacement. The cache can be locked on a per line basis for application critical routines. The cache inhibit mode can be programmed on a per MMU page basis.

The data cache is 1K, two way, set associative with physical addressing. It allows single cycle access on hit with one added clock latency for miss. It has four words per line, supporting burst line fill using LRU replacement. The cache can be locked on a per line basis for application critical data. The data cache can be programmed to support copyback or writethrough via the MMU. The cache inhibit mode can be programmed on a per MMU page basis. The PowerPC core, together with its instruction and data caches, delivers approximately 52 MIPS at 40 MHz using Dhrystone 2.1.

The PowerPC core contains an improved debug interface that provides superior debug capabilities without causing any degradation in the speed of operation. This interface supports six watchpoint pins that are used to detect software events. Internally, it has eight comparators, four of which operate on the effective address of the address bus. The remaining four comparators are split. Two comparators operate on the effective address of the data address bus and two operate on the data bus. The core can compare using the =, ≠, <, and > conditions to generate watchpoints. Then each watchpoint can generate a breakpoint that can be programmed to trigger after a certain number of events.

SYSTEM INTERFACE UNIT

The system interface unit (SIU) on the MPC801 integrates general-purpose features useful in almost any 32-bit processor system, thus enhancing the performance provided by the system integration module on the MC68360 QUICC device. Multiple bus port sizes are supported and bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode. Data parity is supported using 4-bit data parity pins and the parity type can be odd or even. The SIU also contains power management functions, reset control, decrementer, timebase, and real-time clock.

The memory controller manages memories with a nonmultiplexed address bus (SRAM, SSRAM, EPROM, flash EPROM, and other peripherals) using the SRAM interface. Using the DRAM interface, the memory controller also manages memories with a multiplexed address bus (DRAM, SRDRAM, and EDO). Both submodules support glueless interface to 8-, 16-, and 32-bit wide memories. The memory controller supports up to eight memory banks and can use address type matching to qualify the memory bank accesses. Each bank can use either the SRAM or DRAM interface. The memory controller provides four byte enable signals, one output enable signal, and one boot chip-select available at reset.

The SRAM interface provides block sizes that vary between 32K to 64MB. Each bank of memory has 0 to 30 wait states (zero wait state means a two-clock access to external SRAM). The DRAM interface supports 256K, 512K, 1M, 2B, 4M, 8M, 16M, 32M, or 64M memory bank depths for all port sizes. The memory depth can be defined as 64K and 128K for 8-bit memory or 128M and 256M for 32-bit memory. The DRAM controller supports page mode access for successive transfers within bursts.

The MPC801 supports a glueless interface to one bank of DRAM, but external buffers are required for additional memory banks. The refresh unit provides CAS before RAS, a programmable refresh timer, disable refresh mode, and stacking for seven refresh cycles. The DRAM interface uses a programmable state machine to support most memory interfaces.

COMMUNICATION CHANNELS A AND B

Each communication channel has a full-duplex universal asynchronous receiver/transmitter (UART). The operating frequency for each receiver and each transmitter can be selected independently from the baud rate generator, counter/timer, or external clock. The transmitter accepts parallel data from the CPU, converts it to a serial bitstream, inserts the appropriate start, stop, and optional parity bits, and then outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for a start bit, stop bit, parity bit (if any), or break condition, and transfers an assembled character to the CPU during read operations.

I²C CONTROLLER

The I^2C controller is a synchronous, multimaster bus that is used to connect several integrated circuits on a board. It uses two wires (serial data and serial clock) to carry information between the integrated circuits that are connected to the bus. The I^2C controller consists of transmitter and receiver sections, an independent baud rate generator, and a control unit. The transmitter and receiver sections use the same clock that is derived from the I^2C controller baud rate generator in master mode and generated externally in slave mode.

SPI CONTROLLER

The serial peripheral interface (SPI) is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock and slave select). The SPI block consists of transmitter and receiver sections, an independent baud rate generator, and a control unit. The transmitter and receiver sections use the same clock that is derived from the SPI baud rate generator in master mode and generated externally in slave mode. During an SPI transfer, data is simultaneously transmitted and received.

POWER MANAGEMENT

The MPC801 supports a wide range of power management features, including full-on, doze, sleep, deep sleep, and low-power stop. In full-on mode, the MPC801 processor is fully powered with all internal units operating at full speed. A gear mode is provided (determined by a clock divider) that allows the operating system to reduce the operational frequency of the processor. Doze mode disables core functional units (except for the timebase, decrementer, PLL, memory controller, and RTC). Sleep mode disables everything, except the RTC and PIT, thus leaving the PLL active for quick wake-up. The deep sleep mode disables the PLL for low-power, but at the expense of a slower wake-up. Low-power stop disables all logic in the processor (except the minimum logic required to restart the device) and lowers the power consumption, but it also requires the longest wake-up time.

MPC801 APPLICATIONS

The MPC801 device is specifically designed to be a general-purpose, low-cost entry point to the embedded PowerPC Family at Motorola. The device excels in applications that require the performance of a single-issue PowerPC core with moderate amounts of data and instruction cache. It can support alternate bus masters in addition to providing all the basic features of glueless memory connections, but does not provide a wealth of serial connectivity. Instead, it supplies simple UART serial channels as well as I^2C and SPI channels for onboard communication to other peripheral chips.

The MPC801 excels in low-power and portable applications due to its expansive power-down modes. In addition, the normal operation current is low. The MPC801 is ideal for applications where a significant portion of the user's added value is in peripherals or ASICs and a low-cost general-purpose CPU is required. The programmable flexibility of the memory controller ensures that the board design can accommodate future memory types without hardware changes, thus enabling the ASIC to concentrate on other system goals.

DIFFERENCES BETWEEN THE MPC801 AND THE MPC860

The MPC801 can be considered a subset of the standard MPC860 device. The following modifications were made to the MPC860 to create the MPC801:

- 4K instruction cache reduced to 2K
- 4K data cache reduced to 1K
- 32-bit instruction and data TLBs reduced to eight TLB entries each
- 32-bit address bus reduced to 26 bits
- PCMCIA support eliminated
- All existing serial interface logic (including their respective DMAs) replaced with two UARTs, one I^2C and an SPI (all non-DMA based). The UARTs are modeled after the MC68328 DragonBall™.

MPC801 GLUELESS SYSTEM DESIGN

A fundamental design goal of the MPC801 was to have a flexible interface to other system components. Figure 2 shows a system configuration that offers one flash EPROM and supports DRAM SIMM and one SRAM. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

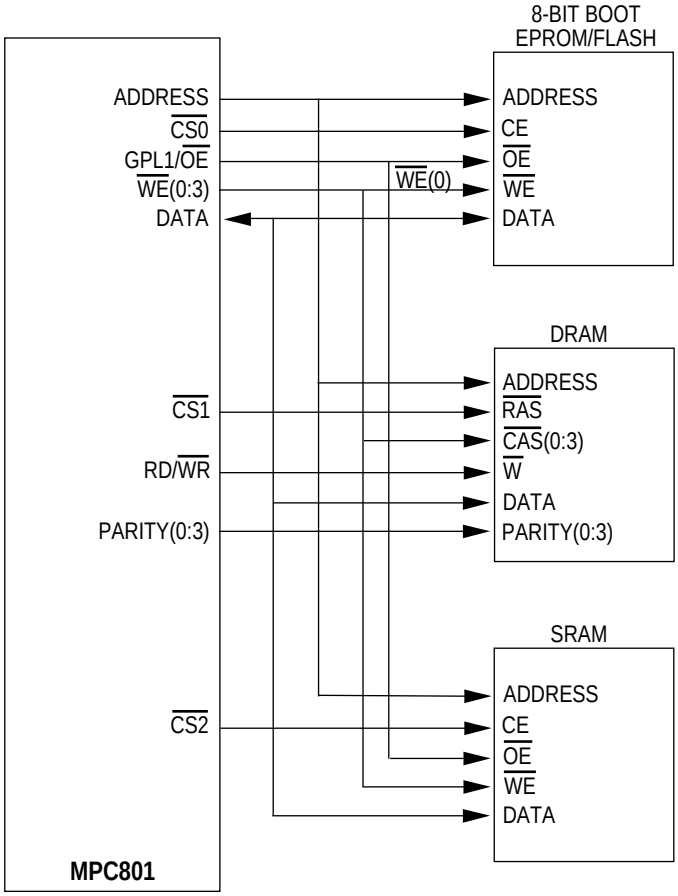

Figure 2. MPC801 System Configuration

ORDERING INFORMATION

The following table identifies the packages and operating frequencies available for the MPC801.

Table 1. MPC801 Package/Frequency Availability

PACKAGE TYPE	FREQUENCY (MHZ)	TEMPERATURE	ORDER NUMBER
Ball Grid Array (ZP Suffix)	25 40	0 to 70°C 0 to 70°C	XPC801ZP25 XPC801ZP40
Ball Grid Array (CZP Suffix)	TBD	-40°C to 85°C	TBD

The documents listed in the following table contain detailed information about the MPC801.

Table 2. MPC801 Documentation

DOCUMENT TITLE	ORDER NUMBER	CONTENTS
MPC801 Reference Manual	MPC801RM/AD	Detailed information for design
MPC860 User's Manual	MPC860UM/AD	Detailed information for design
PowerPC Microprocessor Family: The Programming Environments	MPCFPE/AD	PowerPC programmer’s reference

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.