

# FMS9884A

## Graphics Digitizer

**3x8-Bit, 108/140/175 Ms/s Triple Video A/D Converter with Clamps**

### Features

- 3-channels
- 100/140/175 Ms/s conversion rate
- Programmable Clamps
- Adjustable Gain and offset
- Internal Reference Voltage
- I<sup>2</sup>C/SMBus compatible Serial Port
- Pin Compatible with AD9884A

### Applications

- Flat panel displays and projectors
- RGB Graphics Processing

### Description

As a fully integrated analog interface, the FMS9884A can digitize RGB graphics with resolutions up to 1600 x 1200/65Hz refresh or 1600 x 1200/85Hz using alternate pixel sampling. ADC sampling clock can be derived from either an external source or incoming horizontal sync signal using the internal PLL. Output data is released through either one port at full rate or both ports, each running at half-rate. Setup and control

is via registers, accessible through an SMBus/I<sup>2</sup>C compatible serial port.

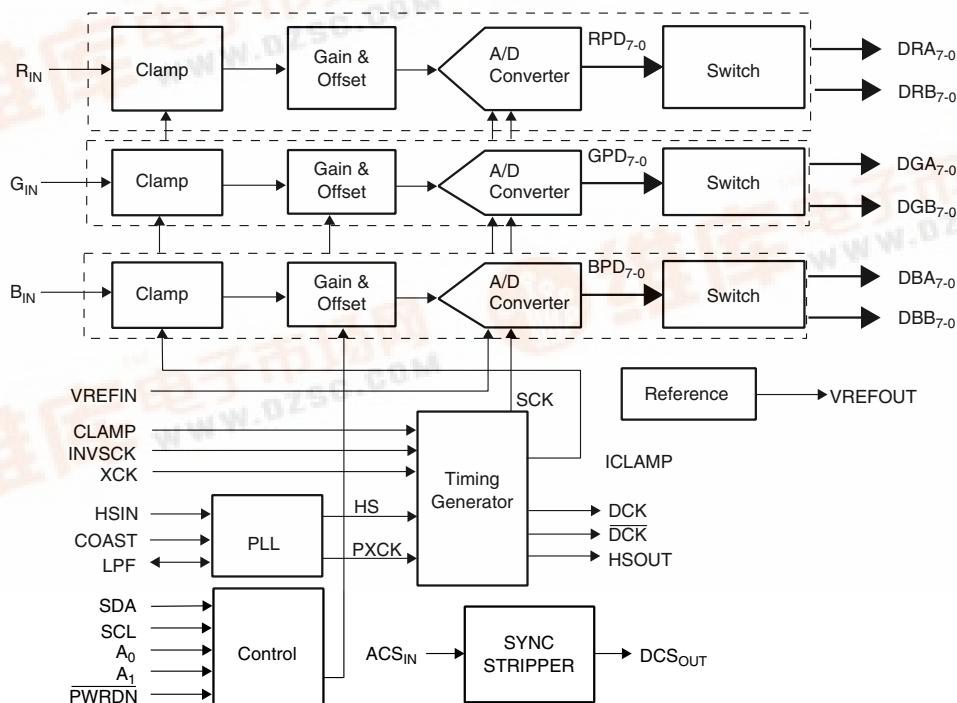
Input amplitude range is 500–1000mV with either DC or AC coupling. Lower reference of AC coupled inputs is established with input clamps that are either internally generated or externally provided.

Common to the three channels are clamp pulses, a bandgap reference voltage and clocks derived from a PLL or an external source. Digital data levels are 2.5–3.3 volt CMOS compliant.

Power can be derived from a single +3.3 Volt power supply. For 175 MHz applications see special V<sub>PLL</sub> requirements. Package is a 128-lead MQFP. Performance specifications are guaranteed over 0°C to 70°C range.

| Product Number | Speed    |
|----------------|----------|
| FMS9884AKAC100 | 108 Ms/s |
| FMS9884AKAC140 | 140 Ms/s |
| FMS9884AKAC175 | 175 Ms/s |

### Block Diagram



## Architectural Overview

Three separate digitizer channels are controlled by common timing signals derived from the Timing Generator. A/D clock signals can be derived from either a PLL or an external clock XCK. With the PLL selected, A/D clocks track the incoming horizontal sync signal connected to the HSIN input. Setup is controlled by registers that are accessible through the serial interface.

## Conversion Channels

Typical RGB graphics signals,  $R_{IN}$ ,  $G_{IN}$ ,  $B_{IN}$  are ground referenced with 700mV amplitude. If a sync signal is embedded then the usual format is sync on green with the sync tip at ground, the black level elevated to 300mV and peak green at 1000mV.

AC coupled video signals must be level shifted to establish the lower level of the conversion range by clamping to the black level of the back porch (see Figure 1). Clamp pulses are derived from internal Timing and Control logic or from the external CLAMP input.

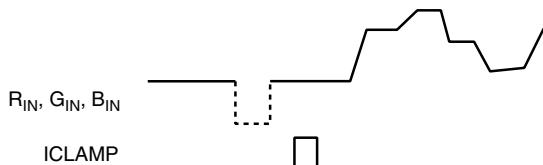


Figure 1. Clamping to the back-porch

## Gain and Offset

Gain and Offset registers serve two functions: adjustment of contrast and brightness by setting RGB values in tandem; matching the gain and offsets between channels, by setting RGB values individually to obtain the same output levels.

A/D conversion range can be matched to the amplitude of the incoming video signal by programming Gain Registers GR, GG and GB, which vary sensitivity (LSB/volt) over a 2:1 range. Incoming video signal amplitudes varying from 0.5 to 1.0 volt can be accommodated.

Input offset voltage of each converter is programmable in 1 LSB steps through the 6-bit OSR, OSG and OSB registers. Range of adjustment is equivalent to -31 to +32 LSB.

## A/D Converter

Each A/D converter digitizes the analog input into 8-bit data words. Latency is  $5-6\frac{1}{2}$  clock cycles, depending upon the data out format.

$V_{REFIN}$  is the source of reference voltage for the three A/D converters.  $V_{REFIN}$  can be connected to either the internal bandgap voltage,  $V_{REFOUT}$  or an external voltage.

## Output Data Configuration

Output data number format for each channel is binary: 00 corresponds to the lowest input; FF corresponds to the highest input. Data can be released in either of two timing formats:

1. Single 8-bit port at pixel rates up to 175Ms/s.
2. Dual 8-bit ports, each running at half the conversion rate. Maximum rate is 88Ms/s per port. Data streams may be parallel or interleaved.

## Timing and Control

Timing and Control logic encompasses the Timing Generator, PLL and Serial Interface.

### Timing Generator

All internal clock and synchronization signals are generated by the Timing Generator. Master Clock source is either the PLL or the external clock input, XCK. Bit XCKSEL selects the Master Clock source. Two clocks are generated.

Sampling clock, SCK is supplied to all three A/D converters. Phase of SCK can be adjusted in 32 11.25 degree phase increments using the 5-bit PHASE register.

DCK is the output data clock. DCK and  $\overline{DCK}$  are supplied as outputs for synchronizing data transfer from the digitizer outputs.

Horizontal sync applied to the input, HSIN is propagated by the Timing and Control to the HSOUT output with a delay that aligns leading and trailing edges with the output data.

### Phase Locked Loop

With a horizontal sync signal connected to the HSIN input pin, the PLL generates a high frequency internal clock signal, PXCK that is fed to the Timing and Control logic. Frequency of PXCK is set by the register programmable PLL divide ratio, PLLN.

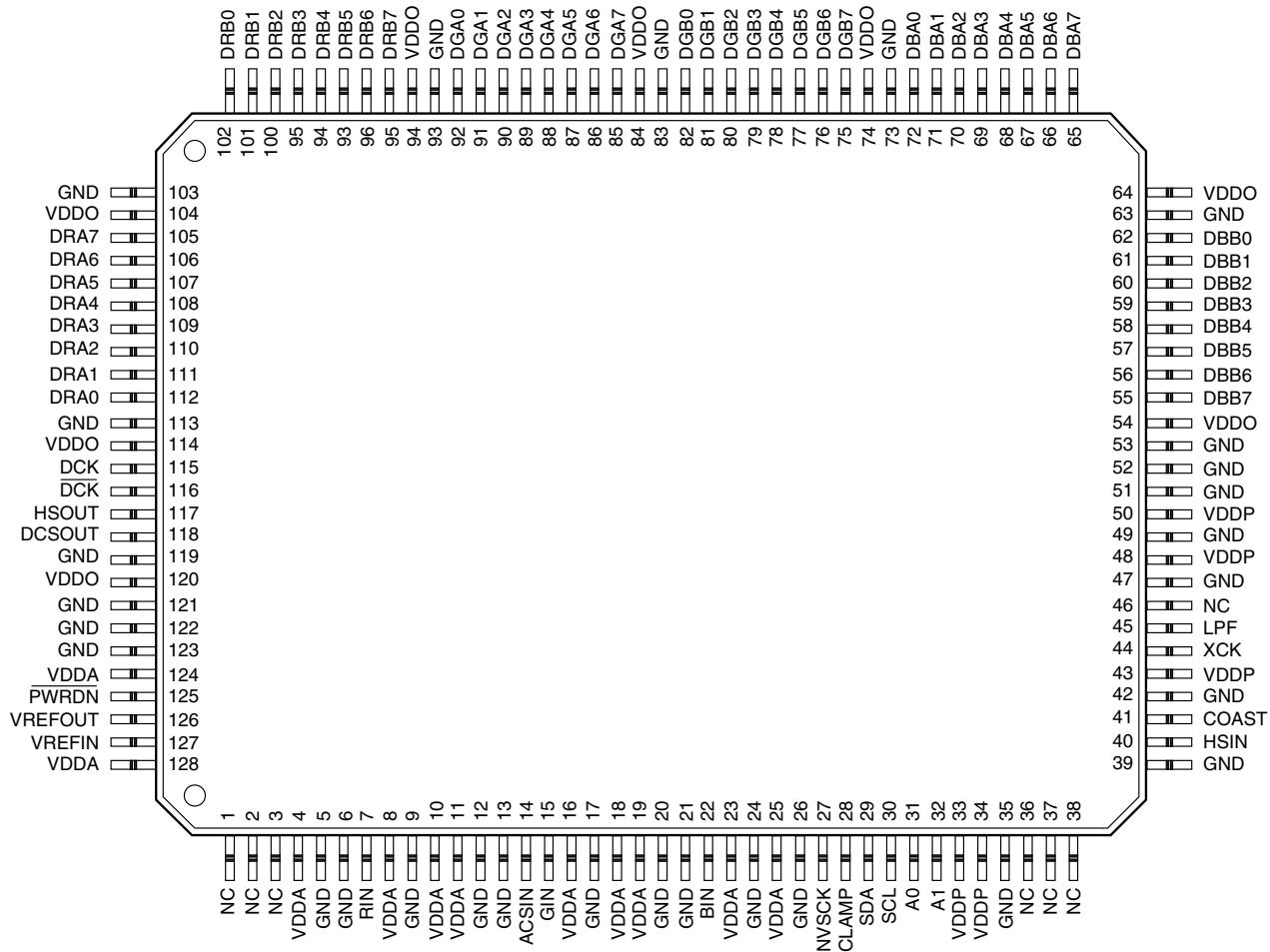
COAST is an input that disables the PLL lock to the horizontal sync input, HSIN. If HSIN is to be disregarded for a period such as the vertical sync interval, COAST allows the VCO frequency to be maintained. Omission of horizontal sync pulses during the vertical interval can cause tearing at the top of a picture, if COAST is not used.

Two pixels per clock mode is set by programming the PLL to half the pixel rate. By toggling the INVCK pin between frames, even and odd pixels can be read on alternate frames.

## Serial Interface

Registers are accessed through an I<sup>2</sup>C/SMBus compatible serial port. Four serial addresses are pin selectable.

## Pin Assignments (128-Lead MQFP (KA) Package)



## Pin Assignments

| No. | Name              | No. | Name             | No. | Name             | No. | Name                |
|-----|-------------------|-----|------------------|-----|------------------|-----|---------------------|
| 1   | NC                | 33  | V <sub>DDP</sub> | 65  | DBA <sub>7</sub> | 97  | DRB <sub>5</sub>    |
| 2   | NC                | 34  | V <sub>DDP</sub> | 66  | DBA <sub>6</sub> | 98  | DRB <sub>4</sub>    |
| 3   | NC                | 35  | GND              | 67  | DBA <sub>5</sub> | 99  | DRB <sub>3</sub>    |
| 4   | V <sub>DDA</sub>  | 36  | NC               | 68  | DBA <sub>4</sub> | 100 | DRB <sub>2</sub>    |
| 5   | GND               | 37  | NC               | 69  | DBA <sub>3</sub> | 101 | DRB <sub>1</sub>    |
| 6   | GND               | 38  | NC               | 70  | DBA <sub>2</sub> | 102 | DRB <sub>0</sub>    |
| 7   | R <sub>IN</sub>   | 39  | GND              | 71  | DBA <sub>1</sub> | 103 | GND                 |
| 8   | V <sub>DDA</sub>  | 40  | HSIN             | 72  | DBA <sub>0</sub> | 104 | V <sub>DDO</sub>    |
| 9   | GND               | 41  | COAST            | 73  | GND              | 105 | DRA <sub>7</sub>    |
| 10  | V <sub>DDA</sub>  | 42  | GND              | 74  | V <sub>DDO</sub> | 106 | DRA <sub>6</sub>    |
| 11  | V <sub>DDA</sub>  | 43  | V <sub>DDP</sub> | 75  | DGB <sub>7</sub> | 107 | DRA <sub>5</sub>    |
| 12  | GND               | 44  | XCK              | 76  | DGB <sub>6</sub> | 108 | DRA <sub>4</sub>    |
| 13  | GND               | 45  | LPF              | 77  | DGB <sub>5</sub> | 109 | DRA <sub>3</sub>    |
| 14  | ACS <sub>IN</sub> | 46  | NC               | 78  | DGB <sub>4</sub> | 110 | DRA <sub>2</sub>    |
| 15  | G <sub>IN</sub>   | 47  | GND              | 79  | DGB <sub>3</sub> | 111 | DRA <sub>1</sub>    |
| 16  | V <sub>DDA</sub>  | 48  | V <sub>DDP</sub> | 80  | DGB <sub>2</sub> | 112 | DRA <sub>0</sub>    |
| 17  | GND               | 49  | GND              | 81  | DGB <sub>1</sub> | 113 | GND                 |
| 18  | V <sub>DDA</sub>  | 50  | V <sub>DDP</sub> | 82  | DGB <sub>0</sub> | 114 | V <sub>DDO</sub>    |
| 19  | V <sub>DDA</sub>  | 51  | GND              | 83  | GND              | 115 | DCK                 |
| 20  | GND               | 52  | GND              | 84  | V <sub>DDO</sub> | 116 | ̄DCK                |
| 21  | GND               | 53  | GND              | 85  | DGA <sub>7</sub> | 117 | HS <sub>OUT</sub>   |
| 22  | B <sub>IN</sub>   | 54  | V <sub>DDO</sub> | 86  | DGA <sub>6</sub> | 118 | DCS <sub>OUT</sub>  |
| 23  | V <sub>DDA</sub>  | 55  | DBB <sub>7</sub> | 87  | DGA <sub>5</sub> | 119 | GND                 |
| 24  | GND               | 56  | DBB <sub>6</sub> | 88  | DGA <sub>4</sub> | 120 | V <sub>DDO</sub>    |
| 25  | V <sub>DDA</sub>  | 57  | DBB <sub>5</sub> | 89  | DGA <sub>3</sub> | 121 | GND                 |
| 26  | GND               | 58  | DBB <sub>4</sub> | 90  | DGA <sub>2</sub> | 122 | GND                 |
| 27  | INV SCK           | 59  | DBB <sub>3</sub> | 91  | DGA <sub>1</sub> | 123 | GND                 |
| 28  | CLAMP             | 60  | DBB <sub>2</sub> | 92  | DGA <sub>0</sub> | 124 | V <sub>DDA</sub>    |
| 29  | SDA               | 61  | DBB <sub>1</sub> | 93  | GND              | 125 | ̄PWRDN              |
| 30  | SCL               | 62  | DBB <sub>0</sub> | 94  | V <sub>DDO</sub> | 126 | V <sub>REFOUT</sub> |
| 31  | A <sub>0</sub>    | 63  | GND              | 95  | DRB <sub>7</sub> | 127 | V <sub>REFIN</sub>  |
| 32  | A <sub>1</sub>    | 64  | V <sub>DDO</sub> | 96  | DRB <sub>6</sub> | 128 | V <sub>DDA</sub>    |

## Pin Descriptions

| Pin Name  | Pin No.   | Type/Value     | Pin Function Description  |
|---|-----------|----------------|---|
| <b>Converter Channels</b>                           |           |                |   |
| R <sub>IN</sub> , G <sub>IN</sub> , B <sub>IN</sub> | 7, 15, 22 | Input          | <b>Analog Inputs.</b>   |
| DRA <sub>7-0</sub>                                  | 105–112   | Output         | <b>Red Channel Port A Data Output.</b> Full rate/half rate, interleaved/parallel data depending upon selected mode.   |
| DRB <sub>7-0</sub>                                  | 95–102    | Output         | <b>Red Channel Port B Data Output.</b> Active for dual port mode only with interleaved/parallel outputs. High impedance when inactive.  |
| DGA <sub>7-0</sub>                                  | 85–92     | Output         | <b>Green Channel Port A Data Output.</b> See red channel port A.  |
| DGB <sub>7-0</sub>                                  | 75–82     | Output         | <b>Green Channel Port B Data Output.</b> See red channel port B.  |
| DBA <sub>7-0</sub>                                  | 65–72     | Output         | <b>Blue Channel Port A Data Output.</b> See red channel port A.   |
| DBB <sub>7-0</sub>                                  | 55–62     | Output         | <b>Blue Channel Port B Data Output.</b> See red channel port B.   |
| <b>Timing Generator</b>                             |           |                |   |
| CLAMP   | 28        | Input          | <b>External Clamp Input.</b>  |
| INV SCK   | 27        | Input          | <b>Invert Sampling Clock.</b> Inverts SCK, the internal clock sampling the analog inputs. Supports Alternate Pixel Sampling mode for capture pixel rates up to 350Ms/s.                                       |
| XCK   | 44        | Input          | <b>External Clock input.</b> Enabled if register bit, XCKSEL = H. Replaces PXCK clock generated by PLL. If unused, connect to ground through a 10kΩ resistor.   |
| DCK   | 115       | Output         | <b>Output Data Clock.</b> Clock for strobing output data to external logic.   |
| ¬DCK  | 116       | Output         | <b>Output Data Clock Inverted.</b> Inverted clock for strobing output data to external logic.   |
| HSOUT   | 117       | Output         | <b>Horizontal Sync Output.</b> Reconstructed HSYNC delayed by FMS9884A latency and synchronized with DCK. Leading edge is synchronized to start of data output. Polarity is always active HIGH.               |
| <b>Phase Locked Loop</b>                            |           |                |   |
| HSIN  | 40        | Schmitt        | <b>Horizontal Sync input.</b> Schmitt trigger threshold is 1.5V. A 5V source should be clamped at 3.3V or current limited to prevent overdriving ESD protection diodes.                                       |
| COAST   | 41        | Input          | <b>PLL Coast.</b> Maintain frequency of PLL output clock PXCK, disregarding HSIN. If horizontal sync is missing during the vertical sync interval, PXCK clock frequency can be maintained by asserting COAST. |
| LPF   | 45        | Passive        | <b>PLL Low Pass Filter.</b> Connect recommended PLL filter to LPF pin. (see Figure 19.)   |
| <b>Sync Stripper</b>                                |           |                |   |
| ACS <sub>IN</sub>                                   | 14        |                | <b>Analog Composite Sync Input.</b> Input to sync stripper with 150mV threshold.  |
| DCS <sub>OUT</sub>                                  | 118       |                | <b>Digital Composite Sync Output.</b> Output from sync stripper.  |
| <b>Control</b>                                      |           |                |   |
| SDA   | 29        | Bi-directional | <b>Serial Port Data.</b> Bi-directional data.   |
| SCL   | 30        | Input          | <b>Serial Port Clock.</b> Clock input.  |
| A <sub>0</sub>                                      | 31        | Input          | <b>Address bit 0.</b> Lower bit of serial port address.   |
| A <sub>1</sub>                                      | 32        | Input          | <b>Address bit 1.</b> Upper bit of serial port address.   |
| PWRDN   | 125       | Input          | <b>Power Down/Output Control.</b> Powers down the FMS9884A and tri-states the outputs.  |

## Pin Descriptions (Continued)

| Pin Name                | Pin No.   | Pin Function Description   |
|-------------------------|---|--|
| <b>Power and Ground</b> |   |  |
| V <sub>DDA</sub>        | 4, 8, 10, 11, 16, 18, 19, 23, 25, 124, 128  | <b>ADC Supply Voltages.</b> Provide a quiet noise free voltage.  |
| V <sub>DDP</sub>        | 33,34,43,48,50  | <b>PLL Supply Voltage.</b> Most sensitive supply voltage. Provide a very quiet noise free voltage.                           |
| V <sub>DDO</sub>        | 54, 64, 74, 84, 94, 104, 114, 120   | <b>Digital Output Supply Voltage.</b> Decouple judiciously to avoid propagation of switching noise.                          |
| GND                     | 5, 6, 9, 12, 13, 17, 20, 21, 24, 26, 35, 39, 42, 47, 49, 51, 52, 53, 63, 73, 83, 93, 103, 113, 119, 121, 122, 123 | <b>Ground.</b> Returns for all power supplies. Connect ground pins to a solid ground plane.                                  |
| V <sub>REFIN</sub>      | 127   | <b>Voltage Reference Input.</b> Common reference input to RGB converters. Connect to VREFOUT, if internal reference is used. |
| V <sub>REFOUT</sub>     | 126   | <b>Voltage Reference Output.</b> Internal band-gap reference output. Tie to ground through a 0.1 $\mu$ F capacitor.          |

## Addressable Memory

### Register Map

| Name                 | Address | Function   | Default (hex) |
|----------------------|---------|--|---------------|
| PLL <sub>N11-4</sub> | 00      | <b>PLL divide ratio, MSBs.</b> PLLN + 1 = total number of pixels per horizontal line.  | 69 (1693)     |
| PLL <sub>N3-0</sub>  | 01      | <b>PLL divide ratio, LSBs.</b> PLLN + 1 = total number of pixels per horizontal line. PLLN <sub>3-0</sub> stored in the four upper register bits 7-4.<br><br>PLL <sub>N3-0</sub>   X   X   X   X | D0 (1693)     |
| GR <sub>7-0</sub>    | 02      | <b>Gain, red channel.</b> Adjustable from 70 to 140%.  | 80            |
| GG <sub>7-0</sub>    | 03      | <b>Gain, green channel.</b> Adjustable from 70 to 140%.  | 80            |
| GB <sub>7-0</sub>    | 04      | <b>Gain, blue channel.</b> Adjustable from 70 to 140%.   | 80            |
| OSR <sub>5-0</sub>   | 05      | <b>Offset, red channel.</b> OSR <sub>5-0</sub> stored in the six upper register bits 7-2. Default value is decimal 32.<br><br>OSR <sub>5-0</sub>   X   X   | 80            |
| OSG <sub>5-0</sub>   | 06      | <b>Offset, green channel.</b> OSG <sub>5-0</sub> stored in the six upper register bits 7-2. Default value is decimal 32.<br><br>OSG <sub>5-0</sub>   X   X                                       | 80            |
| OSB <sub>5-0</sub>   | 07      | <b>Offset, blue channel.</b> OSB <sub>5-0</sub> stored in the six upper register bits 7-2. Default value is decimal 32.<br><br>OSB <sub>5-0</sub>   X   X  | 80            |
| CD <sub>7-0</sub>    | 08      | <b>Clamp delay.</b> Delay in pixels from trailing edge of horizontal sync.   | 80            |
| CW <sub>7-0</sub>    | 09      | <b>Clamp width.</b> Width of clamp pulse in pixels.  | 80            |
| CONFIG1              | 0A      | <b>Configuration Register No. 1</b>  | F4            |

| Name                 | Address | Function  | Default (hex) |
|----------------------|---------|---|---------------|
| PHASE <sub>7-0</sub> | 0B      | <b>Sampling clock phase.</b> PHASE <sub>4-0</sub> stored in upper register bits 7-3. PHASE sets the sampling clock phase in 11.25° increments. Default value is decimal 16.<br><br>PHASE <sub>4-0</sub>   X   X   X | 80            |
| PLLCTRL              | 0C      | <b>PLL Control</b>  | 24            |
| CONFIG2              | 0D      | <b>Configuration</b>  | 00            |
|                      | 0E      | <b>Reserved</b>   | 0X            |
|                      | 0F      | <b>Reserved</b>   | 00            |

## Register Definitions

### Configuration Register 1 (0A)

| Bit no. | Name     | Type | Description  |
|---------|----------|------|--|
| 0       |          |      |  |
| 1       | XCKSEL   | R/W  | <b>External Clock Select.</b> Select internal clock source.<br>0: Internal PLL<br>1: XCK input.  |
| 2       | XCLAMPOL | R/W  | <b>External Clamp Polarity.</b> Select clamp polarity.<br>0: Active L.<br>1: Active H.   |
| 3       | XCLAMP   | R/W  | <b>External Clamp Select.</b> Select clamp source.<br>0: Internally generated by PLL referenced to HSIN.<br>1: External CLAMP input.   |
| 4       | COASTPOL | R/W  | <b>Coast Polarity.</b> Select COAST input polarity.<br>0: Active L.<br>1: Active H.  |
| 5       | HSPOL    | R/W  | <b>HSIN Polarity.</b> Select horizontal sync input polarity. PLL is locked to selected edge:<br>0: Falling edge.<br>1: Rising edge.  |
| 6       | PARALLEL | R/W  | <b>Output Data Format.</b> Select format of data outputs.<br>0: Interleaved. DCK rising edge strobes port A data. <u>DCK</u> rising edge strobes port B data.<br>1: Parallel. Rising edge of DCK strobes port A and port B data. |
| 7       | DEMUX    | R/W  | <b>Output Data Porting.</b> Data released at full rate through one port or through two half-rate ports.<br>0: Single 8-bit port.<br>1: Dual 8-bit ports.   |

### PLL Configuration Register (0C)

| Bit no. | Name                 | Type | Description   |
|---------|----------------------|------|---|
| 1-0     | —                    |      |   |
| 4-2     | IPUMP <sub>2-0</sub> | R/W  | <b>Charge Pump Current.</b> Selects Charge Pump current (µA).<br>(see Table 5. Charge Pump Current Codes)<br><b>000:</b> 50<br><b>001:</b> 100<br><b>010:</b> 150<br><b>011:</b> 250<br><b>100:</b> 350<br><b>101:</b> 500<br><b>110:</b> 750<br><b>111:</b> 1500 |

| Bit no. | Name                | Type | Description   |
|---------|---------------------|------|---|
| 6-5     | FVCO <sub>1-0</sub> | R/W  | <b>VCO Frequency Range.</b> Selects VCO frequency range (MHz).<br><b>00:</b> 20–90<br><b>01:</b> 20–90<br><b>10:</b> 80–120<br><b>11:</b> 110–175 |
| 7       | —                   | R/W  | <b>Reserved.</b><br><b>0:</b> Run.<br><b>1:</b> (reserved).   |

### Configuration Register 2 (0D)

| Bit no. | Name     | Type | Description   |
|---------|----------|------|---|
| 0       | —        | —    | <b>Reserved.</b> Set to 0.  |
| 3-1     | REV      | R    | <b>Revision Number.</b> Die revision number.  |
| 4       | OUTPHASE | R/W  | <b>Output Data Phase.</b> In the dual port mode, selects either odd (1, 3, 5, ...) or even (2, 4, 6, ...) samples following the HSYNC leading edge to be emitted from Port 1.<br><b>0:</b> Even samples to Port A, odd samples to Port B.<br><b>1:</b> Odd samples to Port A, even samples to Port B. |
| 7-5     | —        | R/W  | <b>Reserved.</b> Set to 00.   |

### Test Register (0F)

| Bit no. | Name | Type | Description  |
|---------|------|------|--|
| 7-0     | —    | R/W  | <b>Reserved.</b> After power-up, initialize this register with the default value 0x00. Register 0F does not respond with an acknowledge during serial bus access. Consequently, ACK remains H instead of being pulled H. |

## Functional Description

There are two major sections within the FMS9884A Digitizer:

1. Analog-to-digital Converter Channels, one for each channel, RGB and the voltage reference.
2. Timing and Control comprising the PLL, Timing Generator, Sync Stripper and Serial Interface.

## A/D Converter Channels

Each of the three RGB channels consists of:

1. A clamp to set the lower reference level of an AC coupled input.
2. Gain and offset stages to tune the converter to input signal levels.
3. An Analog-to-Digital Converter to digitize the analog input.
4. A commutating switch for dual port operation.

## Analog Inputs

Input signal range is 500 to 1000mV to support conversion of single-ended signals with a typical amplitude of 700mV p-p. With the clamp active, each input accommodates a negative 300mV excursion.

Inputs are optimized for a source resistance of 37.5 to 75Ω. To reduce noise sensitivity, the ultra-wide 500MHz input bandwidth may be reduced by adding a small series inductor prior to the 75Ω terminating resistor. See Applications Section.

## Clamps

If the incoming signals are not ground referenced, a clamp must be used to set the incoming video range relative to ground. Prior to each A/D converter, each channel includes a clamp that allows a capacitively coupled input to be referenced to the A/D converter bottom reference voltage when the clamp pulse is active. Source of the clamp signal is determined by the XCLAMP bit.

Internal clamp timing is generated by the Timing and Control Block. Position and width of the internal clamp pulse, ICLAMP are programmable through registers CD and CW. External clamp input is selected by register bit XCLAMP and the external clamp polarity selected through register bit XCLAMPOL. To disable the clamp for DC coupled inputs, set XCLAMP = 1 with either of these conditions:

1. XCLAMPOL = 0 with input CLAMP = H.
2. XCLAMPOL = 1 with CLAMP = L.

Best performance will be achieved with the clamp set active for most of the black signal level interval between the trailing edge of horizontal sync and the start of active video.

Insufficient clamping can cause brightness changes at the top of the image and slow recovery from large changes in Average Picture Level (APL). Recommended value of CD is 0x10 to 0x20 for most standard video sources.

### Analog-to-Digital Converter

Figure 2 is a block diagram of the ADC core with gain and offset functions.  $G_{7-0}$ ,  $OS_{5-0}$ ,  $RGB_{IN}$  and  $PD_{7-0}$  generically refer to the gain and offset register values, analog input and parallel data output of any RGB channel.

Core of the ADC block is a high speed A/D encoder with differential inputs. Within the A/D converter core are the following elements:

1. Differential track and hold.
2. Differential analog-to-digital converter.

Setting the gain register value  $G_{7-0}$  ( $GR_{7-0}$ ,  $GG_{7-0}$ ,  $GB_{7-0}$ ), establishes the gain D/A converter voltage which is the A/D reference voltage. Increasing video gain reduces the contrast of the picture since the number of output codes is reduced. Conversion range is defined by the gain setting according to Table 1.

**Table 1. Gain Calibration**

| $G_{7-0}$       | Conversion Range (mV) |
|-----------------|-----------------------|
| 0               | 500                   |
| 66 <sub>h</sub> | 700                   |
| FF <sub>h</sub> | 1000                  |

A/D Converter sensitivity is:

$$S = \frac{255}{500} \cdot \frac{255}{255 + G_{7-0}} \text{ LSB/mV}$$

Offset is set through the Single-Ended to Differential Amplifier which translates the ground referenced input to a differential voltage centered around A/D common mode bias voltage.

The 6-bit Offset D/A converter injects a current into  $R_{LEVEL}$  with two components:

1.  $I_{BIAS}$  to establish the A/D common mode voltage.
2.  $I_{OFFSET}$  to set the offset from the common mode level.

Voltage offset from the common mode voltage at the inverting input of the Track and Hold is:

$$V_{OS} = (OS_{5-0} - 31) \cdot \frac{255 + G_{7-0}}{255} \cdot \frac{500}{255}$$

D/A converter gain tracks A/D gain with 1 LSB of offset corresponding to 1 LSB of gain. Increasing  $OSR_{5-0}$ ,  $OSG_{5-0}$ , or  $OSB_{5-0}$  reduces brightness in the selected channel. Data output from the A/D converter is:

$$D_{7-0} = S \cdot V_{IN} - (OS_{5-0} - 31)$$

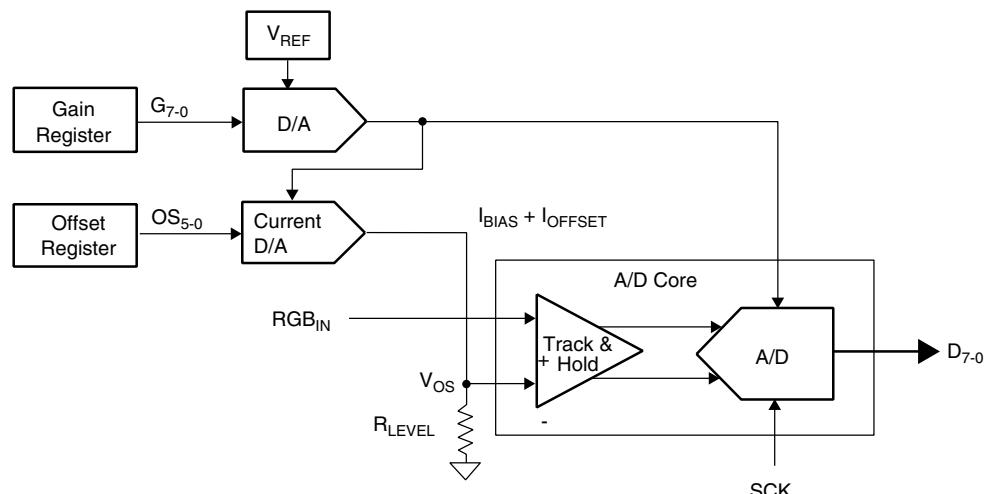
Impact of the offset values  $OSR_{5-0}$ ,  $OSG_{5-0}$ , and  $OSB_{5-0}$  is shown in Table 2.

**Table 2. Offset Calibration**

| $OS_{5-0}$      | Output Offset (decimal) |
|-----------------|-------------------------|
| 0               | +31                     |
| 1F <sub>h</sub> | 0                       |
| 3F <sub>h</sub> | -32                     |

### Sampling Clock PHASE Adjustment

Picture quality is strongly impacted by the  $PHASE_{4-0}$  value. If PHASE is not set correctly, any section of an image consisting of vertical lines may exhibit tearing.



**Figure 2. A/D Converter Architecture**

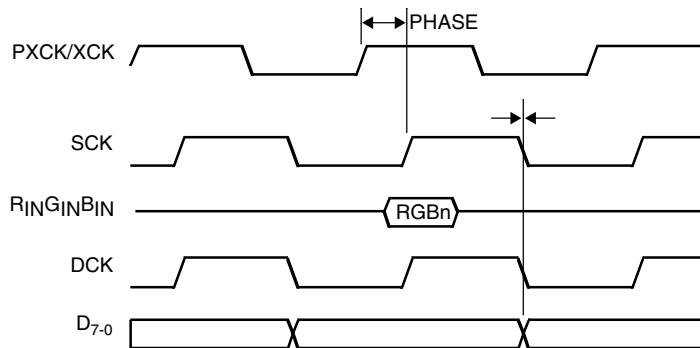


Figure 3. Internal Sampling Clock, SCK Timing

Figure 3 shows how an analog input,  $R_{IN}G_{IN}B_{IN}$  is sampled by the rising edge of SCK after a delay PHASE from the rising edge of either PXCK or XCK. SCK can be delayed up to 32 steps in  $11.25^\circ$  increments by adjusting the register value,  $PHASE_{4-0}$ .

Output data, DCK and  $\overline{DCK}$  are delayed in tandem with SCK relative to PXCK or XCK. There is a  $5-5\frac{1}{2}$  clock latency between the data sample  $RGB_n$  and the corresponding data out  $D_{7-0}$ .

Ideally, incoming pixels would be trapezoidal with fast rise-times and the sampling edge of the A/D clock, SCK would be positioned along the level section of the incoming pixel waveform as shown in Figure 4. There is a narrow zone of uncertainty where sampling during pixel rise time would cause an error in the value of the A/D data output,  $D_{7-0}$ , which is shown as a value, 0-255.

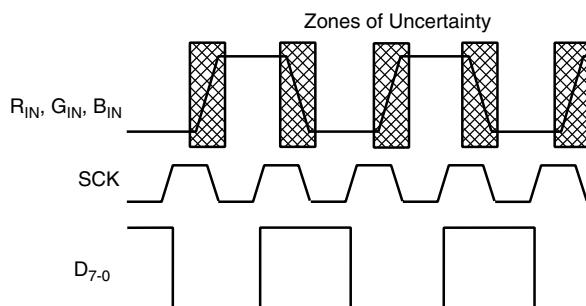


Figure 4. Ideal Pixel Sampling

In practice, high-resolution pixels have long rise-times. As shown in Figure 5, there are narrow zones of serendipity when the pixel amplitude is level. Samples are valid in these zones.

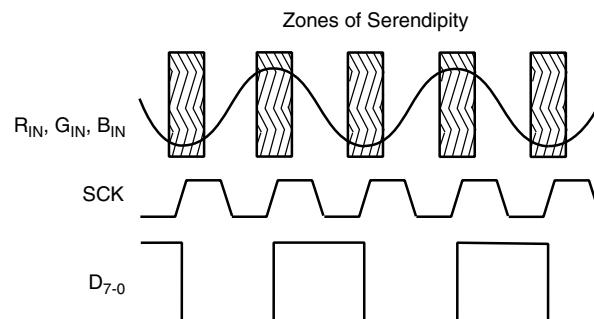


Figure 5. Acceptable Pixel Sampling

Referring to Figure 6, when the sample clock, SCK has some jitter, if the sampling edge occurs anywhere within the zone of uncertainty where the pixel rise time is steep, there will be amplitude modulation of the digitized data,  $D_{7-0}$ , due to the sampling clock jitter. To avoid corruption of the image, setting the value  $PHASE_{7-0}$  is critical.  $PHASE_{4-0}$  should be trimmed to position the sampling edge of SCK within the zone of serendipity.

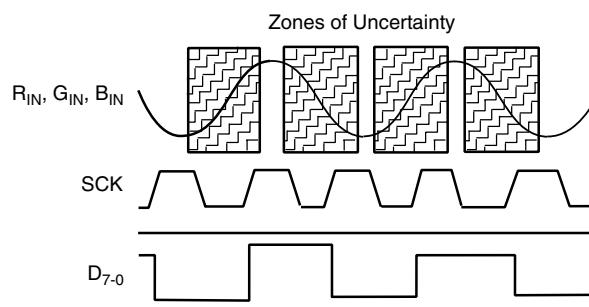


Figure 6. Improper Pixel Sampling

## Voltage References

An on-chip voltage reference is generated from a bandgap source.  $V_{REFOUT}$  is the buffered output of this source that can be connected to  $V_{REFIN}$  to supply a voltage reference that is common to the three converter channels.

$V_{REFIN}$ , with a nominal voltage of 1.25V, is the source of the differential reference voltages for each A/D converter. Reference voltages supplied to the differential inputs of the comparators in the A/D converters are derived from  $V_{REFIN}$ .

### Digital Data Outputs

Input horizontal sync, HSIN and outgoing data, D[7..0] are resynchronized to the delayed sample clock, SCK. Output timing characteristics are defined in Figure 7. Latency of the first pixel, N varies according to the mode:

1. Single or dual output port.
2. Interleaved or parallel output data.
3. 1-pixel or 2-pixel.

Levels are 3.3 volt CMOS with the output supply variable between 2.5 and 3.3 V.  $\overline{PWRDN} = L$  sets the outputs high-impedance.  $\overline{PWRDN} = H$  enables the outputs.

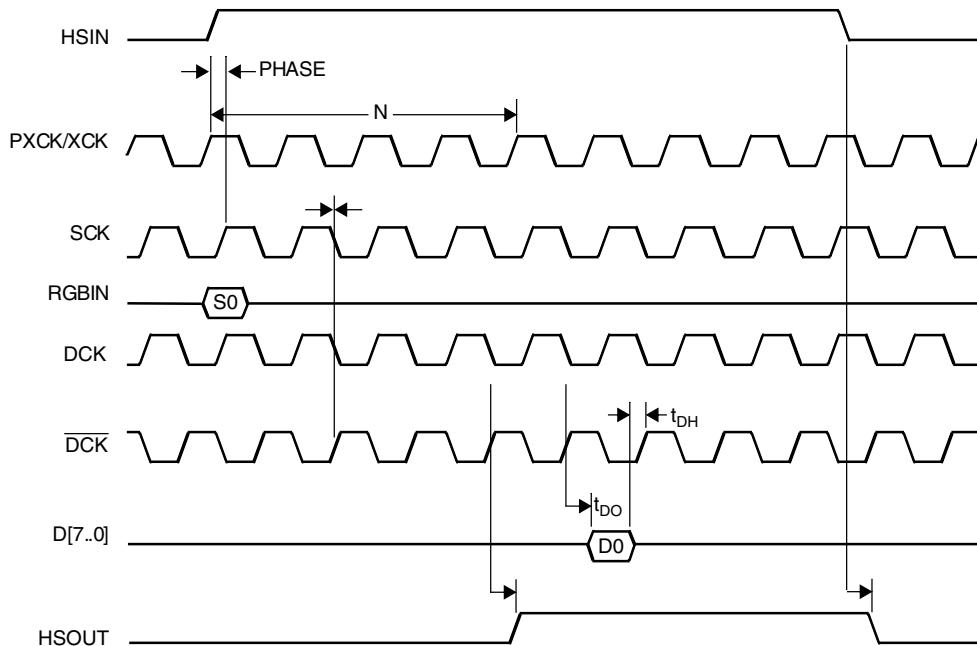


Figure 7. Output Timing

Figures 13 through 21 depict data output timing relative to the sampling clock and inputs for all modes. Timing is referenced to the leading edge of HSIN when the first sample is taken at the rising edge of SCK. Status of register bit OUT-PHASE, determines if even samples are directed the A-port and odd samples are directed to the B-port; or vice versa.

Note the timing of the HSOUT waveform:

1. HSOUT is always active HIGH.
2. Only the leading edge of HSOUT is active or selected by the HSPOL register bit.
3. HSOUT is aligned with DCK.
4. Trailing edge is linked to HSIN.
5. If HSIN does not terminate before mid-line, HSOUT is forced low. A 50% duty cycle indicates that HSPOL is incorrectly set.

HS is the internal sync pulse generated from HSYNC. SCK is the internal A/D converter sampling clock.

Output data transitions are synchronized with the falling edge of DCK. Output data should be strobed on the rising edge of DCK. A 5 to 6.5 clock cycle delay must be flushed before valid data is available.

### Alternate Pixel Sampling Mode

A logic H on the CKINV pin inverts the sampling phase of SCK. In the Alternate Pixel Sampling Mode:

1. PLL is run at half rate. SCK, DCK and  $\overline{DCK}$  are half rate.
2. CKINV is toggled between frames. (see Figure 18)

**Figure 8. Odd and Even Pixels in a Frame**

On one frame, even pixels are sampled. On the other, odd pixels are sampled.

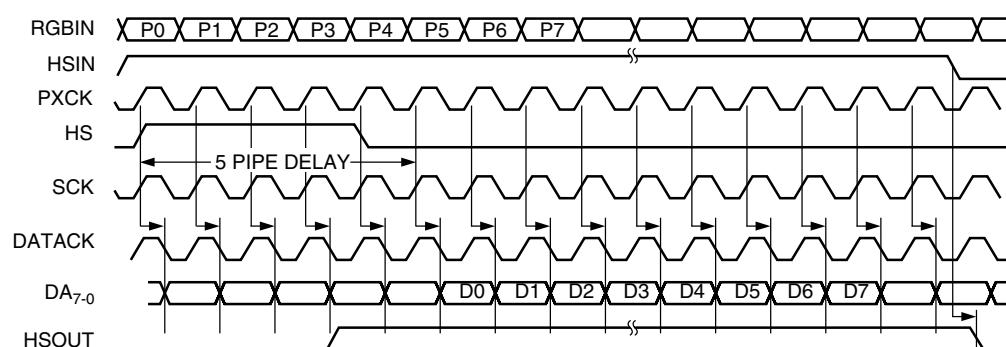
Alternate Pixel Sampling is similar to interlacing used in broadcast video, except that the columns of pixels are interlaced instead of lines.

**Figure 9. Odd Pixels from Frame 1**

**Figure 10. Even Pixels from Frame 2**

**Figure 11. Combined Frames 1 and 2 Output.**

**Figure 12. Subsequent Output Combining Frames 2 and 3**



**Figure 13. Single Port Mode**

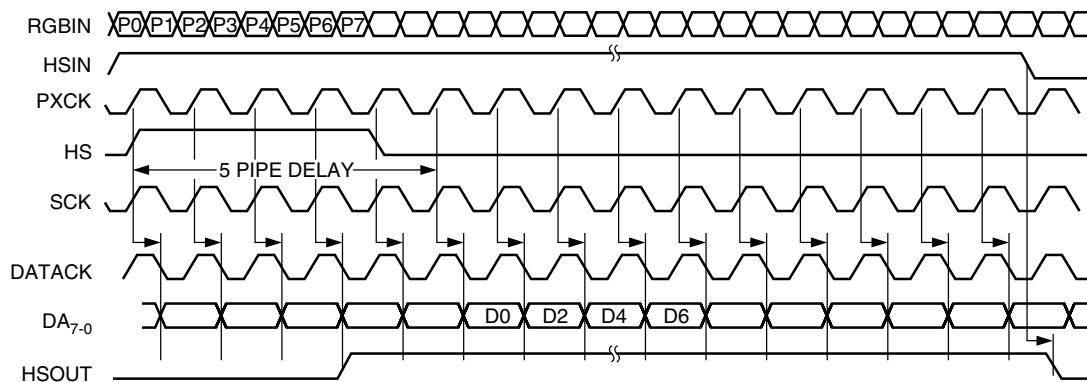


Figure 14. Single Port Mode, Alternate Pixel Sampling, (Even Pixels)

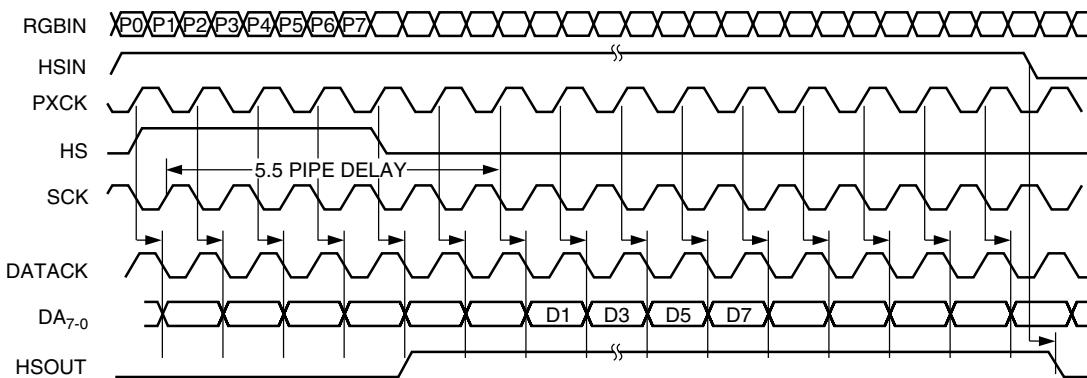


Figure 15. Single Port Mode, Alternate Pixel Sampling, (Odd Pixels)

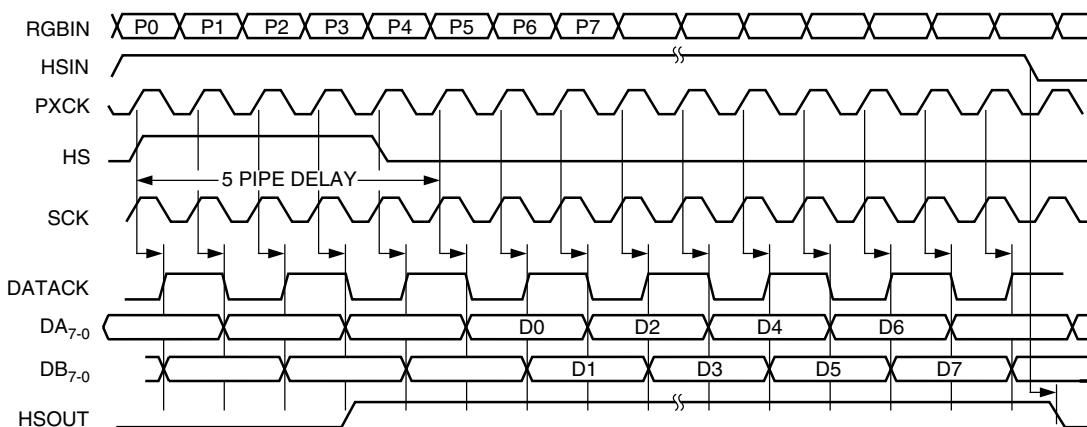


Figure 16. Dual Port Mode, Interleaved Outputs

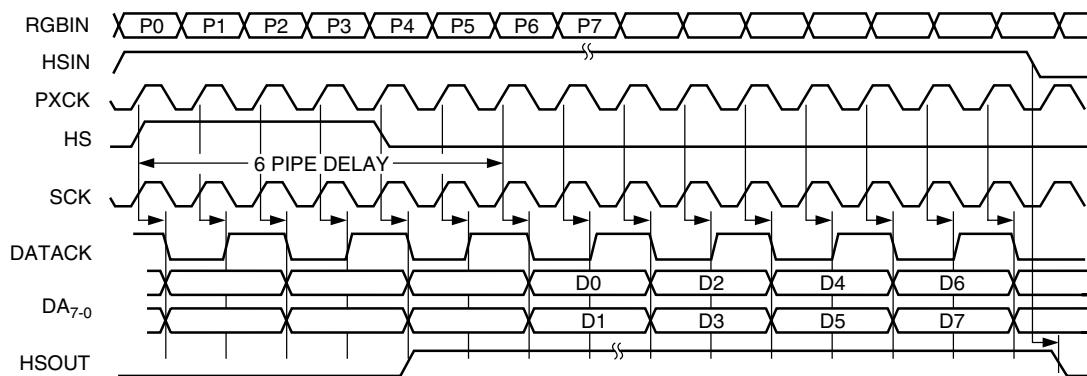


Figure 17. Dual Port Mode, Parallel Outputs

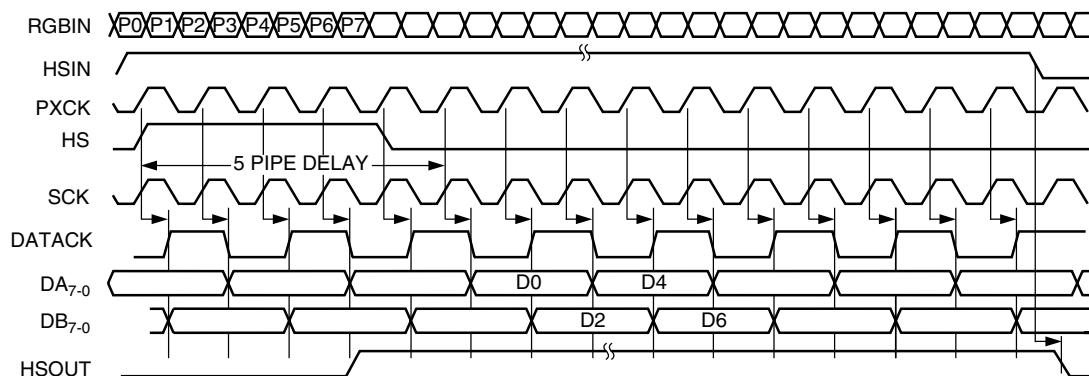


Figure 18. Dual Port Mode, Interleaved Outputs, Alternate Pixel Sampling, (Even Pixels)

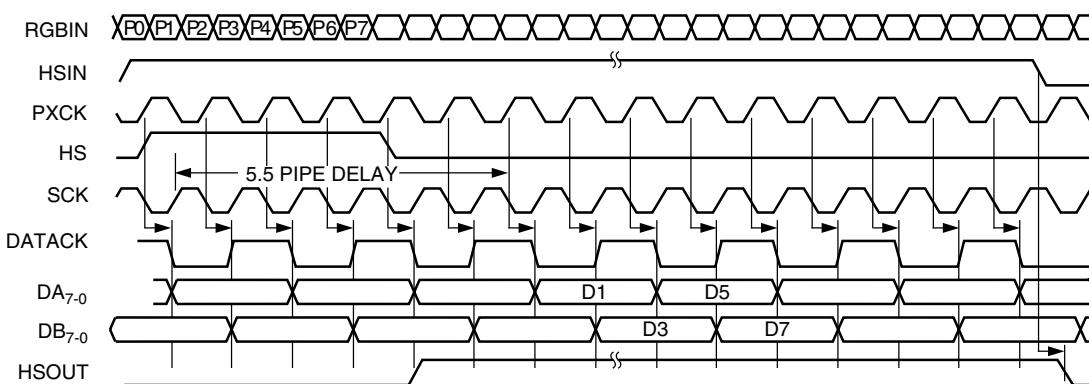


Figure 19. Dual Port Mode, Interleaved Outputs, Alternate Pixel Sampling, (Odd Pixels)

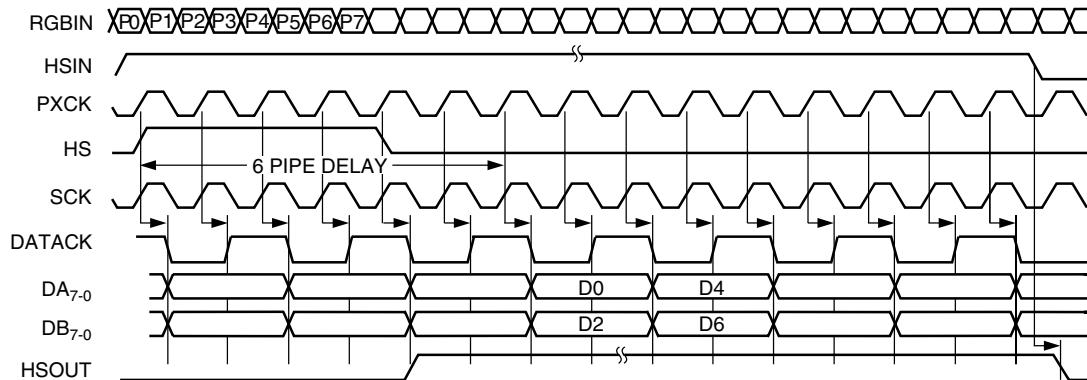


Figure 20. Dual Port Mode, Parallel Outputs, Alternate Pixel Sampling, (Even Pixels)

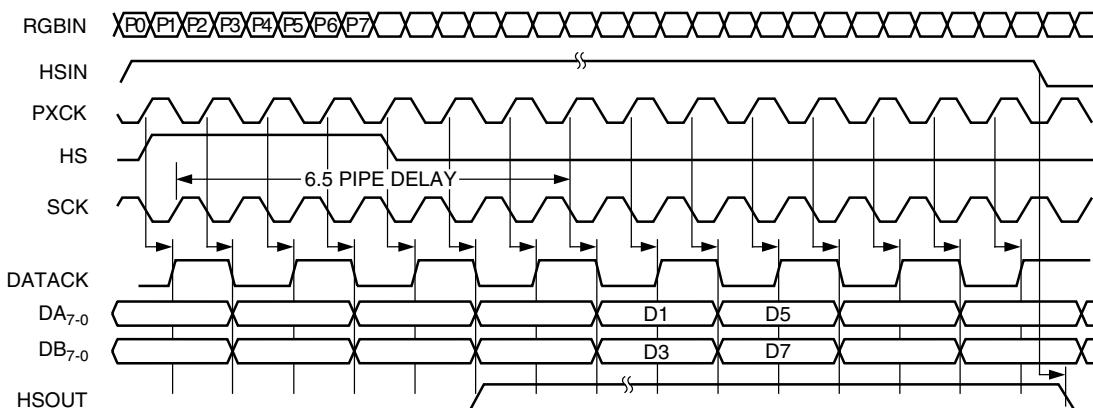


Figure 21. Dual Port Mode, Parallel Outputs, Alternate Pixel Sampling, (Odd Pixels)

## Timing and Control

Timing and Control logic encompasses the PLL, Timing Generator and Sync Stripper.

### Phase Locked Loop

Two clock types originate in the PLL:

1. Data clocks DCK and  $\overline{DCK}$ .
2. Internal sampling clock SCK.

DCK and  $\overline{DCK}$  are used to strobe data from the FMS9884A to following digital circuits. SCK is the ADC sample clock which has adjustable phase controlled through the PHASE register. DCK and  $\overline{DCK}$  are phase aligned with SCK.

Reference for the PLL is the horizontal sync input, HSIN with polarity selected by the HSPOL bit.

Frequency of the HS<sub>IN</sub> input is multiplied by the value PLLN + 1 derived from the PLLN<sub>11-4</sub> and PLLN<sub>3-0</sub> registers. PLLN + 1 should equal the number of pixels per horizontal line including active and blanked sections. Typically blanking is 20–30% of active pixels. Divide ratios from 2–4095 are supported. SCK, DCK and  $\overline{DCK}$  run at a rate PLLN + 1 times the HS<sub>IN</sub> frequency.

The PLL consists of a phase comparator, charge pump VCO and  $\pm N$  counter, with the charge pump connected through the LPF pin to an external filter. These elements must be programmed to match the incoming video source to be captured.

Values of IPUMP and FVCO for Standard VESA timing parameters are shown in Table 3. Timing of many computer video outputs does not comply with VESA recommendations. PLLN should be optimized to avoid vertical noise bars on the displayed image.

Modes marked 2X are 2X-oversampled modes where the number of samples per horizontal line is doubled. To select this mode, the Phase-locked Loop Divide Ratio value must be changed from PLL<sub>1x</sub> to:

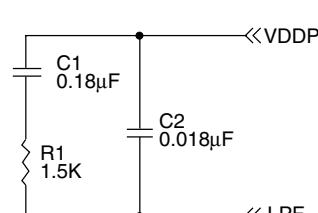
$$PLL_{2x} = 2 \bullet (PLL_{1x} + 1) - 1$$

Values of IPUMP and FVCO are set through the PLL Configuration Register (0x0C). Recommended external filter components are shown in Figure 22. RF Quality  $\pm 10\%$  ceramic capacitors with X7R dielectric are recommended.

Table 3. Recommended IPUMP and FVCO values for Standard Display Formats

| Standard | Resolution  | Refresh Rate | Horizontal Frequency | Sample Rate  | FVCO <sub>1-0</sub> | IPUMP <sub>2-0</sub> |
|----------|-------------|--------------|----------------------|--------------|---------------------|----------------------|
| VGA      | 640 X 480   | 60 Hz        | 31.5 kHz             | 25.175 MHz   | 01                  | 100                  |
|          |             | 72 Hz        | 37.7 kHz             | 31.500 MHz   | 01                  | 100                  |
|          |             | 75 Hz        | 37.5 kHz             | 31.500 MHz   | 01                  | 100                  |
|          |             | 85 Hz        | 43.3 kHz             | 36.000 MHz   | 01                  | 100                  |
| 2X       | 640 X 480   | 60 Hz        | 31.5 kHz             | 50 MHz       | 01                  | 100                  |
|          |             | 67 Hz        | 35 kHz               | 31 MHz       | 01                  | 100                  |
|          |             | 72 Hz        | 37.7 kHz             | 63 MHz       | 01                  | 100                  |
|          |             | 75 Hz        | 37.5 kHz             | 72 MHz       | 01                  | 100                  |
|          |             | 70 Hz        | 31.5 kHz             | 56.6 MHz     | 01                  | 100                  |
| SVGA     | 800 X 600   | 56 Hz        | 35.1 kHz             | 36.000 MHz   | 01                  | 100                  |
|          |             | 60 Hz        | 37.9 kHz             | 40.000 MHz   | 01                  | 100                  |
|          |             | 72 Hz        | 48.1 kHz             | 50.000 MHz   | 01                  | 110                  |
|          |             | 75 Hz        | 46.9 kHz             | 49.500 MHz   | 01                  | 110                  |
|          |             | 85 Hz        | 53.7 kHz             | 56.250 MHz   |                     |                      |
| XGA      | 1024 X 768  | 60 Hz        | 48.4 kHz             | 65.000 MHz   | 01                  | 111                  |
|          |             | 70 Hz        | 56.5 kHz             | 75.000 MHz   | 01                  | 111                  |
|          |             | 75 Hz        | 60.0 kHz             | 78.750 MHz   | 10                  | 111                  |
|          |             | 80 Hz        | 64.0 kHz             | 85.500 MHz   |                     |                      |
|          |             | 85 Hz        | 68.3 kHz             | 94.500 MHz   |                     |                      |
| Mac      | 1024 X 768  | 60 Hz        | 48 kHz               | 64 MHz       | 01                  | 111                  |
|          | 1152 X 870  | 75 Hz        | 60 kHz               | 80 MHz       | 10                  | 111                  |
|          |             | 75 Hz        | 69 kHz               | 100 MHz      | 10                  | 111                  |
| Sun      | 1152 X 900  | 66 Hz        | 62 kHz               | 93 MHz       | 10                  | 111                  |
| HP       | 1280 X 1024 | 60 Hz        | 63 kHz               | 108 MHz      | 10                  | 111                  |
| SXGA     | 1280 X 1024 | 60 Hz        | 64.0 kHz             | 108.000 MHz  | 10                  | 111                  |
|          |             | 72 Hz        | 78.1 kHz             | 135.000 MHz  | 11                  | 111                  |
|          |             | 75 Hz        | 80.0 kHz             | 135.000 MHz  | 11                  | 111                  |
|          |             | 85 Hz        | 91.1 kHz             | 157.500 MHz  | 11                  | 111                  |
| UXGA     | 1600 X 1200 | 60 Hz        | 75.0 kHz             | 162.000 MHz  | 11                  | 111                  |
|          |             | 65 Hz        | 81.3 kHz             | 175.500 MHz  | 11                  | 111                  |
|          |             | 70 Hz        | 87.5 kHz             | 189.000 MHz* |                     |                      |
|          |             | 75 Hz        | 93.8 kHz             | 202.500 MHz* |                     |                      |
|          |             | 85 Hz        | 106.3 kHz            | 229.500 MHz* |                     |                      |

VESA Monitor Timing Standards and Guidelines, September 17, 1998

\* Graphics sampled at  $1/2$  incoming pixel rate using Alternate Pixel Sampling mode.

Loop performance is established by setting:

1. VCO frequency range through FVCO<sub>1-0</sub>. (see Table 4)
2. Charge Pump Current through IPUMP<sub>2-0</sub>. (see Table 5)
3. External loop filter component values.

Figure 22. Schematic, PLL Filter.

**Table 4. VCO Frequency Bands**

| FVCO <sub>2-0</sub> | Frequency Range (MHz) | KVCO (MHz/V) |
|---------------------|-----------------------|--------------|
| 00                  | 20–90                 | 60           |
| 01                  |                       |              |
| 10                  | 80–120                | 90           |
| 11                  | 110–175               | 100          |

**Table 5. Charge Pump Current Levels**

| IPUMP <sub>2-0</sub> | Current (μA) |
|----------------------|--------------|
| 000                  | 50           |
| 001                  | 100          |
| 010                  | 150          |
| 011                  | 250          |
| 100                  | 350          |
| 101                  | 500          |
| 110                  | 750          |
| 111                  | 1500         |

Setting SPHASE<sub>4-0</sub> selects the sampling phase of SCK relative to PXCK in 32 steps of 11.25°. Phase of the output data, DCK and  $\overline{DCK}$  is slaved to the SCK phase.

Clock jitter is less than 5% of pixel period in all operating modes. At lower frequencies below 40MHz, the jitter rises but can be reduced by over-sampling at a 2X clock rate. Data should be read out of one port using the dual port mode. See Performance section for jitter specifications and plots.

## COAST

COAST = H disables PLL lock to HSIN, while the VCO frequency is retained. VCO frequency remains stable over several lines without updates from HSIN. COAST can be connected directly to the vertical sync signal or supplied by the graphics controller.

Operation of COAST is depicted in Figure 23. HSOUT polarity is always positive. When COAST = L, HSOUT tracks HSIN (shown with positive polarity in Figure 23):

1. HSOUT rising edge tracks HSIN delayed by a few pixels.
2. HSOUT falling edge tracks the trailing edge of HSIN with no delay.

When COAST = H, the PLL flywheels, disregarding the incoming HSIN references, while the HSOUT waveform depends upon the state of HSIN.

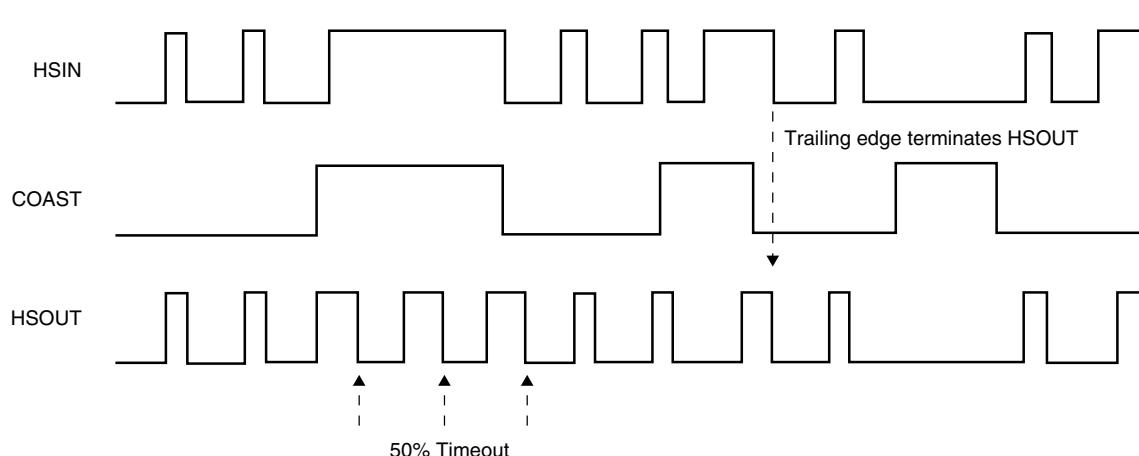
1. If HSIN = H:
  - a.) HSOUT rising edge remains locked to the PLL.
  - b.) HSOUT trailing edge falls after 50% of the HSOUT period has expired.
2. HSIN transitions:
  - a.) HSOUT rising edge remains locked to the PLL.
  - b.) HSOUT falling edge is terminated by the trailing edge of HSIN.
3. If HSIN = L, then HSOUT = L

## Timing Generator

Timing and Control logic generates:

1. Internal sampling clock, SCK.
2. Output data clocks, DCK and  $\overline{DCK}$ .
3. Output horizontal sync, HS<sub>OUT</sub>.
4. Internal clamp pulse, ICLAMP.

With HSPOL set correctly, ICLAMP delay follows the trailing edge of horizontal sync in (HSIN). Delay is set by the CD register. Width of ICLAMP is set by the CW register. Range of CD and CW values is 1–255 pixels.

**Figure 23.**

## Sync Stripper

Some video signals include embedded composite sync rather than separate horizontal and vertical sync signals, typically sync on green. Composite sync is extracted from Composite Video at the ACS<sub>IN</sub> pin.

When the ACS<sub>IN</sub> signal falls below a 150mV ground referenced threshold, sync is detected. Composite Sync Output, DCS<sub>OUT</sub> reflects the ACS<sub>IN</sub> sync timing with non-inverted CMOS digital levels.

## Power Down

PWRDN = L minimizes FMS9884A power consumption. Data outputs become high impedance. Clocks generation is stopped. Register contents are maintained. Sync stripping and the internal voltage reference function.

## Serial Interface

Register access is via a 2-wire I<sup>2</sup>C/SMBus compatible interface. As a slave device, the 7-bit address is selected by the A<sub>1-0</sub> pins (see Table 6). Serial port pins SDA and SCL communicate with the host SMBus/I<sup>2</sup>C controller which act as a master.

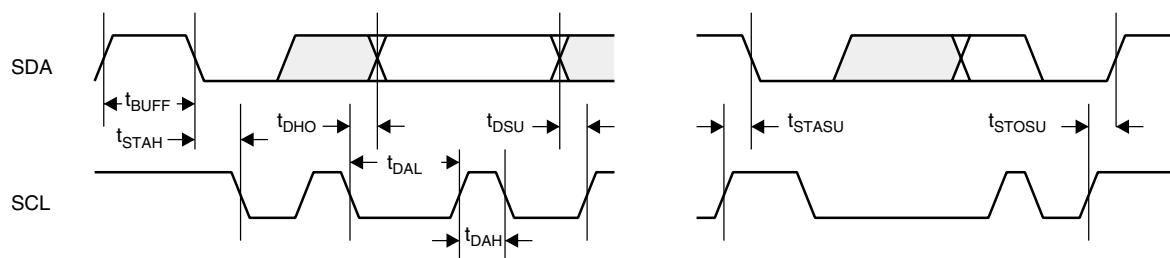
Since the serial control port is design to interface with 3.3V logic, the pins must be protected by series connected 150Ω resistors if SDA and SCL signals originate from 5V logic. (See Applications Section)

**Table 6. Serial Interface Address Codes**

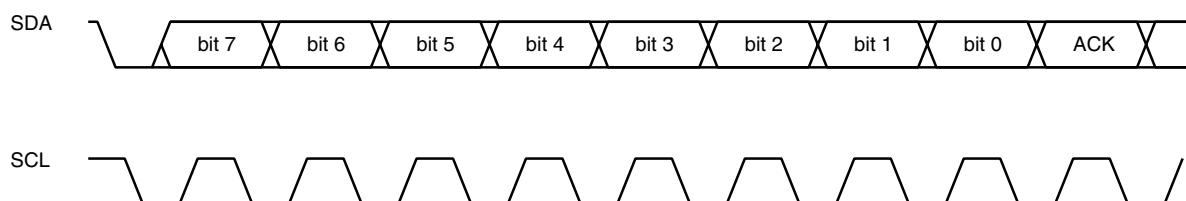
| A <sub>1-0</sub> | 7-bit Address |
|------------------|---------------|
| 00               | 4C            |
| 01               | 4D            |
| 10               | 4E            |
| 11               | 4F            |

Two signals comprise the bus: clock (SCL) and bi-directional data (SDA). When receiving and transmitting data through the serial interface, the FMS9884A acts as a slave, responding only to commands by the I<sup>2</sup>C/SMBus master.

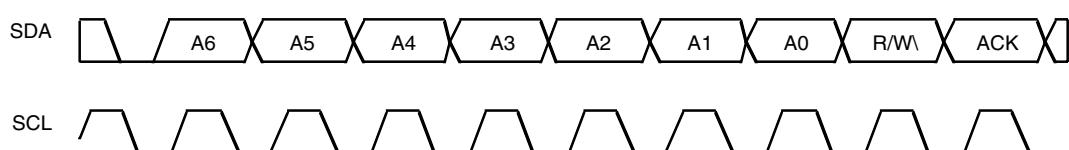
Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA may change only when SCL = L. An SDA transition while SCL = H is interpreted as a start or stop signal.



**Figure 24. Serial Bus: Read/Write Timing**



**Figure 25. SerialBus: Typical Byte Transfer**



**Figure 26. Serial Bus: Slave Address with Read/Write Bit**

There are five steps within an I<sup>2</sup>C/SMBus cycle:

1. Start signal
2. Slave address byte
3. Pointer register address byte
4. Data byte to read or write
5. Stop signal

When the Serial Bus interface is inactive, SCL = H and SDA = H. Communications are initiated by sending a start signal (Figure 24, left waveform) that is a HIGH-to-LOW transition on SDA while SCL is HIGH. A start signal alerts all slaved devices that a data transfer sequence is imminent.

As shown in Figure 26, after a start signal, the first eight bits of data comprise a seven bit slave address followed a single R/W bit (Read = H, Write = L) to set the direction of data transfer: read from; or write to the slave device. If the transmitted slave address matches the address of the FMS9884A which set by the state of the ADD pin, the FMS9884A acknowledges by pulling SDA LOW on the 9th SCL pulse (see Figure 26). If the addresses do not match or the register being accessed is 0x0F, the FMS9884A does not acknowledge.

For each byte of data read or written, the MSB is the first bit of the sequence.

### Data Transfer via Serial Interface

If a slave device, such as the FMS9884A does not acknowledge the master device during a write sequence, SDA remains HIGH so the master can generate a stop signal. During a read sequence, if the master device does not acknowledge by bringing SDA = L, the FMS9884A interprets SDA = H as “end of data.” SDA remains HIGH so the master can generate a stop signal (Figure 24, right waveform).

To write data to a specific FMS9884A control register, three bytes are sent:

1. Write the slave address byte with bit R/W = L.
2. Write the pointer byte.
3. Write to the control register indexed by the pointer.

After each byte is written, the pointer auto-increments to allow multiple data byte transfers within one write cycle.

Data is read from the control registers of the FMS9884A in a similar manner, except that two data transfer operations are required:

1. Write the slave address byte with bit R/W = L.
2. Write the pointer byte.
3. Write the slave address byte with bit R/W = H
4. Read the control register indexed by the pointer.

After each byte is read, the pointer auto-increments to allow multiple data byte transfers within one read cycle.

Preceding each slave write, there must be a start cycle. Following the pointer byte there should be a stop cycle.

After the last read, there must be a stop cycle comprising a LOW-to-HIGH transition of SDA while SCL is HIGH. (see Figure 24, right waveform)

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

### Serial Interface Read/Write Examples

Examples below show how serial bus cycles can be linked together for multiple register read and write access cycles. For sequential register accesses, each ACK handshake initiates further SCL clock cycles from the master to transfer the next data byte.

#### Write to one register

1. Start signal
2. Slave Address byte (R/W bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Stop signal

#### Write to four consecutive registers

1. Start signal
2. Slave Address byte (R/W bit = LOW)
3. Pointer byte
4. Data byte to base address
5. Data byte to (base address + 1)
6. Data byte to (base address + 2)
7. Data byte to (base address + 3)
8. Stop signal

#### Read from one register

1. Start signal
2. Slave Address byte (R/W bit = LOW)
3. Pointer byte (= base address)
4. Stop signal (optional)
5. Start signal
6. Slave Address byte (R/W bit = HIGH)
7. Data byte from base address
8. Stop signal

#### Read from four registers

1. Start signal
2. Slave Address byte (R/W bit = LOW)
3. Pointer byte (= base address)
4. Stop signal (optional)
5. Start signal
6. Slave Address byte (R/W bit = HIGH)
7. Data byte from base address
8. Data byte from (base address + 1)
9. Data byte from (base address + 2)
10. Data byte from (base address + 3)
11. Stop signal

## Absolute Maximum Ratings

(beyond which the device may be damaged)<sup>1</sup>

| Parameter  | Min.  | Typ. | Max.             | Unit   |
|--|-------|------|------------------|--------|
| <b>Power Supply Voltages</b>                                   |       |      |                  |        |
| V <sub>CC</sub> (Measured to GND)                              | -0.5  |      | 4                | V      |
| <b>Digital Inputs</b>  |       |      |                  |        |
| Applied voltage (Measured to GND) <sup>2</sup>                 | -0.3  |      | V <sub>DDA</sub> | V      |
| Forced current <sup>3, 4</sup>                                 | -5.0  |      | 5.0              | mA     |
| <b>Analog Inputs</b>   |       |      |                  |        |
| Applied Voltage (Measured to GND) <sup>2</sup>                 | -0.5  |      | V <sub>DDA</sub> | V      |
| Forced current <sup>3, 4</sup>                                 | -10.0 |      | 10.0             | mA     |
| <b>Digital Outputs</b>   |       |      |                  |        |
| Applied voltage (Measured to GND) <sup>2</sup>                 | -0.5  |      |                  | V      |
| Forced current <sup>3, 4</sup>                                 | -6.0  |      | 6.0              | mA     |
| Forced current <sup>3, 4</sup>                                 | -8.0  |      | 8.0              | mA     |
| Short circuit duration (single output in HIGH state to ground) |       |      | 1                | second |
| <b>Temperature</b>   |       |      |                  |        |
| Junction   |       |      | 150              | °C     |
| Lead Soldering (10 seconds)                                    |       |      | 300              | °C     |
| Vapor Phase Soldering (1 minute)                               |       |      | 220              | °C     |
| Storage  | -65   |      | 150              | °C     |
| Electrostatic Discharge <sup>5</sup>                           |       |      | ±150             | V      |

### Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

## Operating Conditions

| Parameter        | Min.                           | Nom.    | Max. | Units  |
|------------------|--------------------------------|---------|------|--------|
| V <sub>DDA</sub> | 3.0                            | 3.3     | 3.6  | V      |
| V <sub>DDP</sub> | $\leq 140 \text{ Ms/s}$        | 3.0     | 3.3  | V      |
|                  |                                | 3.4     | 3.5  | V      |
| V <sub>DDO</sub> | 2.2                            | 2.5–3.3 | 3.6  | V      |
| T <sub>A</sub>   | Ambient Temperature, Still Air | 0       | 70   | °C     |
|                  | A/D analog input range, min.   |         | 500  | mV p-p |
|                  | A/D analog input range, max.   | 1000    |      | mV p-p |

## Electrical Characteristics<sup>1</sup>

| Parameter                     | Conditions                                   | Min.                              | Typ.                  | Max. | Unit   |
|-------------------------------|--|-----------------------------------|-----------------------|------|--------|
| <b>Power Supply Currents</b>  |  |                                   |                       |      |        |
| I <sub>DDA</sub>              | Supply current, ADC                          | Operating, 25°C                   |                       | 210  | mA     |
| I <sub>DDD</sub>              | Supply current <sup>2</sup> , Digital Output | Operating, 25°C                   |                       | 30   | mA     |
| I <sub>DDP</sub>              | Supply current, PLL                          | Operating, 25°C                   |                       | 50   | mA     |
| P <sub>D</sub>                | Power dissipation                            | 0 to 70°C                         |                       | 950  | mW     |
| I <sub>PD</sub>               | Power-down current                           | 0 to 70°C                         |                       | 15   | mA     |
| P <sub>DD</sub>               | Powered-down dissipation                     | 0 to 70°C                         |                       | 50   | mW     |
| <b>Digital Inputs/Outputs</b> |  |                                   |                       |      |        |
| C <sub>I</sub>                | Input Capacitance                            | 25°C                              |                       | 3    | pF     |
| C <sub>O</sub>                | Output Capacitance                           | 25°C                              |                       | 7    | pF     |
| I <sub>IH</sub>               | Input Current, HIGH                          | 0 to 70°C                         | -1                    | +1   | µA     |
| I <sub>IL</sub>               | Input Current, LOW                           | 0 to 70°C                         | -1                    | +1   | µA     |
| V <sub>IH</sub>               | Input Voltage, HIGH                          | 0 to 70°C                         | 2.5                   |      | V      |
| V <sub>IL</sub>               | Input Voltage, LOW                           | 0 to 70°C                         |                       | 0.8  | V      |
| I <sub>OHD</sub>              | Output Current, HIGH, data                   | 0 to 70°C                         |                       | 4    | mA     |
| I <sub>OHC</sub>              | Output Current, HIGH, clock                  | 0 to 70°C                         |                       | 8    | mA     |
| I <sub>OLD</sub>              | Output Current, LOW, data                    | 0 to 70°C                         |                       | 4    | mA     |
| I <sub>OLC</sub>              | Output Current, LOW, clock                   | 0 to 70°C                         |                       | 8    | mA     |
| V <sub>OH</sub>               | Output Voltage, HIGH                         | I <sub>OH</sub> = max., 0 to 70°C | V <sub>DDO</sub> -0.1 |      | V      |
| V <sub>OL</sub>               | Output Voltage, LOW (V <sub>DD3</sub> )      | I <sub>OL</sub> = max., 0 to 70°C |                       | 0.1  | V      |
| <b>Serial Bus I/O</b>         |  |                                   |                       |      |        |
| V <sub>SMIH</sub>             | Input Voltage, HIGH                          | 0 to 70°C                         | 2.5                   |      | V      |
| V <sub>SMIL</sub>             | Input Voltage, LOW                           | 0 to 70°C                         |                       | 0.8  | V      |
| V <sub>SMOL</sub>             | Output Voltage, LOW                          | I <sub>SMOL</sub> = max.          |                       | 0.1  | V      |
| I <sub>SMOH</sub>             | Output Current, HIGH (Open Drain)            | 0 to 70°C                         | -1                    | +1   | µA     |
| I <sub>SMOL</sub>             | Output Current, LOW                          | 0 to 70°C                         |                       | 4    | mA     |
| <b>Analog Inputs</b>          |  |                                   |                       |      |        |
| I <sub>B</sub>                | Input bias current                           | 0 to 70°C                         | -1                    | 1    | µA     |
| E <sub>OS</sub>               | Input Offset Voltage <sup>3</sup>            | 0 to 70°C                         |                       | 11   | mV     |
| <b>Reference Output</b>       |  |                                   |                       |      |        |
|                               | Output Voltage                               | 0 to 70°C                         | 1.15                  | 1.25 | V      |
|                               | Temperature Coefficient                      | 0 to 70°C                         |                       | ±50  | ppm/°C |

### Notes:

1. Unless otherwise stated, 0 to 70°C
2. DEMUX = 1; DCK,  $\overline{DCK}$  load = 15 pF; data load = 5 pF.
3. For optimum performance, null the input offset by calibrating gain and offset (see Firmware section under Applications Information).

## Switching Characteristics

| Parameter                           | Conditions                    | Min.      | Typ. | Max. | Unit     |
|-------------------------------------|-------------------------------|-----------|------|------|----------|
| <b>Analog-to-Digital Converters</b> |                               |           |      |      |          |
|                                     | Conversion rate               | 0 to 70°C | 10   |      | 175 Ms/s |
| $t_{SKEW}$                          | Data to clock skew            | 0 to 70°C | -0.5 | 2.0  | ns       |
| <b>Timing Generator</b>             |                               |           |      |      |          |
|                                     | HSIN input frequency          | 0 to 70°C | 15   |      | 110 kHz  |
|                                     | Maximum PLL clock rate        | 0 to 70°C | 108  |      | MHz      |
|                                     | FMS9884AKAC100                |           | 140  |      |          |
|                                     | FMS9884AKAC140                |           | 175  |      |          |
|                                     | Minimum PLL clock rate        | 0 to 70°C |      | 20   | MHz      |
| <b>Serial Bus Interface</b>         |                               |           |      |      |          |
| $t_{DAL}$                           | SCL Pulse Width, LOW          | 0 to 70°C | 4.7  |      | μs       |
| $t_{DAH}$                           | SCL Pulse Width, HIGH         | 0 to 70°C | 4.0  |      | μs       |
| $t_{STAH}$                          | SDA Start Hold Time           | 0 to 70°C | 4.0  |      | μs       |
| $t_{STASU}$                         | SCL to SDA Setup Time (Start) | 0 to 70°C | 4.7  |      | μs       |
| $t_{STOSU}$                         | SCL to SDA Setup Time (Stop)  | 0 to 70°C | 4.0  |      | μs       |
| $t_{BUFF}$                          | SDA Stop Hold Time Setup      | 0 to 70°C | 4.7  |      | μs       |
| $t_{DSU}$                           | SDA to SCL Data Setup Time    | 0 to 70°C | 250  |      | ns       |
| $t_{DHO}$                           | SDA to SCL Data Hold Time     | 0 to 70°C | 0    |      | ns       |

## System Performance Characteristics

| Parameter                          | Conditions                                | Min.      | Typ. | Max. | Unit                |
|------------------------------------|---|-----------|------|------|---------------------|
| <b>Analog to Digital Converter</b> |   |           |      |      |                     |
| $E_{LI}$                           | Integral Linearity Error <sup>1</sup>     | 0 to 70°C | -2.5 |      | 2.5 LSB             |
| $E_{LD}$                           | Differential Linearity Error <sup>1</sup> | 0 to 70°C | -1.0 |      | +1.0 LSB            |
|                                    | Missing Codes                             | 0 to 70°C |      | 0    |                     |
|                                    | Input full scale matching                 | 0 to 70°C |      | 2    | 6 %FS <sup>2</sup>  |
|                                    | Offset adjustment range                   | 0 to 70°C | 22   | 23.5 | 25 %FS <sup>2</sup> |
|                                    | Gain tempco                               | 25°C      |      | 280  | ppm/°C              |
| $B_W$                              | Analog bandwidth, full power              | 25°C      |      | 500  | MHz                 |
|                                    | Transient response                        | 25°C      |      | 2    | ns                  |
| $t_{OV}$                           | Over-voltage recovery time                | 25°C      |      | 1.5  | ns                  |
| <b>Phase Locked Loop</b>           |   |           |      |      |                     |
| $t_{PP}$                           | Peak-to-peak PLL Jitter @ MHz             | 25.175    | 25°C | 6.5  | ns                  |
|                                    |   | 31.5      |      | 4.1  |                     |
|                                    |   | 40        |      | 3.3  |                     |
|                                    |   | 49.5      |      | 2.3  |                     |
|                                    |   | 78.75     |      | 1.5  |                     |
|                                    |   | 108       |      | 1.0  |                     |
|                                    |   | 135       |      | 0.8  |                     |
|                                    |   | 162       |      | 0.7  |                     |
|                                    |   | 175       |      | 0.8  |                     |

## System Performance Characteristics (continued)

| Parameter      | Conditions                      | Min. | Typ. | Max. | Unit |
|----------------|---------------------------------|------|------|------|------|
| <b>Thermal</b> |                                 |      |      |      |      |
| $\theta_{JC}$  | Resistance, junction-to-case    |      |      | 8.4  | °C/W |
| $\theta_{JA}$  | Resistance, junction-to-ambient |      |      | 35   | °C/W |

### Notes:

1. Calibrated to 700 mV input.
2. Percentage of Full Scale (uncalibrated).

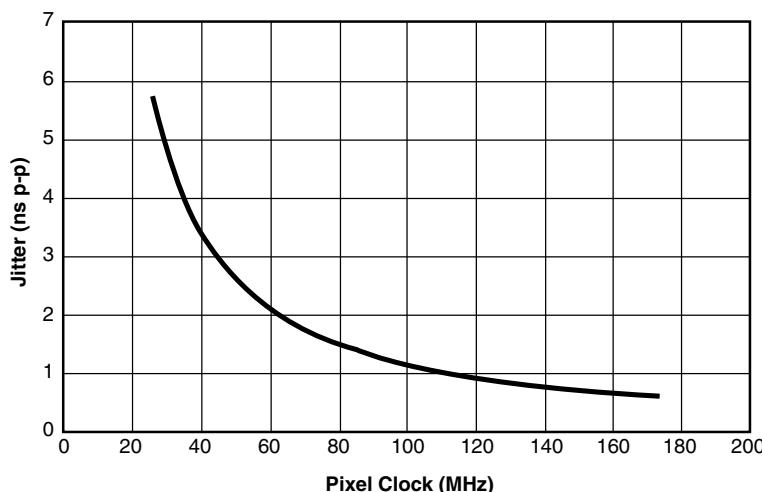


Figure 27. Pixel Clock Jitter vs. Frequency

## Applications Information

Two applications circuits are reviewed:

1. AC coupled digitizer with clamp.
2. AC coupled digitizer with dual ported outputs and sync stripping.

To minimize component count, use of the following on-chip circuits is recommended:

1. ADC sampling clock.
2. Clamp.
3. Voltage reference
4. Dual ported data outputs

Optimum PLL Configuration Register (address 0x0C) settings for typical graphics modes are listed in Table 3. Unless otherwise indicated, all modes are compliant with VESA specifications. For unlisted modes, values should be adjusted to optimize performance.

By adjusting the values in the gain (GR, GG, GB) and offset (OSR, OSG, OSB) registers, the input conversion range can be matched to the incoming analog signals.

To use the FMS9884A in applications where the PLL clock frequency will exceed 140 MHz, the PLL power supply voltage must be 3.4 V min. For applications up to and including 140 MHz, the PLL supply can be 3.0 V min.

## AC Coupled Digitizer

Shown in Figure 28 is an implementation of a video digitizer with AC coupled RGB inputs. Horizontal sync input, HS is passed through a voltage divider which attenuates the 5.0 V logic HIGH excursion to the 3.3 V HIGH input level of the FMS9884A. Vertical sync is also attenuated to make the VSOUT level compatible with 3.3 V pixel processing following the FMS9884A.

Output data is three channel port A data only with a maximum rate of 175Ms/s 24-bit pixels. Data is clocked out on the negative edge of DCK. HSOUT defines the active video along a line, while incoming vertical sync, VSIN is propagated as VSOUT to the output data to synchronize handling of digitized frames of output data.

Control is through the serial port with  $150\Omega$  resistors inserted to allow interfacing with 5V logic. If the serial bus is operates with 3.3V levels, these resistors are unnecessary.

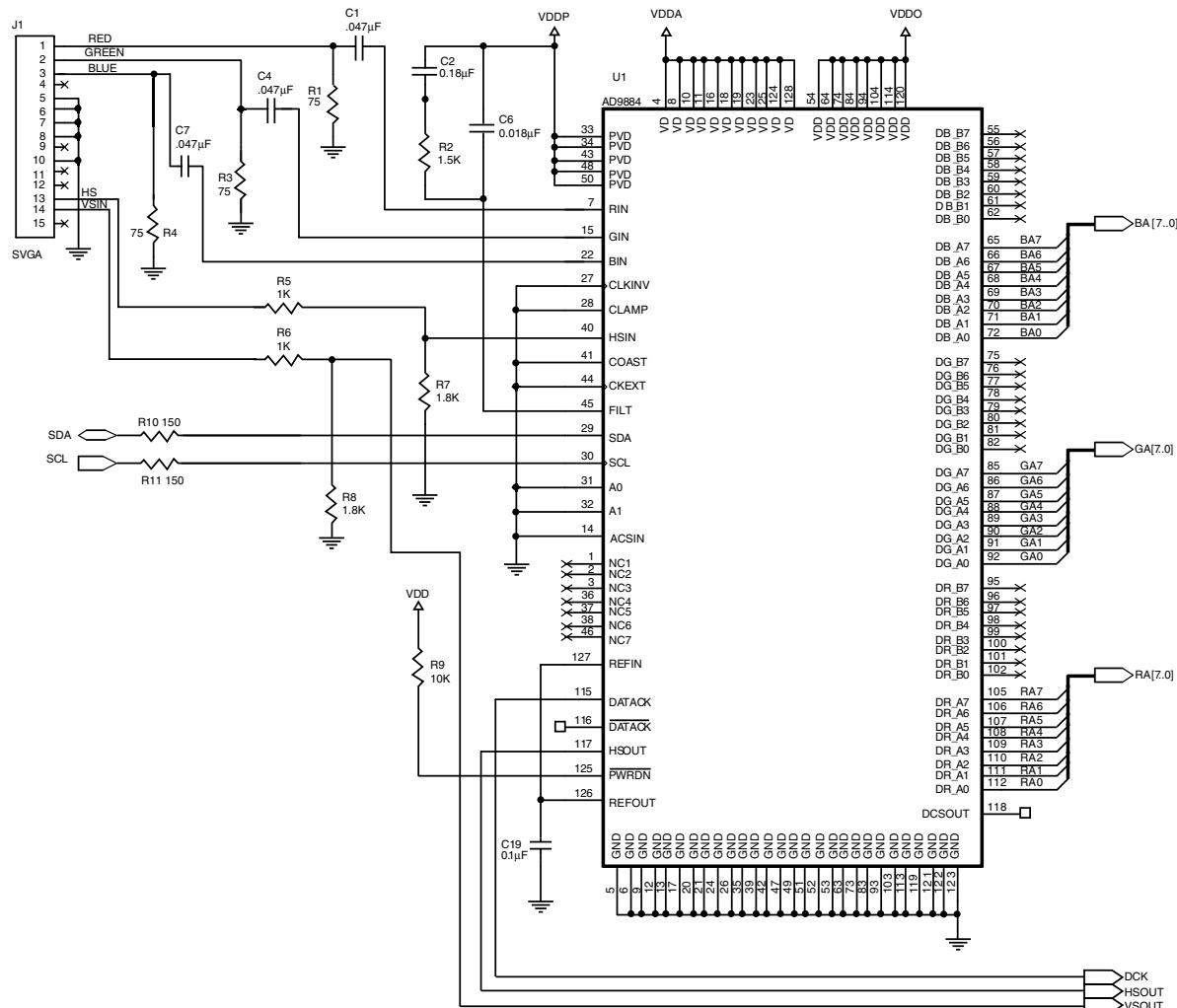


Figure 28. Schematic, VGA Digitizer, Single-Port Outputs

### VGA Source with Dual Ported Outputs

Shown in Figure 29 is a more complex implementation of a video digitizer. Incoming RGB video has sync-on-green. Output data is dual ported. COAST is shown to free wheel the PLL when horizontal sync is inactive or 2H pulse are present.

RGB inputs signals are AC coupled to the FMS9884A RGB inputs with the green input connected to the Sync Separator input, CVIN.

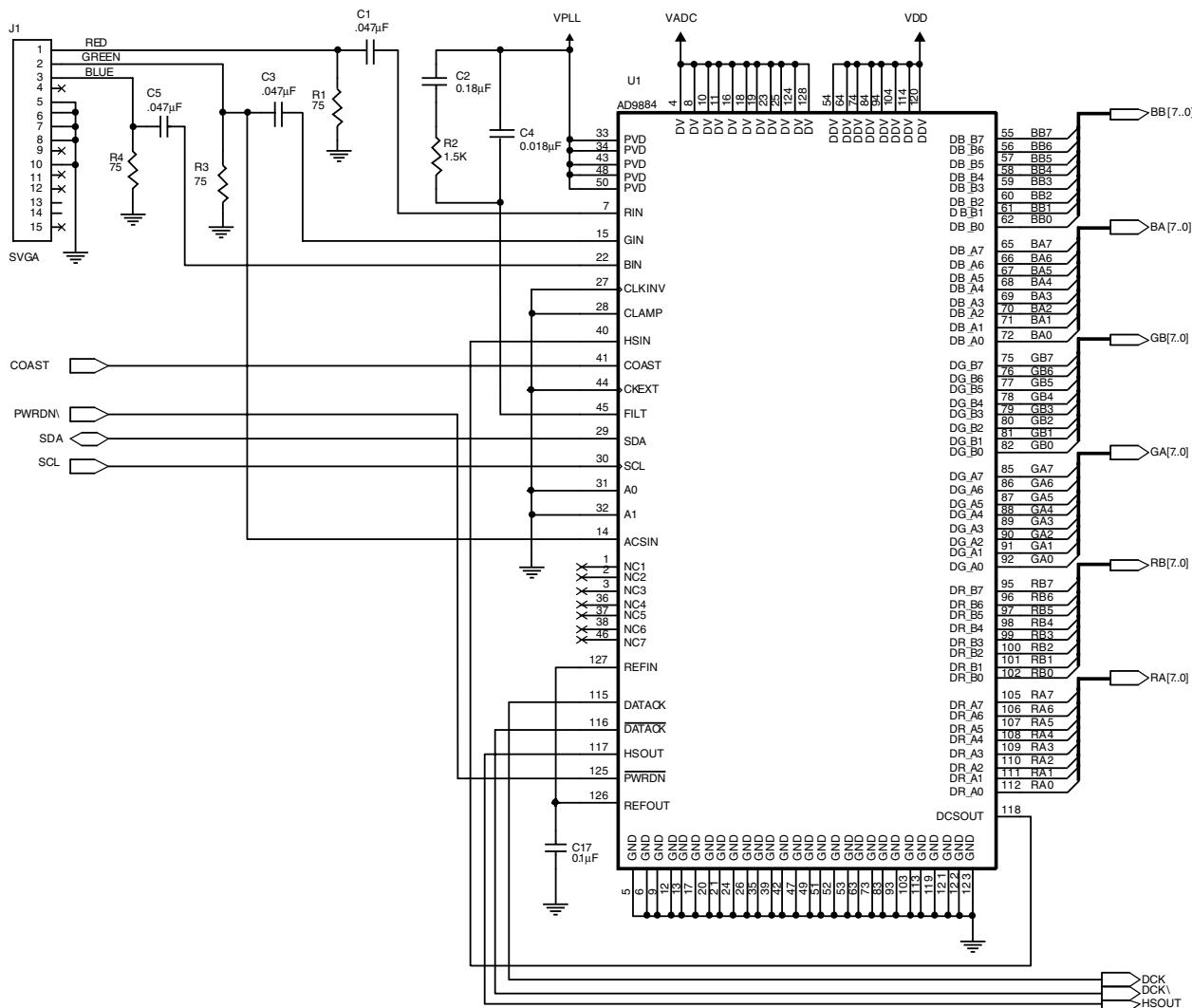
Output data is three channel dual port data with a maximum rate of 70Ms/s per port. Port A data is synchronized to the negative edge of DCK. Port B data transitions on:

1. Positive edge of DCK in the Parallel Data Out Mode.
2. Negative edge of DCK in the Interleaved Data Out Mode.

DCK and DCK clocks should be timed to strobe data that is valid between transitions.

Composite Sync from the Sync Stripper output CSOUT is supplied to the HSYNC input as a reference for the internal PLL. CSSOUT contains horizontal and vertical sync signals that can be extracted by subsequent Sync processing logic. If the vertical sync pulse omits horizontal sync or if serrations or equalizing pulses are present, then the sync processing logic should emit a COAST signal to disengage the PLL from the HSYNC input during the Vertical Sync interval.

Vertical and horizontal sync waveforms within CSSOUT signal frame the active video area.



**Figure 29. Schematic, VGA Digitizer, Dual Port Outputs**

## Printed Wiring Board Design Guidelines

Recommended strategy is to mount the FMS9884A over a ground plane with carefully routed analog inputs and digital outputs. All connections should be treated as transmission lines to ensure that reflections due to mismatches are minimized and ground return currents do not interfere with critical signals.

## Analog Inputs

### Recommendations:

1. Keep analog trace lengths short to minimize crosstalk.
2. Terminate analog inputs with  $75\Omega$  resistors, placed close to the FMS9884A analog inputs,  $R_{IN}$ ,  $G_{IN}$  and  $B_{IN}$ . By matching transmission line impedances, reflections will be minimized.

3. Layout traces as  $75\Omega$  transmission lines.
4. Avoid running analog traces near digital traces. Due to the wide input bandwidth (500MHz) digital noise can easily leak into analog inputs.
5. If necessary, limit bandwidth by adding a ferrite bead in series with each RGB input as shown in Figure 30. A Fair-Rite #2508051217Z0 is recommended. Further bandwidth reduction using a shunt 10pF capacitor may reduce snow (intensity noise) caused by HF noise riding on the RGB input. Mismatches, reflections and noise may cause ringing or distortion of the incoming video signals.

- Bypass the reference with a  $0.1\mu\text{F}$  capacitor to ground.

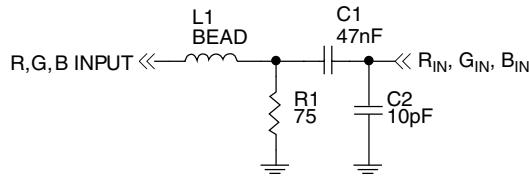


Figure 30. RGB Input Filter Options

## Digital I/O

Recommendations:

- Route digital I/O signals clear of analog inputs.
- Terminate clock lines to reduce reflections. Treat clock lines as transmission lines.
- Scale the HSIN input to 3.3V, using a resistor network or a series  $1\text{k}\Omega$  resistor.
- Limit Serial Port inputs SDA and SDL with  $150\Omega$  resistors connected directly to the pins.

- If necessary terminate the HSIN input with  $330/220\Omega$ .
- If necessary, to reduce reflections, EMI or spikes add a  $50-200\Omega$  resistor at each data output pin.
- To minimize noise within the FMS9884A, restrict the capacitive load at the digital outputs to  $< 10\text{pF}$ .

## Power and Ground

A schematic of the recommended power distribution is shown in Figure 31. Note that:

- Analog and digital circuits are layed out over a common solid ground plane.
- Each FMS9884A pin is decoupled with a  $0.1\mu\text{F}$  capacitor.
- A group of pins may be de-coupled through a common capacitor if no pin is more than 5 mm from the capacitor.
- A separate regulated supply is used for the phase-locked loop power supply,  $V_{DPP}$ .
- Capacitors are attached to each PLL pin or pin-pair.

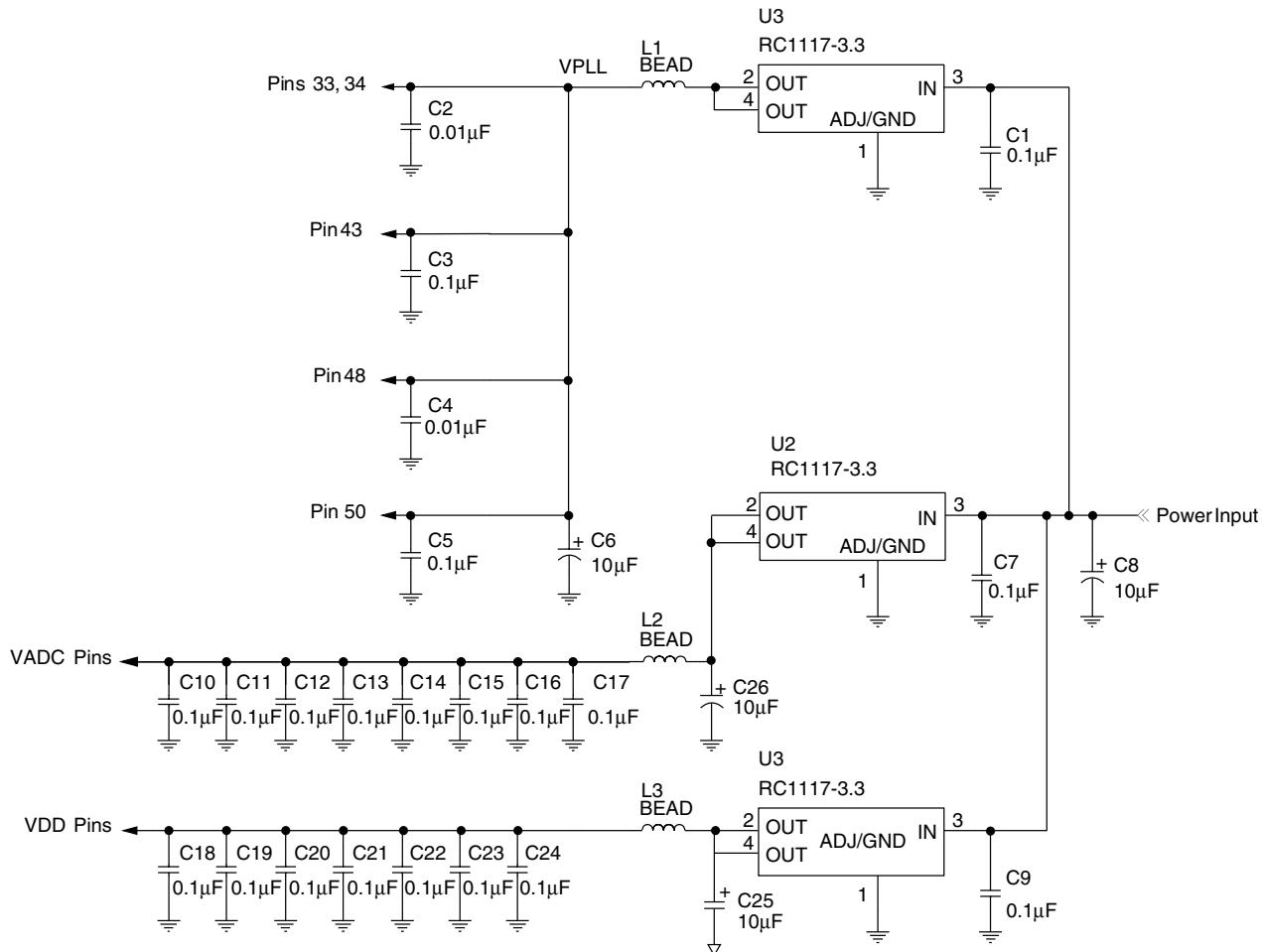


Figure 31. Recommended Power Distribution

Physical placement of PLL power supply decoupling components is critical. Bearing in mind the following suggestions:

1. All components should be placed in close proximity to the FMS9884A pins.
2. Routing through vias should be avoided, if possible.
3. Each  $V_{DDP}/GND$  pin pair: 33&34/35, 43/42, 48/47, and 50/49 should be decoupled with a 100–1000p/10 $\mu$ F pair of capacitors (see Figure 31). If board space is limited, use as many capacitor pairs as possible.
4. Use Fair-rite 274 301 9447 bead.

## Firmware

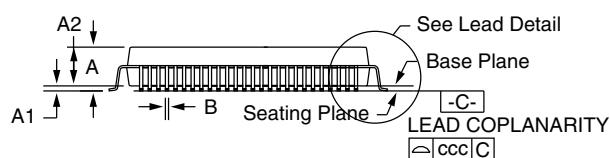
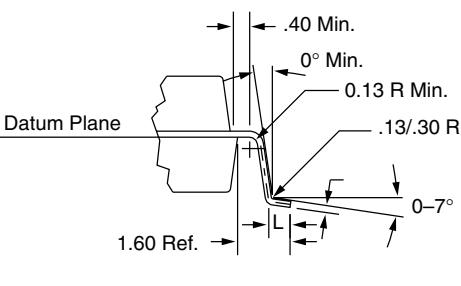
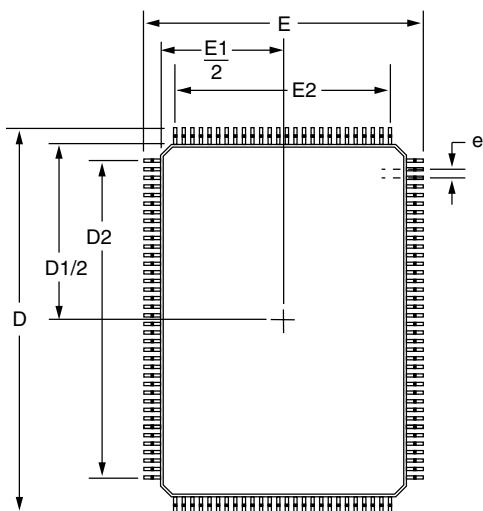
Best performance can be achieved by correctly setting the FMS9884A registers. Here are some recommendations:

1. Set the value of PLLN equal to the number of pixels to be sampled minus one. With this setting, the number of samples per horizontal line equals the number of pixels. If PLLN + 1 does not equal the number of pixels, there will be irregular intensities on text and an interference pattern on a vertical grill pattern.
2. Calibrate Offset and Gain by first setting each input to 0mV. Then adjust OSR, OSG, and OSB to set each RGB data output  $D_{7-0} = 0x00$ . Next with 700mV input, adjust GR, GG and GB so that each RGB data output  $D_{7-0} =$  (same value), typically 240 decimal.
3. Clamp registers, CD and CW, should be programmed to maximize the period of the clamp during the backporch, while not encroaching into the sync or active video periods.
4. PHASE must be trimmed to minimize onscreen snow (intensity noise) when a vertical grill pattern is displayed.
5. FVCO must be set to encompass the incoming frequency range.
6. IPUMP must be set to minimize intensity noise.
7. To ensure correct power-on defaults, program all registers including Test Register 0x0F, which must be set to 0x00 for normal operation. Note that unlike registers 0x00 through 0x0D, register 0x0F does not acknowledge. The ACK bit remains H instead of being pulled L.

## Mechanical Dimensions

### 128-Lead MQFP (KA) Package

| Symbol | Millimeters |      |      | Notes |
|--------|-------------|------|------|-------|
|        | Min.        | Typ. | Max  |       |
| A      | —           | 3.04 | 3.40 |       |
| A1     | 0.25        | 0.33 | —    |       |
| A2     | 2.57        | 2.71 | 2.87 | 3, 5  |
| D      | 22.60 BSC   |      |      |       |
| D1     | 20.00 BSC   |      |      |       |
| D2     | 18.00 BSC   |      |      |       |
| E      | 17.20 BSC   |      |      |       |
| E1     | 14.00 BSC   |      |      |       |
| E2     | 12.00 BSC   |      |      |       |
| L      | 0.65        | 0.70 | 0.95 | 4     |
| N      | 128         |      |      |       |
| e      | 0.50 BSC    |      |      |       |
| b      | 0.13        | —    | 0.28 |       |
| ccc    |             | 0.12 |      |       |



## Ordering Information

| Product Number | Temperature Range | Screening  | Package       | Package Marking |
|----------------|-------------------|------------|---------------|-----------------|
| FMS9884AKAC100 | 0°C to 70°C       | Commercial | 128 Lead MQFP | 9884AKAC100     |
| FMS9884AKAC140 |                   |            |               | 9884AKAC140     |
| FMS9884AKAC175 |                   |            |               | 9884AKAC175     |

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.