

**TOSHIBA**

**TMP47P870**

CMOS 4-BIT MICROCONTROLLER

**TMP47P870N**

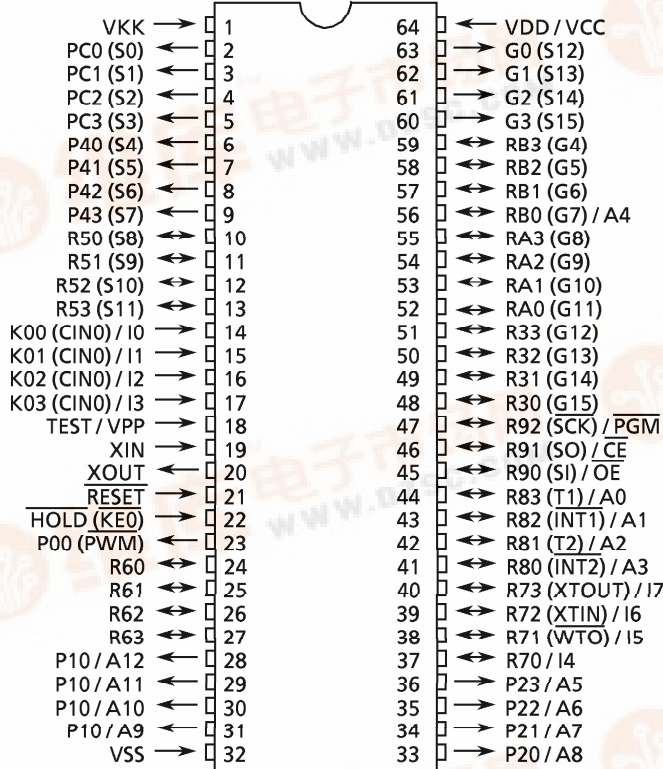
The 47P870N is the system evaluation LSI of 47C670/870 with 64K bits one-time PROM. The 47P870 programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764D.

In addition, the 47P870 and the 47C670/870 are pin compatible. The 47P870 operates as the same as 47C670/870 by programming to the internal PROM.

PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P870N	OTP 8192 x 8-bit	512 x 4-bit	SDIP64-P-750-1.78	BM1107A

**PIN ASSIGNMENT (TOP VIEW)**

SDIP64-P-750-1.78



**PIN FUNCTION**

The 47P870 has MCU mode and PROM mode.

(1) MCU mode

The 47C670/870 and the 47P870 are pin compatible (TEST pin for out-going test. Be fixed to low level.).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME (MCU MODE)
A12 - A9	Input	Address inputs	P10 - P13
A8 - A5			P20 - P23
A4			RB0
A3 - A0			R80 - R83
I7 - I4	I/O	Data outputs / inputs	R73 - R70
I3 - I0			K03 - K00
$\overline{\text{PGM}}$	Input	Program control input	R92
$\overline{\text{CE}}$		Chip Enable input	R91
$\overline{\text{OE}}$		Output Enable input	R90
VPP	Power supply	+ 21V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V (GND)	VSS
P00	Output	Open	
P43 - P40			
PC3 - PC0			
G3 - G0			
R32 - R30	I/O	Be fixed to low level.	
R53 - R50			
RB3 - RB1			
R63 - R60			
RA3, RA2			Open
RA1, RA0			
$\overline{\text{RESET}}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{\text{HOLD}}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		
VKK	Power supply	Open	

**OPERATIONAL DESCRIPTION**

The following is an explanation of hardware configuration and operation in relation to the 47P870. The 47P870 is the same as the 47C670/870 except that an OTP is used instead of a Mask ROM.

**1. OPERATION MODE**

The 47P870 has an MCU mode and a PROM mode.

**1.1 MCU mode**

The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C670 / 870, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

**1.1.1 Program Memory**

The program storage area is the same as for the 47C870. Data conversion tables must be set in two locations when using the 47P870 to check 47C670 operation.

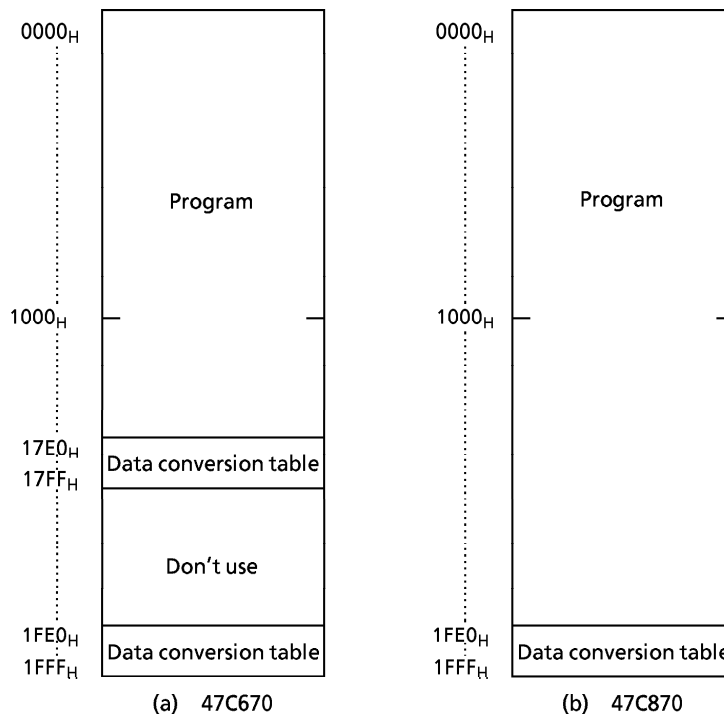


Figure 1-1. Program area

**1.1.2 Data Memory**

The 47P870 has 512 x 4-bit data memory banks (RAM).

When using the 47P870 as a 47C670 evaluator, do not write data to address 80H and following, even though the bank1 addresses are 00-FFH. There is no necessary to take into consideration a special function Shared area because one is built in bank0.

1.1.3 Input / Output Circuitry

(1) Control pins

This is the same as for the 47C670 / 870 except that there is no built in pull-down resistor for the TEST pin.

(2) I/O port

The input / output circuit of the 47P870 is the same as I/O code MA of the 47C670 / 870. External resistor, for example, is required when using as evaluator of other codes (MB, MC), (Refer to Figure1-2).



Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the  $\overline{\text{RESET}}$ ,  $\overline{\text{HOLD}}$ , RA0 and RA1 pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764D).

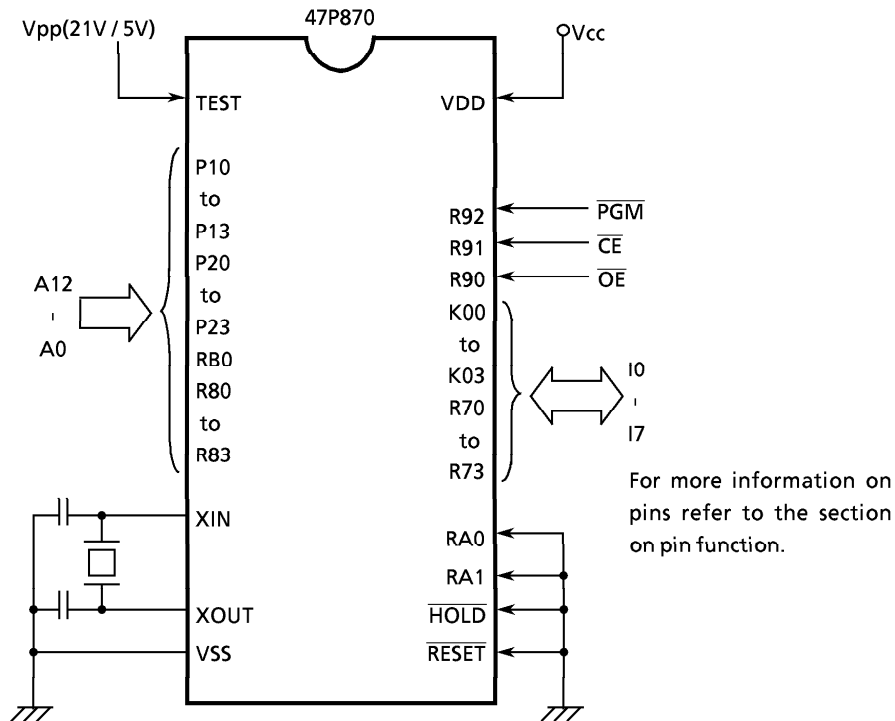


Figure 1-3. Setting for PROM mode

### 1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (21.0V) is applied to the Vpp terminal with Vcc = 6V and PGM = VIH4. The programming is achieved by applying a Single TTL low level 1 ms, pulse the PGM input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 15 times). After correctly programming the selected address, one additional program pulse with pulse width 4 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

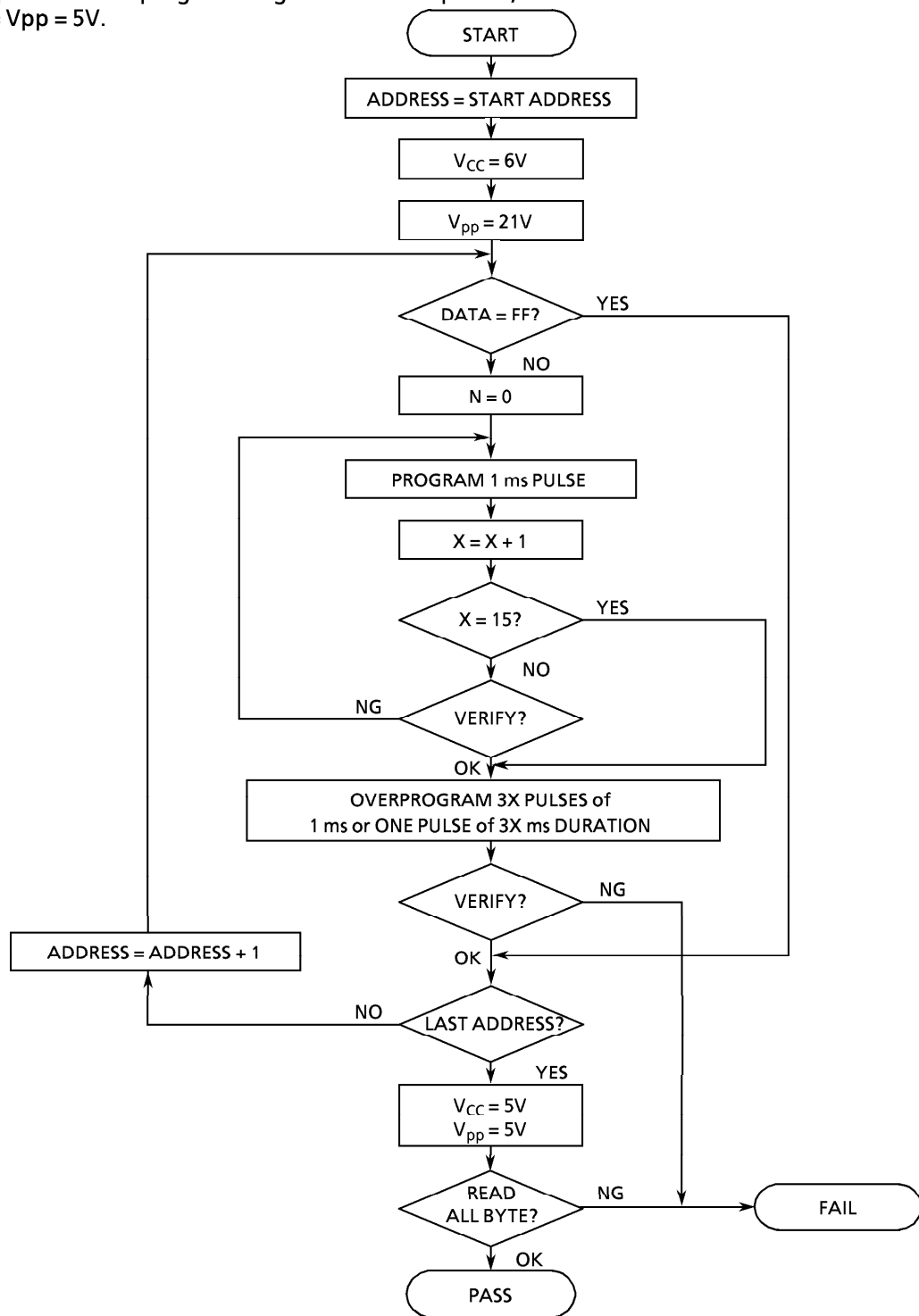


Figure1-4. FLOW CHART

## ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V<sub>SS</sub> = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V <sub>DD</sub>		- 0.3 to 7	V
Program Voltage	V <sub>PP</sub>	TEST / VPP pin	- 0.3 to 22.0	V
Input Voltage	V <sub>IN</sub>		- 0.3 to V <sub>DD</sub> + 0.3	V
Output Voltage	V <sub>OUT1</sub>	R7, XOUT	- 0.3 to V <sub>DD</sub> + 0.3	V
	V <sub>OUT2</sub>	Ports P0-P2, R6, R8, R9	- 0.3 to 10	
	V <sub>OUT3</sub>	Source open drain ports	- 35 to V <sub>DD</sub> + 0.3	
Output (per 1 pin)	I <sub>OUT1</sub>	Ports P1, P2	30	mA
	I <sub>OUT2</sub>	Ports P0, R6-R9	3.2	
	I <sub>OUT3</sub>	Ports P4, R5, PC	- 12	
	I <sub>OUT4</sub>	Ports R3, RA, RB, G / S	- 25	
Output Current (total)	ΣI <sub>OUT1</sub>	Ports P1, P2	120	mA
	ΣI <sub>OUT3</sub>	Ports R4, R5, RC	- 80	
	ΣI <sub>OUT4</sub>	Ports R3, RA, RB, G / S	- 100	
Power Dissipation [T <sub>opr</sub> = 70 °C]	PD		600	mW
Soldering Temperature (time)	T <sub>slid</sub>		260 (10s)	°C
Storage Temperature	T <sub>stg</sub>		- 55 to 125	°C
Operating Temperature	T <sub>opr</sub>		- 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V<sub>SS</sub> = 0V, T<sub>opr</sub> = - 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V <sub>DD</sub>		In the Normal mode	4.5	6.0	V
			In the SLOW mode			
			In the HOLD mode	2.0		
Input High Voltage	V <sub>IH1</sub>	Except Hysteresis Input	V <sub>DD</sub> ≥ 4.5V	V <sub>DD</sub> × 0.7	V <sub>DD</sub>	V
	V <sub>IH2</sub>	Hysteresis Input		V <sub>DD</sub> × 0.75		
	V <sub>IH3</sub>			V <sub>DD</sub> < 4.5V		
Input Low Voltage	V <sub>IL1</sub>	Hysteresis Input	V <sub>DD</sub> ≥ 4.5V	0	V <sub>DD</sub> × 0.3	V
	V <sub>IL2</sub>	Hysteresis Input			V <sub>DD</sub> × 0.25	
	V <sub>IL3</sub>				V <sub>DD</sub> < 4.5V	
Clock Frequency	f <sub>c</sub>	XIN, XOUT	High-freq.clock	0.4	6.0	MHz
	f <sub>s</sub>	XIN, XOUT	Low-freq.clock	30	34	kHz

Note. Input Voltage V<sub>IH3</sub>, V<sub>IL3</sub>: in the SLOW operation or HOLD operation

**D.C. CHARACTERISTICS** ( $V_{SS} = 0V$ ,  $T_{opr} = -40$  to  $70$  °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	$V_{HS}$	Hysteresis input		—	0.7	—	V
Input Current	$I_{IN1}$	Port K0, TEST, RESET, HOLD	$V_{DD} = 5.5V$	—	—	$\pm 2$	$\mu A$
	$I_{IN2}$	Ports R (open drain)	$V_{IN} = 5.5V / 0V$				
Input Resistance	$R_{IN2}$	RESET		100	220	450	$k\Omega$
Pull-down Resistance	$R_K$	Source open drain	$V_{DD} = 5.5V$ , $V_{KK} = -30V$	—	80	—	$k\Omega$
Output Leakage Current	$I_{LO1}$	Sink open drain ports	$V_{DD} = 5.5V$ , $V_{IN} = 5.5V$	—	—	2	$\mu A$
	$I_{LO2}$	Source open drain ports	$V_{DD} = 5.5V$ , $V_{OUT} = -32V$	—	—	-2	$\mu A$
Output Level High Voltage	$V_{OH}$	Ports P4, R5, PC	$V_{DD} = 4.5V$ , $I_{OH} = -5$ mA	2.4	—	—	V
Output Level Low Voltage	$V_{OL}$	Ports P0, R6 - R9	$V_{DD} = 4.5V$ , $I_{OL} = 1.6$ mA	—	—	0.4	
High Level Output Current	$I_{OH}$	Ports R3, RA, RB, G/S	$V_{DD} = 4.5V$ , $V_{OL} = 2.4V$	—	-15	—	mA
Low Level Output Current	$I_{OL}$	Ports P1, P2	$V_{DD} = 4.5V$ , $V_{OL} = 1.0V$	—	20	—	
Supply Current (in the Normal mode)	$I_{DD}$		$V_{DD} = 5.5V$ $f_c = 4$ MHz	—	5	10	mA
Supply Current (in the SLOW mode)	$I_{DDS}$		$V_{DD} = 5.0V$ $f_s = 32.768$ kHz	—	5	8	mA
Supply Current (in the HOLD mode)	$I_{DDH}$		$V_{DD} = 5.5V$	—	0.5	10	$\mu A$

Note 1. Typ. values show those at  $T_{opr} = 25$  °C,  $V_{DD} = 5V$ .

Note 2. Input Current  $I_{IN1}$ ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3.  $I_{DD}$ ,  $I_{DDH}$ ;  $V_{IN} = 5.3V / 0.2V$

The K0 port is opened when the input resistor is contained.

The voltage applied to the R port is within the valid range.

$I_{DDS}$ ;  $V_{IN} = 4.8V / 0.2V$ , low frequency clock is only oscillated (connecting XTIN, XTOUT)

**A / D CONVERSION CHARACTERISTICS** ( $V_{SS} = 0V$ ,  $V_{DD} = 4.5$  to  $6.0V$ ,  $T_{opr} = -40$  to  $70$  °C)

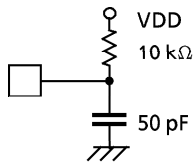
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog input Voltage	$V_{AIN}$	CIN3-CIN0	$V_{ASS}$	—	$V_{DD}$	V
Total Error			—	—	$\pm \frac{1}{2}$	LSB

**A.C. CHARACTERISTICS** ( $V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70\text{ }^\circ\text{C}$ )

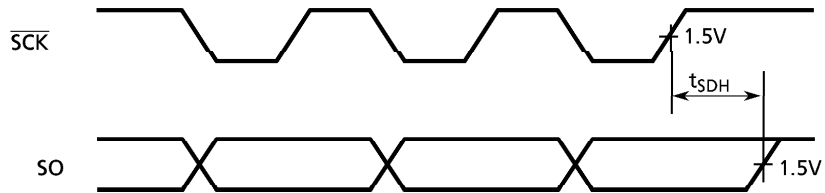
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	$t_{cy}$	In the Normal mode	1.3	–	20	$\mu\text{s}$
		In the SLOW mode	235	–	267	
High level Clock pulse Width	$t_{WCH}$	For external clock operation	80	–	–	ns
Low level Clock pulse Width	$t_{WCL}$					
Shift Data Hold Time	$t_{SDH}$		$0.5t_{cy} - 300$	–	–	ns

**Note. Shift Data Hold Time:**

External circuit  $\overline{\text{SCK}}$  pin and SO pin



Serial port (completion of transmission)



**RECOMMENDED OSCILLATING CONDITIONS** ( $V_{SS} = 0V, V_{DD} = 4.5 \text{ to } 6.0V, T_{opr} = -40 \text{ to } 70\text{ }^\circ\text{C}$ )

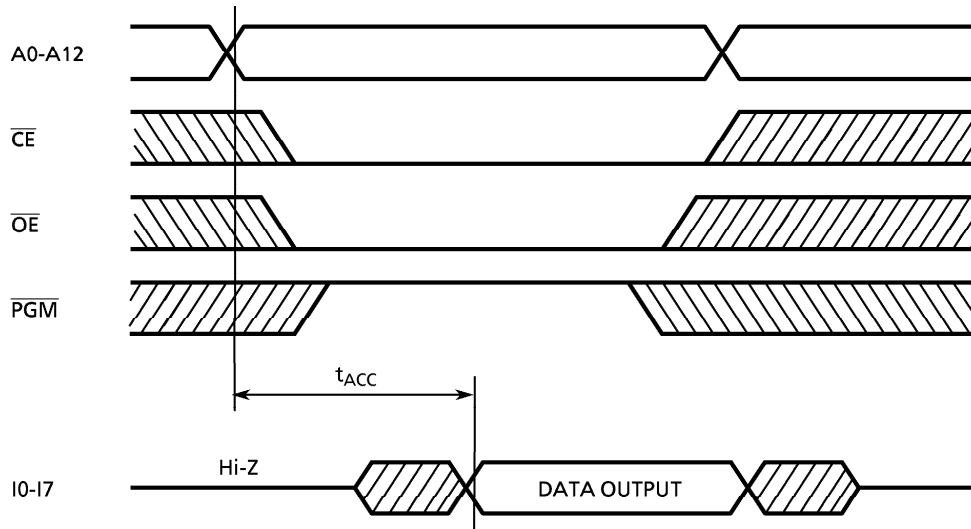
Recommended oscillating conditions of the 47P870 are equal to the 47C870's.

**D.C./A.C. CHARACTERISTICS** ( $V_{SS} = 0V$ )

(1) Read Operation

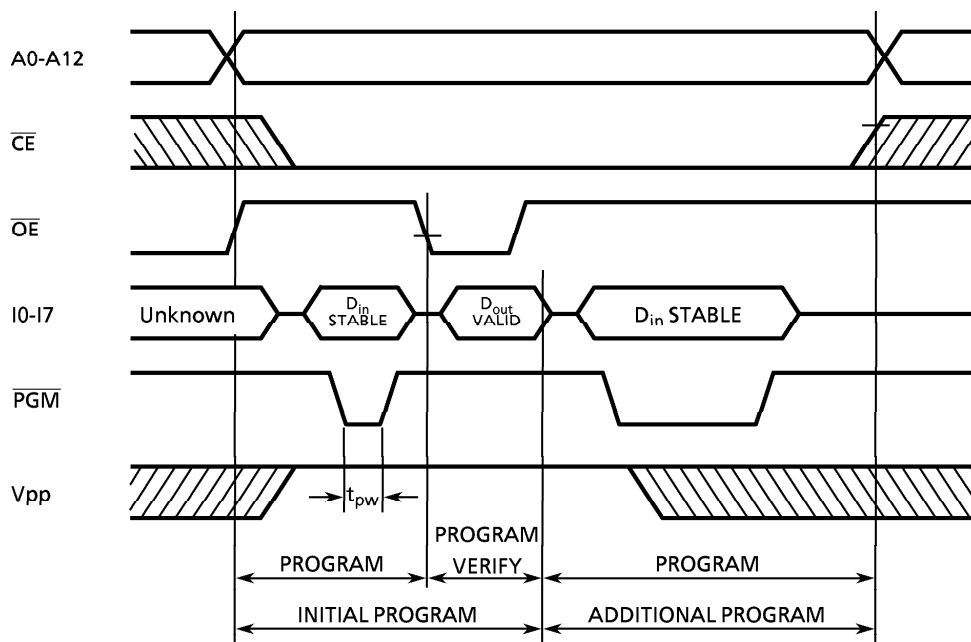
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	$V_{IH4}$		$V_{CC} \times 0.7$	–	$V_{CC}$	V
Output Level Low Voltage	$V_{IL4}$		0	–	$V_{CC} \times 0.12$	V
Supply Voltage	$V_{CC}$		4.75	–	6.0	V
Programming Voltage	$V_{PP}$					
Address Access Time	$t_{ACC}$	$V_{CC} = 5.0 \pm 0.25V$	0	–	350	ns





(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	$V_{IH4}$		$V_{CC} \times 0.7$	-	$V_{CC}$	V
Input Low Voltage	$V_{IL4}$		0	-	$V_{CC} \times 0.12$	V
Supply Voltage	$V_{CC}$		4.75	-	6.0	V
$V_{PP}$ Power Supply Voltage	$V_{PP}$		20.5	21.0	21.5	V
Programming Pulse Width	$t_{PW}$	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms



※ Difference compared with the 47C870N  
 The 47P870 is different from the 47C670/870 with respect to the following spec points.

PARAMETER	SYMBOL	CONDITION	47C870			47P870			UNIT
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage	$V_{DD}$	in the NORMAL OPERATION	4.5	—	6.0	4.5	—	6.0	V
		in the SLOW OPERATION	2.7	—					
Supply Current	$I_{DD}$	in the NORMAL OPERATION	—	3	6	—	5	10	mA
	$I_{DDS}$	in the SLOW OPERATION	—	30 $\mu$ A ( $V_{DD} = 3V$ )	60 $\mu$ A	—	5 mA ( $V_{DD} = 5V$ )	8 mA	—

Note. Be fixed low level at MCU mode because of TEST pin does not have pull-down resistor.

**TYPICAL CHARACTERISTICS**

