



# Dual Bipolar/JFET, Precision Operational Amplifier

T-79-15 OP-285\*

## FEATURES

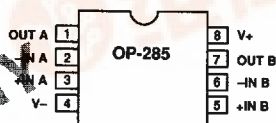
Low Offset Voltage: 250  $\mu$ V  
 Wide Bandwidth: 8 MHz  
 High Slew Rate: 20 V/ $\mu$ s  
 Low Noise: 6 nV/ $\sqrt{\text{Hz}}$   
 Low Distortion: 0.001%  
 Low Supply Current: 5 mA  
 Low Offset Current: 2 nA  
 Unity-Gain Stable

## APPLICATIONS

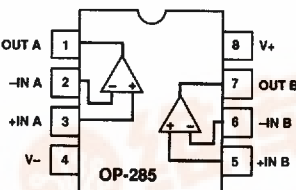
Active Filters  
 Fast Amplifiers  
 Integrators

## PIN CONNECTIONS

### 8-Lead Narrow-Body SOIC (S Suffix)



### 8-Lead Epoxy DIP (P Suffix)



## GENERAL DESCRIPTION

The OP-285 is a precision high speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP-285 is specified over the extended industrial ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) temperature range. OP-285s are available in plastic DIP plus SO-8 surface mount packages.

\*Patents pending.



**OP-285—SPECIFICATIONS****ELECTRICAL CHARACTERISTICS** (@  $V_S = \pm 15.0$  V,  $T_A = +25^\circ\text{C}$  unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$			125	250	$\mu\text{V}$
Input Bias Current	$I_B$	$V_{CM} = 0$ V		150		nA
Input Offset Current	$I_{OS}$	$V_{CM} = 0$ V		2		nA
Input Voltage Range	$V_{CM}$		-10.5		+10.5	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 10.5$ V	86			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 600 \Omega$		200		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			5		$\mu\text{V}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage Swing	$V_O$	$R_L = 10 \text{ k}\Omega$	-13	$\pm 14.1$	+13	V
Open Loop Output Resistance	$R_{OUT}$					$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5$ V to $\pm 15$ V		80		dB
Supply Current	$I_{SY}$	$V_O = 0$ V		4	5	mA
Supply Voltage Range	$V_S$				$\pm 18$	V
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 2 \text{ k}\Omega$		20		V/ $\mu\text{s}$
Full-Power Bandwidth	BW <sub>p</sub>					kHz
Settling Time	$t_s$					$\mu\text{s}$
Gain Bandwidth Product	GBP			8		MHz
Total Harmonic Distortion	THD	@ 20 kHz		0.002		%
		@ 1 kHz		0.0006		%
Phase Margin	$\theta_0$			62		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	0.1 Hz to 10 Hz		1.1		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1 \text{ kHz}$		6		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1 \text{ kHz}$		1.5		pA/ $\sqrt{\text{Hz}}$

Specifications subject to change without notice.

T-79-15

OP-285

**WAFER TEST LIMITS** @  $V_s = \pm 15.0$  V,  $T_A = +25^\circ\text{C}$  unless otherwise specified.)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	$V_{OS}$		250	mV max
Input Bias Current	$I_B$	$V_{CM} = 0$ V	200	nA max
Input Offset Current	$I_{OS}$	$V_{CM} = 0$ V	50	nA max
Input Voltage Range <sup>1</sup>			$\pm 10.5$	V min
Common-Mode Rejection	CMRR	$V_{CM} = \pm 10.5$ V	86	dB min
Power Supply Rejection Ratio	PSRR	$V = \pm 4.5$ V to $\pm 15$ V	80	dB min
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10$ k $\Omega$	100	V/mV min
Output Voltage Range	$V_O$	$R_L = 10$ k $\Omega$	$\pm 13$	V min
Supply Current	$I_{SY}$	$V_O = 0$ V, $R_L = \infty$	5	mA max

**NOTE**

Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods, normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on die lot quantities through sample lot assembly and testing.

<sup>1</sup>Guaranteed by CMR test.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Supply Voltage	$\pm 18$ V
Input Voltage <sup>2</sup>	$\pm 18$ V
Differential Input Voltage <sup>2</sup>	$\pm 7.5$ V
Output Short-Circuit Duration	Limited
Storage Temperature Range	
P, S Package	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	
OP-285E, F	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Junction Temperature Range	
P, S Package	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature Range (Soldering, 60 Sec)	$+300^\circ\text{C}$

Package Type	$\theta_{JA}$ <sup>3</sup>	$\theta_{JC}$	Units
8-Pin Plastic DIP (P)	103	43	$^\circ\text{C/W}$
8-Pin SOIC (S)	158	43	$^\circ\text{C/W}$

**NOTES**

<sup>1</sup>Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

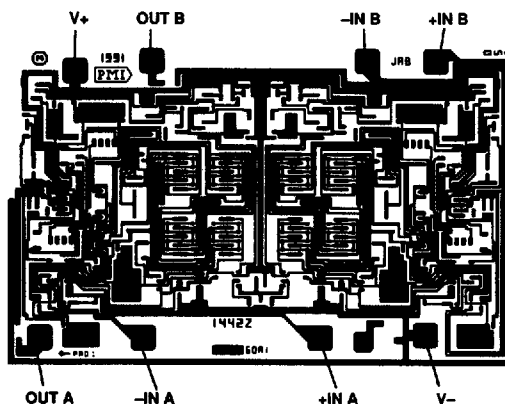
<sup>2</sup>For supply voltages less than  $\pm 18$  V, the absolute maximum input voltage is equal to the supply voltage.

<sup>3</sup> $\theta_{JA}$  is specified for the worst case conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for cerdip, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered in circuit board for SOIC package.

**ORDERING GUIDE**

Model	Temperature Range	Package Option*
OP285EP	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin Plastic DIP
OP285ES	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin SOIC
OP285FP	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin Plastic DIP
OP285FS	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	8-Pin SOIC
OP285GBC	$+25^\circ\text{C}$	DICE

\*For outline information see Package Information section.

**DICE CHARACTERISTICS**

OP-285 Die Size 0.070 in.  $\times$  0.108 in. (7,560 sq. mils)