INTEGRATED CIRCUITS

DATA SHEET

TDA9887TS

I²C-bus controlled multistandard alignment-free IF-PLL demodulator with FM radio

Product specification 2002 Mar 05

Philips Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- 5 V supply voltage
- Gain controlled wide-band Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF Voltage Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I^{2}C-bus
- Digital acquisition help, VIF frequencies of 33.4, 33.9, 38.0, 38.9, 45.75, and 58.75 MHz
- 4 MHz reference frequency input: signal from Phase-Locked Loop (PLL) tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals on pin OTP2
- External AGC setting via pin OP1
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I^{2}C-bus
- TakeOver Point (TOP) adjustable via I^{2}C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5, 5.5, 6.0, and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
- SIF-AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I^{2}C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise
- I^{2}C-bus control for all functions
- I^{2}C-bus transceiver with pin programmable Module Address (MAD)
- Four I^{2}C-bus addresses via MAD
- SIF and FM-AGC for radio (optional)
- Radio IF (RIF) input using the sound IF SAW input for converting to 10.7 MHz, input frequencies are 41.3 MHz for NTSC (M/N standard) applications and 33.3 MHz for other applications
- Alignment-free FM radio demodulation at 10.7 MHz
- Radio AFC
- External FM input and demodulation.

2 GENERAL DESCRIPTION

The TDA9887TS is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing. A special function is implemented for the demodulation of FM radio signals (f_{RIF} = 10.7 MHz).

3 APPLICATIONS

- TV, VTR, PC, and STB applications.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9887TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	notes 1 and 2	4.5	5.0	5.5	V
I_P	supply current		52	63	70	mA
Video part						
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	–1 dB video at output	–	60	100	µV
$G_{VIF(cr)}$	VIF gain control range		60	66	–	dB
f_{VIF}	vision carrier operating frequencies	see Table 17	–	33.4	–	MHz
			–	33.9	–	MHz
			–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Fig.9	–	±2.3	–	MHz
$V_{o(video)(p-p)}$	video signal output voltage (peak-to-peak value)	see Fig.3				
		normal mode	1.7	2.0	2.3	V
		trap bypass mode	0.95	1.10	1.25	V
G_{dif}	differential gain	*"CCIR 330"*; note 3				
		B/G standard	–	–	5	%
		L standard	–	–	7	%
φ_{dif}	differential phase	*"CCIR 330"*	–	2	4	deg
$B_{video(-1dB)}$	–1 dB video bandwidth	trap bypass mode; AC load; C_L < 20 pF; R_L > 1 kΩ	5	6	–	MHz
$B_{video(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	note 4				
		f_{trap} = 4.5 MHz	3.95	4.05	–	MHz
		f_{trap} = 5.5 MHz	4.90	5.00	–	MHz
		f_{trap} = 6.0 MHz	5.40	5.50	–	MHz
		f_{trap} = 6.5 MHz	5.50	5.95	–	MHz
α_{SC1}	trap attenuation at first sound carrier	M/N standard	30	36	–	dB
		B/G standard	30	36	–	dB
$S/N_{W(video)}$	weighted signal-to-noise ratio of video signal	see Fig.11; note 5	56	59	–	dB
$PSRR_{CVBS}$	power supply ripple rejection at pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Fig.4	20	25	–	dB
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{VIF}$	0.85	1.05	1.25	µA/kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio part						
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	27 kHz FM deviation; 50 µs de-emphasis	430	540	650	mV
THD	total harmonic distortion of audio signal	FM: 27 kHz FM deviation; 50 µs de-emphasis	–	0.15	0.50	%
		AM: m = 54%	–	0.5	1.0	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; dependent on FM-PLL filter	80	100	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM: 27 kHz FM deviation; 50 µs de-emphasis; vision carrier unmodulated	52	56	–	dB
		AM: m = 54%	45	50	–	dB
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	50 µs de-emphasis; AM: f = 1 kHz and m = 54%; referenced to 27 kHz FM deviation	40	46	–	dB
$PSRR_{AUD}$	power supply ripple rejection on pin AUD	f_{ripple} = 70 Hz; see Fig.4				
		for AM	20	26	–	dB
		for FM	14	20	–	dB
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; SC_1; SC_2 off; note 6	–	–	–	mV
Radio part						
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{RIF}$	0.85	1.05	1.25	µA/kHz
$V_{i(FM)(rms)}$	IF intercarrier input level on pin FMIN for gain controlled operation of FM-PLL (RMS value)	radio mode and FM external mode; see Table 16	1	–	100	mV
Reference frequency						
f_{ref}	reference signal frequency	note 7	–	4	–	MHz
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal	80	–	400	mV

Notes

1. Values of video and sound parameters can be decreased at V_P = 4.5 V.
2. For applications without I^2C-bus, the time constant (R × C) at the supply must be >1.2 µs (e.g. 1 Ω and 2.2 µF).
3. Condition: luminance range (5 steps) from 0% to 100%.
4. AC load: C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on the TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; $|H(s)|$ is the absolute value of transfer function).
5. $S/N_{W(video)}$ is the ratio of the black-to-white amplitude to the black level noise voltage (RMS value measured on pin CVBS). B = 5 MHz weighted in accordance with *"CCIR 567"*.

6. The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)} = 1.1\ V\ (p\text{-}p) \times \frac{1}{2\sqrt{2}} \times 10^{\frac{\frac{V_{i(SC)}}{V_{i(PC)}}(dB) + 6\ dB\ \pm 3\ dB}{20}}\ (RMS)$$

where:

$\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(dB)$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

7. Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

6 BLOCK DIAGRAM

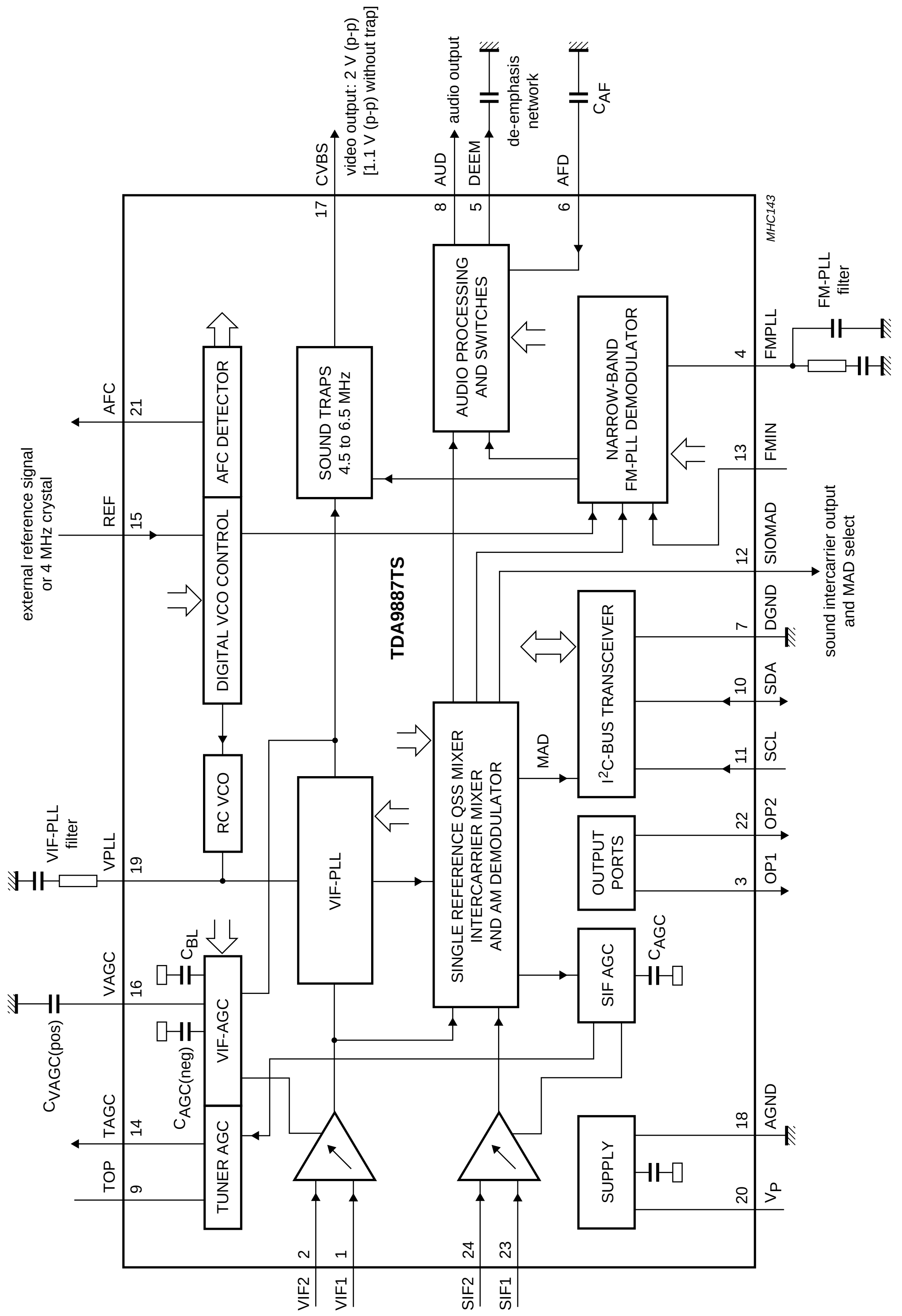


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
VIF1	1	VIF differential input 1
VIF2	2	VIF differential input 2
OP1	3	output port 1; open-collector
FMPLL	4	FM-PLL for loop filter
DEEM	5	de-emphasis output for capacitor
AFD	6	AF decoupling input for capacitor
DGND	7	digital ground
AUD	8	audio output
TOP	9	tuner AGC TakeOver Point (TOP) for resistor adjustment
SDA	10	I^2C-bus data input and output
SCL	11	I^2C-bus clock input
SIOMAD	12	sound intercarrier output and MAD select with resistor
FMIN	13	radio IF and external second SIF input
TAGC	14	tuner AGC output
REF	15	4 MHz crystal or reference signal input
VAGC	16	VIF-AGC for capacitor
CVBS	17	composite video output
AGND	18	analog ground
VPLL	19	VIF-PLL for loop filter
V_P	20	supply voltage
AFC	21	AFC output
OP2	22	output port 2; open-collector
SIF1	23	SIF differential input 1 and MAD select with resistor
SIF2	24	SIF differential input 2 and MAD select with resistor

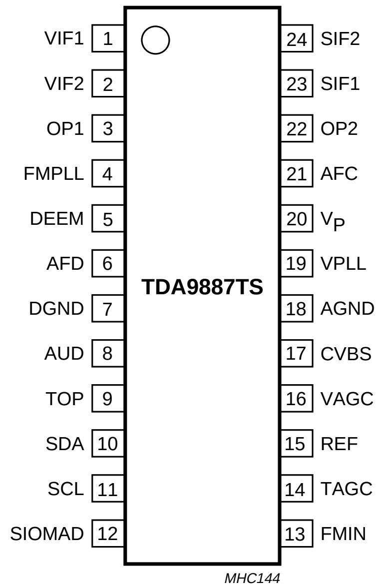


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

Figure 1 shows the simplified block diagram of the device which comprises the following functional blocks:

1. VIF amplifier
2. Tuner AGC and VIF-AGC
3. VIF-AGC detector
4. Frequency Phase-Locked Loop (FPLL) detector
5. VCO and divider
6. AFC and digital acquisition help
7. Video demodulator and amplifier
8. Sound carrier trap
9. SIF amplifier
10. SIF-AGC detector
11. Single reference QSS mixer
12. AM demodulator
13. FM demodulator and acquisition help
14. Audio amplifier and mute time constant
15. Radio mode
16. Internal voltage stabilizer
17. I^{2}C-bus transceiver and MAD (module address).

8.1 VIF amplifier

The VIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. The total gain control range is typical 66 dB. The differential input impedance is typical 2 kΩ in parallel with 3 pF.

8.2 Tuner AGC and VIF-AGC

This block adapts the voltages, generated at the VIF-AGC and SIF-AGC detectors, to the internal signal processing at the VIF and SIF amplifiers and performs the tuner AGC control current generation. The onset of the tuner AGC control current generation can be set either via the I^{2}C-bus (see Table 13) or optional by a potentiometer at pin TOP (in case that the I^{2}C-bus information cannot be stored, related to the device). The presence of a potentiometer will automatically be detected and disables the I^{2}C-bus setting.

Furthermore, derived from the AGC detector voltage, a comparator is used to test the corresponding VIF input voltage to be higher than 200 μV. This information can be read out via the I^{2}C-bus (bit VIFLEV = 1).

8.3 VIF-AGC detector

Gain control is performed by sync level detection (negative modulation) or peak white detection (positive modulation).

For negative modulation, the sync level voltage is stored at an integrated capacitor by means of a fast peak detector. This voltage is compared with a reference voltage (nominal sync level) by a comparator which charges or discharges the integrated AGC capacitor for the generation of the required VIF gain. The time constants for decreasing or increasing the gain are nearly equal and the total AGC reaction time is fast to cope with ‘aeroplane fluttering’.

For positive modulation, the white peak level voltage is compared with a reference voltage (nominal white level) by a comparator which charges (fast) or discharges (slow) the external AGC capacitor directly for the generation of the required VIF gain. The need of a very large time constant for VIF gain increase is caused by the fact that the peak white level may appear only once in a field. In order to reduce this time constant, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step controlled by the detected actual black level voltage. The threshold level for fast mode AGC is typical −6 dB video amplitude. The fast mode state is also transferred to the SIF-AGC detector for speed-up. In case of missing peak white pulses, the VIF gain increase is limited to typical +3 dB by comparing the detected actual black level voltage with a corresponding reference voltage.

8.4 FPLL detector

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier for removing the video AM.

During acquisition the frequency detector produces a current proportional to the frequency difference between the VIF and the VCO signal. After frequency lock-in the phase detector produces a current proportional to the phase difference between the VIF and the VCO signal. The currents from the frequency and phase detector are charged into the loop filter which controls the VIF VCO and locks it to the frequency and phase of the VIF carrier.

For a positive modulated VIF signal, the charging currents are gated by the composite sync in order to avoid signal distortion in case of overmodulation. The gating depth is switchable via the I^{2}C-bus.

8.5 VCO and divider

The VCO of the VIF-FPLL operates as an integrated low radiation relaxation oscillator at double the picture carrier frequency. The control voltage, required to tune the VCO to actually double the picture carrier frequency, is generated at the loop filter by the frequency phase detector. The possible frequency range is 50 to 140 MHz (typical value).

The oscillator frequency is divided-by-two for providing two differential square wave signals with exactly 90 degrees phase difference, independent of the frequency, for use in the FPLL detectors, the video demodulator and the intercarrier mixer.

8.6 AFC and digital acquisition help

Each relaxation oscillator of the VIF-PLL and FM-PLL demodulator has a wide frequency range. To prevent false locking of the PLLs and with respect to the catching range, the digital acquisition help provides an individual control, until the frequency of the VCO is within the preselected standard dependent lock-in window of the PLL.

The in-window and out-window control at the FM-PLL is additionally be used to mute the audio stage (if auto mute is selected via the I²C-bus).

The principle working of the digital acquisition help is as following. The PLL VCO output is connected to a down counter which has a predefined start value (standard dependent). The VCO frequency clocks the down counter for a fixed gate time. Thereafter, the down counter stop value is analysed. In case the stop value is higher (lower) than the expected value range, the VCO frequency is lower (higher) than the wanted lock-in window frequency range. A positive (negative) control current is injected into the PLL loop filter and consequently the VCO frequency will be increased (decreased) and a new counting cycle starts.

The gate time as well as the control logic of the acquisition help circuit is dependent on the precision of the reference signal at pin REF. Operation as crystal oscillator is possible as well as connecting this input via a serial capacitor to an external reference frequency e.g. the tuning system oscillator.

The AFC signal is derived from the corresponding down counter stop value after a counting cycle. The last four bits are latched and can be read out via the I²C-bus (see Table 7). Also the digital-to-analog converted value is given as current at pin AFC.

8.7 Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The VIF signal is multiplied with the ‘in phase’ signal of the VIF-PLL VCO.

The demodulator output signal is fed into the video preamplifier via a level shift stage with integrated low-pass filter to achieve carrier harmonics attenuation.

The output signal of the preamplifier is fed to the VIF-AGC detector (see Section 8.3) and in the sound trap mode also fed internally to the integrated sound carrier trap (see Section 8.8). The differential trap output signal is converted and amplified by the following postamplifier. The video output level at pin CVBS is 2 V (p-p).

In the bypass mode the output signal of the preamplifier is fed directly through the postamplifier to pin CVBS. The output video level is 1.1 V (p-p) for using an external sound trap with 10% loss over all.

Noise clipping is provided in both cases.

8.8 Sound carrier trap

The sound carrier trap consists of a reference filter, a phase detector and the sound trap itself.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces a DC voltage by charging or discharging an integrated capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage controls the frequency position of the reference filter and the sound trap. So the accurate frequency position for the different standards is set by the sound carrier reference signal.

The sound trap itself is constructed of three separate traps to realize sufficient suppression of the first and second sound carrier.

8.9 SIF amplifier

The SIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration. The total gain control range is typical 66 dB. The differential input impedance is typical 2 kΩ in parallel with 3 pF.

8.10 SIF-AGC detector

SIF gain control is performed by the detection of the DC component of the AM demodulator output signal. This DC signal is directly corresponding to the SIF voltage at the output of the SIF amplifier so that a constant SIF signal is supplied to the AM demodulator and to the single reference QSS mixer.

By switching the gain of the input amplifier of the SIF-AGC detector via the I^2C-bus, the internal SIF level for FM sound is 5.5 dB lower than for AM sound. This is done to adapt the SIF-AGC characteristic to the VIF-AGC characteristic. The adaption is ideal for a picture-to-sound FM carrier ratio of 13 dB.

Via a comparator the integrated AGC capacitor is charged or discharged for the generation of the required SIF gain. Due to AM sound, the AGC reaction time is slow (f_c < 20 Hz for the closed AGC loop). For reducing this AM sound time constant in the event of a decreasing IF amplitude step, the load current of the AGC capacitor is increased (fast mode) when the VIF-AGC detector (at positive modulation mode) operates in the fast mode too. An additional circuit (threshold approximately 7 dB) ensures a very fast gain reduction for a large increasing IF amplitude step.

8.11 Single reference QSS mixer

With the present system a high performance Hi-Fi stereo sound processing can be achieved. For a simplified application without a SIF SAW filter, the single reference QSS mixer can be switched to the intercarrier mode via the I^2C-bus.

The single reference QSS mixer generates the 2nd FM TV sound intercarrier signal. It is realized by a linear multiplier which multiplies the SIF amplifier output signal and the VIF-PLL VCO signal (90 degrees output) which is locked to the picture carrier. By this way the QSS mixer operates as a quadrature mixer in the intercarrier mode and provides suppression of the low frequency video signals.

The QSS mixer output signal is fed internally via a high-pass and low-pass combination to the FM demodulator as well as via an operational amplifier to the intercarrier output pin SIOMAD.

8.12 AM demodulator

The amplitude modulated SIF amplifier output signal is fed both to a two-stage limiting amplifier for removing the AM and to a linear multiplier. The result of the multiplication of the SIF signal with the limiter output signal is AM demodulation (passive synchronous demodulator). The demodulator output signal is fed via a low-pass filter for the attenuation of carrier harmonics and via the input amplifier of the SIF-AGC detector to the audio amplifier.

8.13 FM demodulator and acquisition help

The narrow-band FM-PLL detector consists of:

- Gain controlled FM amplifier and AGC detector
- Narrow-band PLL.

The intercarrier signal from the intercarrier mixer or from pin FMIN is fed to the input of an AC-coupled gain controlled amplifier with two stages. The gain controlled output signal is fed to the phase detector of the narrow-band FM-PLL (FM demodulator). For good selectivity and robustness against disturbance caused by the video signal, a high linearity of the gain controlled FM amplifier and of the phase detector as well as a constant signal level are required. The gain control is done by means of an ‘in phase’ demodulator for the FM carrier (from the output of the FM amplifier). The demodulation output is fed into a comparator for charging or discharging the integrated AGC capacitor. This leads to a mean value AGC loop to control the gain of the FM amplifier

The FM demodulator is realized as a narrow-band PLL with an external loop filter, which provides the necessary selectivity (bandwidth approximately 100 kHz). To achieve good selectivity, a linear phase detector and a constant input level are required. The gain controlled intercarrier signal from the FM amplifier is fed to the phase detector. The phase detector controls via the loop filter the integrated low radiation relaxation oscillator. The designed frequency range is from 4 to 7 MHz.

The VCO within the FM-PLL is phase-locked to the incoming 2nd SIF signal, which is frequency modulated. On to this fact, the VCO control voltage is superimposed by the AF voltage. Therefore, the VCO tracks with the FM of the 2nd SIF signal. So, the AF voltage is present at the loop filter and is typically 5 mV (RMS) for 27 kHz FM deviation. This AF signal is fed via a buffer to the audio amplifier.

The correct locking of the PLL is supported by the digital acquisition help circuit (see Section 8.6).

8.14 Audio amplifier and mute time constant

The audio amplifier consists of two parts:

- AF preamplifier
- AF output amplifier.

The AF preamplifier used for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator is 5 mV (RMS) for frequency deviation of 27 kHz and is amplified by 30 dB. By the use of a DC operating point control circuit (with external capacitor C_{AF}), the AF preamplifier is decoupled from the PLL DC voltage. The low-pass characteristic of the amplifier reduces the harmonics of the sound intercarrier signal at the AF output terminal.

For FM sound a switchable de-emphasis network (with external capacitor) is implemented between the preamplifier and the output amplifier.

The AF output amplifier provides the required AF output level by a rail-to-rail output stage. A preceding stage makes use of an input selector for switching between FM sound, AM sound and mute state. The gain can be switched between 10 dB (normal) and 4 dB (reduced).

Switching to the mute state is controlled automatically, dependent on the digital acquisition help for the case the VCO of the FM-PLL is not in the required frequency window. This is done by a time constant: fast for switching to the mute state and slow (typically 40 ms) for switching to the no-mute state.

All switching functions are controlled via the I²C-bus:

- AM sound, FM sound and forced mute
- Auto mute enable or disable
- De-emphasis off or on with 50 or 75 μs
- Audio gain normal or reduced.

8.15 Radio mode

The principle is to multiply the first radio IF (e.g. 33.3 MHz at tuner output) with 44 MHz reference signal. The result of the down-conversion is the second radio IF (10.7 MHz) at intercarrier output.

In the radio mode the tuner delivers a first radio IF signal of 33.3 MHz. This signal is fed via the SIF SAW filter (conventional used for QSS TV sound processing) to the SIF input. The sound IF amplifier supplies this radio IF signal by means of gain control with constant level to the QSS mixer. The single reference QSS mixer generates the second radio IF signal of 10.7 MHz. In the radio mode the VIF VCO operates as part of a frequency synthesizer and delivers a constant 44 MHz signal (derived from the reference signal of 4 MHz) for the down-conversion of the first radio IF to 10.7 MHz. This signal is fed via the external ceramic band-pass filter to the FM demodulator. The demodulated AF signal is amplified by the audio amplifier.

In case of NTSC application (M/N standard) the internal mixing frequency is 52 MHz. So, the first radio IF has to be 41.3 MHz.

For tuning search mode, the device offers certain monitoring functions. Switchable are radio AFC, FM-AGC or SIF-AGC to pin AFC.

8.16 Internal voltage stabilizer

The band gap circuit internally generates a voltage of approximately 2.4 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

8.17 I²C-bus transceiver and module address

The device can be controlled via the 2-wire I²C-bus by a microcontroller. Two wires carry serial data (SDA) and serial clock (SCL) information between the devices connected to the I²C-bus.

The device has an I²C-bus slave transceiver with auto-increment. The circuit operates up to clock frequencies of 400 kHz.

A slave address is sent from the master to the slave receiver. To avoid conflicts in a real application with other devices providing similar or complementing functions, there are four possible slave addresses available. These Module Addresses (MADs) can be selected by connecting resistors on pin SIOMAD and/or pins SIF1 and SIF2 (see Fig.23). Pin SIOMAD relates with bit A0 and pins SIF1 and SIF2 relate with bit A3. The slave addresses of this device are given in Table 1.

The power-on preset value is dependent on the use of pin SIOMAD and can be chosen for 45.75 MHz NTSC as default (pin SIOMAD left open-circuit) or 58.75 MHz NTSC (resistor on pin SIOMAD). In this way the device can be used without the I²C-bus as an NTSC only device.
Remark: In case of using the device without the I²C-bus, then the rise time of the supply voltage after switching on power must be longer than 1.2 μs.

Table 1 Slave address detection

SLAVE ADDRESS	SELECTABLE ADDRESS BIT		RESISTOR ON PIN	
	A3	A0	SIF1 AND SIF2	SIOMAD
MAD1	0	1	no	no
MAD2	0	0	no	yes
MAD3	1	1	yes	no
MAD4	1	0	yes	yes

9 I²C-BUS CONTROL

9.1 Read format

Table 2 I²C-bus read format (slave transmits data)

S	BYTE 1								A	BYTE 2								AN	P
	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$		D7	D6	D5	D4	D3	D2	D1	D0		
	slave address							1		data									

Table 3 Explanation of Table 2

SYMBOL	FUNCTION
S	START condition, generated by the master
Slave address	see Table 4
R/$\overline{W}$ = 1	read command, generated by the master
A	acknowledge bit, generated by the slave
Data	8-bit data word, transmitted by the slave (see Table 5)
AN	acknowledge-not bit, generated by the master
P	STOP condition, generated by the master

The master generates an acknowledge when it has received the dataword READ. The master next generates an acknowledge, then slave begins transmitting the dataword READ, and so on until the master generates an acknowledge-not bit and transmits a STOP condition.

9.1.1 SLAVE ADDRESS

The first module address MAD1 is the standard address (see Table 1).

Table 4 Slave addresses; notes 1 and 2

SLAVE ADDRESS		BIT						
NAME	**VALUE (HEX)**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
MAD1	43	1	0	0	0	0	1	1
MAD2	42	1	0	0	0	0	1	0
MAD3	4B	1	0	0	1	0	1	1
MAD4	4A	1	0	0	1	0	1	0

Notes

1. For MAD activation via external resistor: see Table 1 and Fig.23.
2. For applications without I²C-bus: see Tables 18 and 19.

9.1.2 DATA BYTE

Table 5 Data read register (status register)

MSB			BIT				LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AFCWIN	VIFLEV	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 6 Description of status register bits

BIT	VALUE	DESCRIPTION
AFCWIN		**AFC window**
	1	VCO in ±1.6 MHz AFC window; note 1
	0	VCO out of ±1.6 MHz AFC window
VIFLEV		**VIF input level**
	1	high level; VIF input voltage ≥200 μV (typically)
	0	low level
CARRDET		**FM carrier detection**
	1	detection
	0	no detection
AFC[4:1]		**Automatic frequency control**
		see Table 7
PONR		**Power-on reset**
	1	after power-on reset or after supply breakdown
	0	after a successful reading of the status register

Note

1. If no IF input is applied, then bit AFCWIN = 1 due to the fact that the VCO is forced to the AFC window border for fast load-in behaviour.

Table 7 Automatic frequency control bits; note 1

BIT				f_{VIF}
AFC4	**AFC3**	**AFC2**	**AFC1**	
0	1	1	1	≤ (f_0 – 187.5 kHz)
0	1	1	0	f_0 – 162.5 kHz
0	1	0	1	f_0 – 137.5 kHz
0	1	0	0	f_0 – 112.5 kHz
0	0	1	1	f_0 – 87.5 kHz
0	0	1	0	f_0 – 62.5 kHz
0	0	0	1	f_0 – 37.5 kHz
0	0	0	0	f_0 – 12.5 kHz
1	1	1	1	f_0 + 12.5 kHz
1	1	1	0	f_0 + 37.5 kHz
1	1	0	1	f_0 + 62.5 kHz
1	1	0	0	f_0 + 87.5 kHz
1	0	1	1	f_0 + 112.5 kHz
1	0	1	0	f_0 + 137.5 kHz
1	0	0	1	f_0 + 162.5 kHz
1	0	0	0	≥ (f_0 + 187.5 kHz)

Note

1. f_0 is the nominal frequency of f_{VIF}.

9.2 Write format

Table 8 I^2C-bus write format (slave receives data); note 1

S	BYTE 1		A	BYTE 2	A	BYTE 3	A	BYTE n	A	P
	A6 to A0	$R/\overline{W}$		A7 to A0		bits 7 to 0		bits 7 to 0		
	slave address	0		subaddress		data 1		data n		

Note

1. The auto-increment of the subaddress stops, if the subaddress is 3.

Table 9 Explanation of Table 8

SYMBOL	FUNCTION
S	START condition, generated by the master
Slave address	see Table 4
$R/\overline{W}$ = 0	write command, generated by the master
A	acknowledge bit, generated by the slave
Subaddress (SAD)	see Table 10
Data 1, data n	8-bit data words, transmitted by the master (see Tables 11, 12 and 14)
P	STOP condition

9.2.1 SUBADDRESS

If more than 1 data byte is transmitted, then auto-increment is performed: starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 10.

Table 10 Definition of the subaddress (second byte after slave address); note 1

REGISTER	MSB			BIT				LSB
	A7(2)	**A6**(3)	**A5**(3)	**A4**(3)	**A3**(3)	**A2**(3)	**A1**	**A0**
SAD for switching mode	0	X	X	X	X	X	0	0
SAD for adjust mode	0	X	X	X	X	X	0	1
SAD for data mode	0	X	X	X	X	X	1	0

Notes

1. X = don't care.
2. Bit A7 = 1 is not allowed.
3. Bits A6 to A2 will be ignored by the internal hardware.

9.2.2 DATA BYTE FOR SWITCHING MODE

Table 11 Bit description of SAD register for switching mode (SAD = 00)

BIT	VALUE	DESCRIPTION
7		**Output port 2 for SAW switching or monitoring**
	1	high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
6		**Output port 1 for SAW switching or external input**
	1	high-impedance, disabled or HIGH
	0	low-impedance, active or LOW
5		**Forced audio mute**
	1	on
	0	off
4 and 3		**TV standard modulation and radio mode**
	00	positive AM TV; note 1
	01	FM radio; note 2
	10	negative FM TV
	11	FM radio; note 2
2		**Carrier mode**
	1	QSS mode
	0	intercarrier mode

BIT	VALUE	DESCRIPTION
1		**Mute of FM AF outputs**
	1	active
	0	inactive
0		**Video mode (sound trap)**
	1	sound trap bypass
	0	sound trap active

Notes

1. For positive AM TV choose 6.5 MHz for the second SIF.
2. For FM radio, select f_{VIF} = 45.75 MHz for NTSC applications; otherwise use an arbitrary video IF (see Table 17).

9.2.3 DATA BYTE FOR ADJUST MODE

Table 12 Bit description of SAD register for adjust mode (SAD = 01)

BIT	VALUE	DESCRIPTION
7		**Audio gain**
	1	–6 dB
	0	0 dB
6		**De-emphasis time constant**
	1	50 μs
	0	75 μs
5		**De-emphasis**
	1	on
	0	off
4 to 0		**Tuner takeover point adjustment**
		see Table 13

Table 13 Tuner takeover point adjustment bits

BIT					TOP ADJUSTMENT (dB)
4	**3**	**2**	**1**	**0**	
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	0(1)
0	1	1	1	1	–1
0	1	1	1	0	–2
0	1	1	0	1	–3
0	1	1	0	0	–4
0	1	0	1	1	–5
0	1	0	1	0	–6
0	1	0	0	1	–7
0	1	0	0	0	–8
0	0	1	1	1	–9
0	0	1	1	0	–10
0	0	1	0	1	–11
0	0	1	0	0	–12
0	0	0	1	1	–13
0	0	0	1	0	–14
0	0	0	0	1	–15
0	0	0	0	0	–16

Note

1. 0 dB is equal to 17 mV (RMS).

9.2.4 DATA BYTE FOR DATA MODE

Table 14 Bit description of SAD register for data mode (SAD = 10)

BIT	VALUE	DESCRIPTION
7		**VIF-AGC output at pin OP2**
		dependent on bits 5 and 1; see Table 15
6		**L standard PLL gating HIGH**
	1	gating in case of 36% positive modulation
	0	gating in case of 0% positive modulation
5		**VIF, SIF and tuner minimum gain**
		dependent on bit 7; see Table 15
4 to 2		**Frequency selection**
		see Table 17
1 and 0		**Standard frequency sound intercarrier (sound 2nd IF)**
	00	f_{FM} = 4.5 MHz
	01	f_{FM} = 5.5 MHz
	10	f_{FM} = 6.0 MHz
	11	f_{FM} = 6.5 MHz (for positive modulation choose 6.5 MHz)

Table 15 Options in extended TV mode; bit 3 = 0 of SAD = 00 register

FUNCTION	BIT 7 = 0		BIT 7 = 1	
	BIT 5 = 0	BIT 5 = 1	BIT 5 = 0	BIT 5 = 1
Pin OP1	port function	port function	port function	VIF-AGC external input
Pin OP2	port function	port function	VIF-AGC output	port function
Gain	normal gain	minimum gain	normal gain	external gain

Table 16 Options in extended radio mode; bit 3 = 1 of SAD = 00 register

FUNCTION	BIT 7 = 0	BIT 7 = 1	
		BIT 4 = 0, BIT 3 = 0	BIT 4 = 1, BIT 3 = 1
Pin AFC	FM radio carrier related AFC	SIF-AGC radio output	FM-AGC radio output

Table 17 Frequency selection bits

BIT			DESCRIPTION	
4	**3**	**2**	**TV MODE** **BIT 3 = 0 OF REGISTER SAD = 00**	**RADIO MODE** **BIT 3 = 1 OF REGISTER SAD = 00**
0	0	0	f_{VIF} = 58.75 MHz; note 1	f_{RIF1} = 33.3 MHz, f_{VCO} = 44 MHz; f_{RIF2} = 10.7 MHz
0	0	1	f_{VIF} = 45.75 MHz	f_{RIF1} = 41.3 MHz, f_{VCO} = 52 MHz; f_{RIF2} = 10.7 MHz
0	1	0	f_{VIF} = 38.9 MHz	f_{RIF1} = 33.3 MHz, f_{VCO} = 44 MHz; f_{RIF2} = 10.7 MHz
0	1	1	f_{VIF} = 38.0 MHz	f_{RIF1} = 33.3 MHz, f_{VCO} = 44 MHz; f_{RIF2} = 10.7 MHz
1	0	0	f_{VIF} = 33.9 MHz	f_{RIF1} = 33.3 MHz, f_{VCO} = 44 MHz; f_{RIF2} = 10.7 MHz
1	0	1	f_{VIF} = 33.4 MHz	f_{RIF1} = 33.3 MHz, f_{VCO} = 44 MHz; f_{RIF2} = 10.7 MHz
1	1	0	f_{VIF} = 45.75 MHz plus FM external input via pin FMIN; note 2	f_{RIF1} = 41.3 MHz, f_{VCO} = 52 MHz; f_{RIF2} = 10.7 MHz
1	1	1	f_{VIF} = 38.9 MHz plus FM external input via pin FMIN; note 2	f_{RIF1} = 33.3 MHz, f_{VCO} = 44 MHz; f_{RIF2} = 10.7 MHz

Notes

1. Pin SIOMAD can be used for the selection of the different NTSC standards without I^2C-bus. With a resistor on pin SIOMAD, the f_{VIF} = 58.75 MHz and without a resistor on pin SIOMAD, the f_{VIF} = 45.75 MHz (NTSC-M).
2. Attention: video sound traps are locked on the FM VCO. The second VIF should be selected in accordance with the selected video standard.

Table 18 Data setting after power-on reset (default setting for MAD = 0)

REGISTER	MSB							LSB
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	0	0	0

Table 19 Data setting after power-on reset (default setting for MAD = 1)

REGISTER	MSB							LSB
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Switching mode	1	1	0	1	0	1	1	0
Adjust mode	0	0	1	1	0	0	0	0
Data mode	0	0	0	0	0	1	0	0

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	5.5	V
V_n	voltage on				
	pins VIF1, VIF2, SIF1, SIF2, OP1, OP2, V_P, and FMPLL		0	V_P	V
	pin TAGC		0	8.8	V
t_{sc}	short-circuit time to ground or V_P		–	10	s
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	ambient temperature		–20	+70	°C
V_{es}	electrostatic discharge voltage on all pins	note 1	–300	+300	V
		note 2	–3000	+3000	V

Notes

1. Machine model in accordance with SNW-FQ-302B: class B, discharging a 200 pF capacitor via a 0.75 µH series inductance.
2. Human body model in accordance with SNW-FQ-302A: class 2, discharging a 100 pF capacitor via a 1.5 kΩ series resistor.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	105	K/W

12 CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; see Table 21 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC/SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10% and for L is 3%; video signal in accordance with *"CCIR line 17 and line 330"* or *"NTC-7 Composite"*; measurements taken in test circuit of Fig.23; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin V_P)						
V_P	supply voltage	note 1	4.5	5.0	5.5	V
I_P	supply current		52	63	70	mA
P_{tot}	total power dissipation		–	305	385	mW
POWER-ON RESET						
$V_{P(start)}$	supply voltage for start of reset	decreasing supply voltage	2.5	3.0	3.5	V
$V_{P(stop)}$	supply voltage for end of reset	increasing supply voltage; I²C-bus transmission enable	–	–	4.4	V
τ_P	time constant (R × C) for network at pin V_P	for applications without I²C-bus	1.2	–	–	µs
VIF amplifier (pins VIF1 and VIF2)						
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	–1 dB video at output	–	60	100	µV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	+1 dB video at output	150	190	–	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)	note 2	–	–	440	mV
$\Delta V_{IF(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 5.5 MHz	–	0.7	–	dB
$G_{VIF(cr)}$	VIF gain control range		60	66	–	dB
$B_{VIF(-3dB)(ll)}$	lower limit –3 dB VIF bandwidth		–	15	–	MHz
$B_{VIF(-3dB)(ul)}$	upper limit –3 dB VIF bandwidth		–	80	–	MHz
$R_{i(dif)}$	differential input resistance	note 3	–	2	–	kΩ
$C_{i(dif)}$	differential input capacitance	note 3	–	3	–	pF
V_I	DC input voltage		–	1.93	–	V
FPLL and true synchronous video demodulator; note 4						
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	f = $2f_{PC}$	120	140	–	MHz
f_{VIF}	vision carrier operating frequencies	see Table 17	–	33.4	–	MHz
			–	33.9	–	MHz
			–	38.0	–	MHz
			–	38.9	–	MHz
			–	45.75	–	MHz
			–	58.75	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Fig.9	–	±2.3	–	MHz
t_{acq}	acquisition time	BL = 70 kHz; note 5	–	–	30	ms
$V_{i(lock)(rms)}$	input voltage sensitivity for PLL to be locked (RMS value)	measured on pins VIF1 and VIF2; maximum IF gain	–	30	70	μV
$T_{cy(DAH)}$	cycle time of digital acquisition help		–	64	–	μs
$K_{O(VIF)}$	VIF VCO steepness	definition: $\Delta f_{VIF}/\Delta V_{VPLL}$	–	20	–	MHz/V
$K_{D(VIF)}$	VIF phase detector steepness	definition: $\Delta I_{VPLL}/\Delta\varphi_{VIF}$	–	23	–	μA/rad
Video output 2 V (pin CVBS)						
NORMAL MODE (SOUND CARRIER TRAP ACTIVE) AND SOUND CARRIER ON						
$V_{o(p-p)}$	video output voltage (peak-to-peak value)	see Fig.3	1.7	2.0	2.3	V
ΔV_o	video output voltage difference	difference between L and B/G standard	–12	–	+12	%
V/S	ratio between video (black-to-white) and sync level		1.90	2.33	3.00	
V_{sync}	sync voltage level		1.0	1.2	1.4	V
$V_{clip(u)}$	upper video clipping voltage level		$V_P - 1.1$	$V_P - 1$	–	V
$V_{clip(l)}$	lower video clipping voltage level		–	0.7	0.9	V
R_o	output resistance	note 3	–	–	30	Ω
$I_{bias(int)}$	internal DC bias current for emitter-follower		1.5	2.0	–	mA
$I_{o(sink)(max)}$	maximum AC and DC output sink current		1	–	–	mA
$I_{o(source)(max)}$	maximum AC and DC output source current		3.9	–	–	mA
$\Delta V_{o(CVBS)}$	deviation of CVBS output voltage	50 dB gain control	–	–	0.5	dB
		30 dB gain control	–	–	0.1	dB
$\Delta V_{o(bl)}$	black level tilt	negative modulation	–	–	1	%
$\Delta V_{o(bl)(v)}$	vertical black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only	–	–	3	%
G_{dif}	differential gain	*“CCIR 330”*; note 6				
		B/G standard	–	–	5	%
		L standard	–	–	7	%
φ_{dif}	differential phase	*“CCIR 330”*	–	2	4	deg
$S/N_{W(video)}$	weighted signal-to-noise ratio	weighted in accordance with *“CCIR 567”*; see Fig.11; note 7	56	59	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$S/N_{UW(video)}$	unweighted signal-to-noise ratio	note 7	47	51	–	dB
$\alpha_{IM(blue)}$	intermodulation attenuation at ‘blue’	see Fig.12; note 8				
		f = 1.1 MHz	58	64	–	dB
		f = 3.3 MHz	58	64	–	dB
$\alpha_{IM(yellow)}$	intermodulation attenuation at ‘yellow’	see Fig.12; note 8				
		f = 1.1 MHz	60	66	–	dB
		f = 3.3 MHz	59	65	–	dB
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics	–	2	5	mV
$\Delta f_{unw(p-p)}$	robustness for unwanted frequency deviation of picture carrier (peak-to-peak value)	3% residual carrier; 50% serration pulses; L standard; note 3	–	–	12	kHz
$\Delta\varphi$	robustness for modulator imbalance	0% residual carrier; 50% serration pulses; L standard; L-gating = 0%; note 3	–	–	3	%
α_H	suppression of video signal harmonics	C_L < 20 pF; R_L > 1 kΩ; AC load; note 9a	35	40	–	dB
α_{spur}	suppression of spurious elements	note 9b	40	–	–	dB
$PSRR_{CVBS}$	power supply ripple rejection at pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Fig.4	20	25	–	dB
M/N STANDARD INCLUSIVE KOREA; see Fig.13						
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz; note 10	3.95	4.05	–	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz	30	36	–	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 4.5 MHz	21	27	–	dB
α_{SC2}	attenuation at second sound carrier	f = 4.724 MHz	21	27	–	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 4.724 MHz	15	21	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	f = 3.58 MHz; see Fig.14	110	180	250	ns
B/G STANDARD; see Fig.15						
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 5.5 MHz; note 10	4.90	5.00	–	MHz
α_{SC1}	attenuation at first sound carrier	f = 5.5 MHz	30	36	–	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 5.5 MHz	24	30	–	dB
α_{SC2}	attenuation at second sound carrier	f = 5.742 MHz	21	27	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 5.742 MHz	15	21	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	f = 4.43 MHz; see Fig.16	110	180	250	ns
I STANDARD; see Fig.17						
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 6.0 MHz; note 10	5.40	5.50	–	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.0 MHz	26	32	–	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 6.0 MHz	20	26	–	dB
α_{SC2}	attenuation at second sound carrier	f = 6.55 MHz	12	18	–	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 6.55 MHz	10	15	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	f = 4.43 MHz	–	90	160	ns
D/K STANDARD; see Fig.18						
$B_{v(-3dB)(trap)}$	–3 dB video bandwidth including sound carrier trap	f_{trap} = 6.5 MHz; note 10	5.50	5.95	–	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.5 MHz	26	32	–	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 6.5 MHz	20	26	–	dB
α_{SC2}	attenuation at second sound carrier	f = 6.742 MHz	18	24	–	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 6.742 MHz	13	18	–	dB
$t_{d(g)(cc)}$	group delay at colour carrier frequency	f = 4.28 MHz	–	60	130	ns
Video output 1.1 V (pin CVBS)						
TRAP BYPASS MODE AND SOUND CARRIER OFF; note 11						
$V_{o(p-p)}$	video output voltage (peak-to-peak value)	see Fig.3	0.95	1.10	1.25	V
V_{sync}	sync voltage level		1.35	1.5	1.6	V
$V_{clip(u)}$	upper video clipping voltage level		3.5	3.6	–	V
$V_{clip(l)}$	lower video clipping voltage level		–	0.9	1.0	V
$B_{v(-1dB)}$	–1 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	5	6	–	MHz
$B_{v(-3dB)}$	–3 dB video bandwidth	C_L < 20 pF; R_L > 1 kΩ; AC load	7	8	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_W	weighted signal-to-noise ratio	weighted in accordance with *“CCIR 567”*; see Fig.11; note 7	56	59	–	dB
S/N_{UW}	unweighted signal-to-noise ratio	note 7	48	52	–	dB
VIF-AGC (pin VAGC); note 12						
$I_{ch(max)}$	maximum charge current	L standard	–	100	–	μA
$I_{ch(add)}$	additional charge current	L standard: in the event of missing VITS pulses and no white video content	–	100	–	nA
I_{dch}	discharge current	L standard; normal mode	–	35	–	nA
		L standard; fast mode	–	1.8	–	μA
$t_{resp(inc)}$	AGC response time to an increasing VIF step	negative modulation; 20 dB; note 13	–	4	–	ms
		positive modulation; 20 dB; note 13	–	2.6	–	ms
$t_{resp(dec)}$	AGC response time to a decreasing VIF step	negative modulation; 20 dB; note 13	–	3	–	ms
		positive modulation; 20 dB; note 13	–	890	–	ms
		L standard; fast mode	–	2.6	–	ms/dB
		L standard; normal mode; note 13	–	143	–	ms/dB
$\Delta V_{i(VIF)}$	VIF amplitude step for activating AGC fast mode	L standard	–2	–6	–10	dB
V_{VAGV}	gain control voltage range		0.8	–	3.5	V
CR_{stps}	control steepness	definition: $\Delta G_{VIF}/\Delta V_{VAGC}$; V_{VAGC} = 2 to 3 V	–	–80	–	dB/V
$V_{th(VIF)}$	threshold voltage for high level VIF input	see Tables 5 and 6	120	200	320	μV
Tuner AGC (pin TAGC); see Figs 5 to 8						
$V_{i(VIF)(start1)(rms)}$	VIF input signal voltage for minimum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	I_{TAGC} = 120 μA; R_{TOP} = 22 kΩ or no R_{TOP} and –15 dB via I^2C-bus (see Table 13)	–	2	5	mV
$V_{i(VIF)(start2)(rms)}$	VIF input signal voltage for maximum starting point of tuner takeover at pins VIF1 and VIF2 (RMS value)	I_{TAGC} = 120 μA; R_{TOP} = 0 Ω or no R_{TOP} and +15 dB via I^2C-bus (see Table 13)	45	90	–	mV
$V_{i(SIF)(start1)(rms)}$	SIF input signal voltage for minimum starting point of tuner takeover at pins SIF1 and SIF2 (RMS value)	I_{TAGC} = 120 μA; R_{TOP} = 22 kΩ or no R_{TOP} and –15 dB via I^2C-bus (see Table 13)	–	1	2.5	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(SIF)(start2)(rms)}$	SIF input signal voltage for maximum starting point of tuner takeover at pins SIF1 and SIF2 (RMS value)	I_{TAGC} = 120 μA; R_{TOP} = 0 Ω or no R_{TOP} and +15 dB via I^2C-bus (see Table 13)	22.5	45	–	mV
QV_{TOP}	tuner takeover point accuracy	I_{TAGC} = 120 μA; R_{TOP} = 10 kΩ or no R_{TOP} and 0 dB via I^2C-bus (see Table 13)	7	17	43	mV
$\Delta QV_{TOP}/\Delta T$	takeover point variation with temperature	I_{TAGC} = 120 μA	–	0.03	0.07	dB/K
V_o	permissible output voltage	from external source	–	–	8.8	V
V_{sat}	saturation voltage	I_{TAGC} = 450 μA	–	–	0.5	V
I_{sink}	sink current	no tuner gain reduction; V_{TAGC} = 8.8 V	–	–	0.75	μA
		maximum tuner gain reduction; V_{TAGC} = 1 V	450	600	750	μA
ΔG_{IF}	IF slip by automatic gain control	tuner gain current from 20% to 80%	3	5	8	dB
AFC circuit and AGC monitor options (pin AFC); see Figs 9 and 10; notes 14 and 15						
$V_{sat(ul)}$	upper limit saturation voltage		V_P – 0.6	V_P – 0.3	–	V
$V_{sat(ll)}$	lower limit saturation voltage		–	0.3	0.6	V
$I_{o(source)}$	output source current		160	200	240	μA
$I_{o(sink)}$	output sink current		160	200	240	μA
TV MODE						
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{VIF}$	0.85	1.05	1.25	μA/kHz
$Qf_{VIF(a)}$	analog accuracy of AFC circuit	I_{AFC} = 0; f_{REF} = 4 MHz	–20	–	+20	kHz
$Qf_{VIF(d)}$	digital accuracy of AFC circuit via I^2C-bus	I_{AFC} = 0; f_{REF} = 4 MHz; 1 digit = 25 kHz	–20 – 1 digit	–	+20 + 1 digit	kHz
RADIO MODE						
AFC_{stps}	AFC control steepness	definition: $\Delta I_{AFC}/\Delta f_{RIF}$	0.85	1.05	1.25	μA/kHz
$Qf_{RIF(a)}$	analog accuracy of AFC circuit	I_{AFC} = 0; f_{REF} = 4 MHz	–10	–	+10	kHz
$Qf_{RIF(d)}$	digital accuracy of AFC circuit via I^2C-bus	I_{AFC} = 0; f_{REF} = 4 MHz; 1 digit = 25 kHz	–10 – 1 digit	–	+10 + 1 digit	kHz
$I_{o(source)}$	SIF or FM-AGC monitor source current	see Table 16	–	–	600	mA
$I_{o(sink)}$	SIF or FM-AGC monitor sink current	see Table 16	–	–	270	mA
SIF amplifier (pins SIF1 and SIF2)						
$V_{i(SIF)(rms)}$	SIF input voltage sensitivity (RMS value)	FM mode; –3 dB at intercarrier output pin SIOMAD	–	30	70	μV
		AM mode; –3 dB at AF output pin AUD	–	70	100	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	FM mode; 1 dB at intercarrier output pin SIOMAD	50	70	–	mV
		AM mode; 1 dB at AF output pin AUD	80	140	–	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)	note 2	–	–	320	mV
$G_{SIF(cr)}$	SIF gain control range	FM and AM mode	60	66	–	dB
$B_{SIF(-3dB)(ll)}$	lower limit –3 dB SIF bandwidth		–	15	–	MHz
$B_{SIF(-3dB)(ul)}$	upper limit –3 dB SIF bandwidth		–	80	–	MHz
$R_{i(dif)}$	differential input resistance	note 3	–	2	–	kΩ
$C_{i(dif)}$	differential input capacitance	note 3	–	3	–	pF
V_I	DC input voltage		–	1.93	–	V
SIF-AGC detector						
t_{resp}	AGC response time to an increasing or decreasing SIF step of 20 dB	FM or AM fast steps				
		increasing	–	8	–	ms
		decreasing	–	25	–	ms
		AM slow steps				
		increasing	–	80	–	ms
		decreasing	–	250	–	ms
Single reference QSS intercarrier mixer (pin SIOMAD)						
$V_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC_1; SC_2 off	90	140	180	mV
		L standard; without modulation	90	140	180	mV
		intercarrier mode; PC/SC_1 = 20 dB; SC_2 off; note 16	–	75	–	mV
$B_{intc(-3dB)(ul)}$	upper limit –3 dB intercarrier bandwidth		12	15	–	MHz
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics				
		QSS mode	–	2	5	mV
		intercarrier mode	–	2	5	mV
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics				
		QSS mode	–	2	5	mV
		intercarrier mode	–	5	20	mV
α_H	suppression of video signal harmonics	intercarrier mode; f_{video} = 5 MHz	35	40	–	dB
R_o	output resistance	note 3	–	–	30	Ω
V_O	DC output voltage		–	2	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{bias(int)}$	internal DC bias current for emitter follower		0.90	1.15	–	mA
$I_{o(sink)(max)}$	maximum AC output sink current		0.6	0.8	–	mA
$I_{o(source)(max)}$	maximum AC output source current		0.6	0.8	–	mA
$I_{o(source)}$	DC output source current	MAD2 activated; note 17	0.75	0.93	1.20	mA
FM-PLL demodulator output; notes 15 and 18 to 22						
SOUND INTERCARRIER OUTPUT (PIN SIOMAD)						
$V_{FM(rms)}$	IF intercarrier level for gain controlled operation of FM-PLL (RMS value)	corresponding PC/SC ratio at input pins VIF1 and VIF2 is 7 to 47 dB	3.2	–	320	mV
$V_{FM(lock)(rms)}$	IF intercarrier level for lock-in of PLL (RMS value)		–	–	2	mV
$V_{FM(det)(rms)}$	IF intercarrier level for FM carrier detect (RMS value)	see Table 6	–	–	2.3	mV
f_{FM}	sound intercarrier operating FM frequencies	see Tables 11 and 14	–	4.5	–	MHz
			–	5.5	–	MHz
			–	6.0	–	MHz
			–	6.5	–	MHz
			–	10.7	–	MHz
IF INTERCARRIER INPUT (PIN FMIN)						
$V_{i(FM)(rms)}$	IF intercarrier input voltage for gain controlled operation of FM-PLL (RMS value)	radio mode and FM external mode; see Table 16	1	–	100	mV
$V_{FM(lock)(rms)}$	IF intercarrier level for lock-in of PLL (RMS value)		–	–	0.7	mV
$V_{FM(det)(rms)}$	IF intercarrier level for FM carrier detect (RMS value)	see Table 6	–	–	0.8	mV
AUDIO OUTPUT (PIN AUD)						
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	25 kHz FM deviation; 75 µs de-emphasis	400	500	600	mV
		27 kHz FM deviation; 50 µs de-emphasis	430	540	650	mV
		radio mode; 22.5 kHz modulation	200	250	300	mV
$V_{o(AF)(cl)(rms)}$	AF output clipping level (RMS value)	THD < 1.5%	1.3	1.4	–	V
$\Delta V_{o(AF)}/\Delta T$	AF output voltage variation with temperature		–	3×10^{-3}	7×10^{-3}	dB/K

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	75 µs de-emphasis; FM deviation: for TV mode 25 kHz and for radio mode 22.5 kHz	–	0.15	0.50	%
Δf_{AF}	frequency deviation	THD < 1.5%; note 19	–	–	±55	kHz
		–6 dB AF output via I^2C-bus; note 19	–	–	±110	kHz
$B_{AF(-3dB)}$	–3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter of Fig.23	80	100	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	FM-PLL only; 27 kHz FM deviation; 50 µs de-emphasis	52	56	–	dB
		black picture; see Fig.19	50	56	–	dB
$S/N_{UW(AF)}$	unweighted signal-to-noise ratio	radio mode; 22.5 kHz modulation	–	58	–	dB
$\Delta V_{r(SC)(rms)}$	residual sound carrier (RMS value)	fundamental wave and harmonics; without de-emphasis	–	–	2	mV
$\alpha_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54%	40	46	–	dB
$PSRR_{FM}$	power supply ripple rejection	f_{ripple} = 70 Hz; see Fig.4	14	20	–	dB
FM-PLL FILTER (PIN FMPLL)						
V_{loop}	DC loop voltage		1.5	–	3.3	V
$I_{o(source)(PD)(max)}$	maximum phase detector output source current		–	60	–	µA
$I_{o(sink)(PD)(max)}$	maximum phase detector output sink current		–	60	–	µA
$I_{o(source)(DAH)}$	output source current of digital acquisition help		–	55	–	µA
$I_{o(sink)(DAH)}$	output sink current of digital acquisition help		–	55	–	µA
$t_{W(DAH)}$	pulse width of digital acquisition help current		–	16	–	µs
$T_{cy(DAH)}$	cycle time of digital acquisition help		–	64	–	µs
$K_{O(FM)}$	VCO steepness	definition: $\Delta f_{FM}/\Delta V_{FMPLL}$	–	3.3	–	MHz/V
$K_{D(FM)}$	phase detector steepness	definition: $\Delta I_{FMPLL}/\Delta\varphi_{FM}$	–	4	–	µA/rad

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Audio amplifier						
DE-EMPHASIS NETWORK (PIN DEEM)						
R_o	output resistance	50 µs de-emphasis; see Table 12	4.4	5.0	5.6	kΩ
		75 µs de-emphasis; see Table 12	6.6	7.5	8.4	kΩ
$V_{AF(rms)}$	audio signal (RMS value)	f_{AF} = 400 Hz; V_{AUD} = 500 mV	–	170	–	mV
V_O	DC output voltage		–	2.37	–	V
AF DECOUPLING (PIN AFD)						
V_{dec}	DC decoupling voltage	dependent on f_{FM} intercarrier frequency	1.5	–	3.3	V
I_L	leakage current	$\Delta V_{O(AUD)}$ < ±50 mV	–	–	±25	nA
$I_{ch(max)}$	maximum charge current		1.15	1.50	1.85	µA
$I_{dch(max)}$	maximum discharge current		1.15	1.50	1.85	µA
AUDIO OUTPUT (PIN AUD)						
R_o	output resistance	note 3	–	–	300	Ω
$V_{O(AUD)}$	DC output voltage		–	2.37	–	V
R_L	load resistance	AC-coupled	10	–	–	kΩ
$R_{L(DC)}$	DC load resistance		100	–	–	kΩ
C_L	load capacitance		–	–	1.5	nF
$B_{AF(-3dB)(ul)}$	upper limit –3 dB AF bandwidth of audio amplifier		150	–	–	kHz
$B_{AF(-3dB)(ll)}$	lower limit –3 dB AF bandwidth of audio amplifier	note 20	–	–	20	Hz
α_{mute}	mute attenuation of AF signal	via I^2C-bus	70	75	–	dB
ΔV_{jump}	DC jump voltage for switching AF output to mute state or vice versa	activated by digital acquisition help or via I^2C-bus mute	–	±50	±150	mV
FM operation; notes 21 and 23						
INTERCARRIER AF PERFORMANCE; note 24						
S/N_W	weighted signal-to-noise ratio	PC/SC ratio is 21 to 27 dB at pins VIF1 and VIF2				
		black picture	50	56	–	dB
		white picture	45	51	–	dB
		6 kHz sine wave (black-to-white modulation)	40	46	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	35	40	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SINGLE REFERENCE QSS AF PERFORMANCE; notes 25 and 26						
$S/N_{W(SC1)}$	weighted signal-to-noise ratio for SC_1	PC/SC_1 ratio at pins VIF1 and VIF2; 27 kHz (54% FM deviation); *“CCIR 468”*	40	–	–	dB
		black picture	53	58	–	dB
		white picture	50	53	–	dB
		6 kHz sine wave (black-to-white modulation)	44	48	–	dB
		250 kHz square wave (black-to-white modulation)	40	45	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	45	51	–	dB
		sound carrier subharmonics; f = 2.87 MHz ±3 kHz	46	52	–	dB
$S/N_{W(SC2)}$	weighted signal-to-noise ratio for SC_2	PC/SC_2 ratio at pins VIF1 and VIF2; 27 kHz (54% FM deviation); *“CCIR 468”*	40	–	–	dB
		black picture	48	55	–	dB
		white picture	46	51	–	dB
		6 kHz sine wave (black-to-white modulation)	42	46	–	dB
		250 kHz square wave (black-to-white modulation)	29	34	–	dB
		sound carrier subharmonics; f = 2.75 MHz ±3 kHz	44	50	–	dB
		sound carrier subharmonics; f = 2.87 MHz ±3 kHz	45	51	–	dB
AM operation						
L STANDARD (PIN AUD); see Figs 20 and 21; note 27						
$V_{o(AF)(rms)}$	AF output voltage (RMS value)	54% modulation	400	500	600	mV
THD	total harmonic distortion	54% modulation	–	0.5	1.0	%
$B_{AF(-3dB)}$	–3 dB AF bandwidth		100	125	–	kHz
$S/N_{W(AF)}$	weighted signal-to-noise ratio of audio signal	in accordance with *“CCIR 468”*	45	50	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{O(AUD)}$	DC potential voltage		–	2.37	–	V
$PSRR_{AM}$	power supply ripple rejection	see Fig.4	20	26	–	dB
Reference frequency input (pin REF)						
V_I	DC input voltage		2.3	2.6	2.9	V
R_i	input resistance	note 3	–	5	–	kΩ
R_{xtal}	resonance resistance of crystal	operation as crystal oscillator	–	–	200	Ω
C_x	pull-up/down capacitance	note 28	–	–	–	pF
f_{ref}	reference signal frequency	note 29	–	4	–	MHz
Δf_{ref}	tolerance of reference signal frequency	note 15	–	–	±0.1	%
$V_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal	80	–	400	mV
$R_{o(ref)}$	output resistance of reference signal source		–	–	4.7	kΩ
C_K	decoupling capacitance to external reference signal source	operation as input terminal	22	100	–	pF
I^2C-bus transceiver (pins SDA and SCL); notes 30 and 31						
f_{SCL}	SCL clock frequency		0	–	400	kHz
V_{IH}	HIGH-level input voltage		3	–	V_{CC}	V
V_{IL}	LOW-level input voltage		–0.3	–	+1.5	V
I_{IH}	HIGH-level input current		–10	–	+10	μA
I_{IL}	LOW-level input current		–10	–	+10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.4	V
$I_{o(sink)}$	output sink current	V_P = 0 V	–	–	10	μA
$I_{o(source)}$	output source current	V_P = 0 V	–	–	10	μA
Output ports (pins OP1 and OP2); note 32						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA (sink current)	–	–	0.4	V
V_{OH}	HIGH-level output voltage		–	–	6	V
$I_{o(sink)}$	output sink current		–	–	2	mA
$I_{o(sink/source)(max)}$	maximum output sink or source current	pin OP2 functions as VIF-AGC output	–	–	10	μA

Notes

1. Values of video and sound parameters can be decreased at V_P = 4.5 V.
2. Level headroom for input level jumps during gain control setting.
3. This parameter is not tested during the production and is only given as application information for designing the receiver circuit.

4. Loop bandwidth BL = 70 kHz (damping factor d = 1.9; calculated with sync level within gain control range). Calculation of the VIF-PLL filter can be done by use of the following formula:

$$BL_{-3dB} = \frac{1}{2\pi} K_O K_D R \text{ , valid for } d \geq 1.2$$

$$d = \frac{1}{2} R \sqrt{K_O K_D C} \text{ ,}$$

where:

K_O is the VCO steepness $\left(\frac{rad}{V}\right)$ or $\left(2\pi\frac{Hz}{V}\right)$; K_D is the phase detector steepness $\left(\frac{\mu A}{rad}\right)$;

R is the loop resistor; C is the loop capacitor; BL_{-3dB} is the loop bandwidth for –3 dB; d is the damping factor.

5. $V_{i(VIF)}$ = 10 mV (RMS); Δf = 1 MHz (VCO frequency offset related to picture carrier frequency); white picture video modulation.
6. Condition: luminance range (5 steps) from 0% to 100%.
7. S/N is the ratio of black-to-white amplitude to the black level noise voltage (RMS value on pin CVBS). B = 5 MHz (B/G, I and D/K standard). Noise analyzer setting: 200 kHz high-pass and SC-trap switched on.
8. The intermodulation figures are defined for:

   a) f = 1.1 MHz (referenced to black and white signal) as $\alpha_{IM} = 20 \log\left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 1.1 \text{ MHz}}\right) + 3.6 \text{ dB}$

   b) f = 3.3 MHz (referenced to colour carrier) as $\alpha_{IM} = 20 \log\left(\frac{V_0 \text{ at } 4.4 \text{ MHz}}{V_0 \text{ at } 3.3 \text{ MHz}}\right)$

9. Measurements taken with SAW filter M1963M (sound shelf: 20 dB); loop bandwidth BL = 70 kHz.

   a) Modulation Vestigial Side-Band (VSB); sound carrier off; f_{video} > 0.5 MHz.

   b) Sound carrier on; f_{video} = 10 kHz to 10 MHz.

10. AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figs 13 to 18; $|H(s)|$ is the absolute value of transfer function).
11. The sound carrier trap can be bypassed by switching the I²C-bus. In this way the full composite video spectrum appears at pin CVBS. The amplitude is 1.1 V (p-p).
12. If selected by the I²C-bus, the VIF-AGC voltage can be monitored at pin OP2, and pin OP1 can be used as input. In this case, both pins cannot be used for the normal port function.
13. The response time is valid for a VIF input level range from 200 μV to 70 mV.
14. To match the AFC output signal to different tuning systems a current source output is provided. The test circuit is given in Fig.9. The AFC slope (voltage per frequency) can be changed by resistors R1 and R2.
15. The tolerance of the reference frequency determines the accuracy of the VIF-AFC, FM demodulator centre frequency and maximum FM deviation.

16. The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with 1.1 V (p-p) as a reference:

$$V_{o(intc)} = 1.1\ \text{V (p-p)} \times \frac{1}{2\sqrt{2}} \times 10^{\frac{\frac{V_{i(SC)}}{V_{i(PC)}}(\text{dB}) + 6\ \text{dB} \pm 3\ \text{dB}}{20}}\ \text{(RMS)}$$

where:

$\frac{1}{2\sqrt{2}}$ is the correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}(\text{dB})$ is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output $V_{o(intc)(rms)}$.

17. For normal operation (with the I²C-bus) no DC load at pin SIOMAD is allowed. The second module address (MAD2) will be activated by the application of a 2.2 kΩ resistor between pin SIOMAD and ground. If this MAD2 is activated, also the power-on set-up state activates a VIF frequency of 58.75 MHz.
18. SIF input level is 10 mV (RMS); VIF input level is 10 mV (RMS) unmodulated.
19. Measured with an FM deviation of 25 kHz and the typical AF output voltage of 500 mV (RMS). The AF output signal can be attenuated by 6 dB to 250 mV (RMS) via the I²C-bus. For handling a frequency deviation of more than 55 kHz, the AF output signal has to be reduced in order to avoid clipping (THD < 1.5%).
20. The lower limit of the audio bandwidth depends on the value of the capacitor at pin AFD. A value of C_{AF} = 470 nF leads to $f_{AF(-3dB)} \approx 20$ Hz and C_{AF} = 220 nF leads to $f_{AF(-3dB)} \approx 40$ Hz.
21. For all S/N measurements the used VIF modulator has to meet the following specifications:
    a) Incidental phase modulation for black-to-white jump less than 0.5 degrees.
    b) QSS AF performance, measured with the television demodulator AMF2 (audio output, weighted S/N ratio) better than 60 dB (at deviation 27 kHz) for 6 kHz sine wave black-to-white video modulation.
    c) Picture-to-sound carrier ratio PC/SC_1 = 13 dB (transmitter).
22. Calculation of the loop filter can be done approximately by use of the following formulae:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{K_O K_D}{C_P}}$$

$$\vartheta = \frac{1}{2R\sqrt{K_O K_D C_P}}$$

$$BL_{-3dB} = f_o(1.55 - \vartheta^2)$$

The formulae are only valid under the following conditions:
$\vartheta \leq 1$ and $C_S > 5C_P$
where:

K_O is the VCO steepness $\left(\frac{\text{rad}}{\text{V}}\right)$ or $\left(2\pi\frac{\text{Hz}}{\text{V}}\right)$; K_D is the phase detector steepness $\left(\frac{\mu\text{A}}{\text{rad}}\right)$;

R is the loop resistor; C_S is the series capacitor; C_P is the parallel capacitor; f_o is the natural frequency of PLL; BL_{-3dB} is the loop bandwidth for –3 dB; ϑ is the damping factor. For examples, see Table 20.

23. The PC/SC ratio is calculated as the addition of TV transmitter PC/SC_1 ratio and SAW filter PC/SC_1 ratio. This PC/SC ratio is necessary to achieve the S/N_W values as noted. A different PC/SC ratio will change these values.
24. Measurements taken with SAW filter G1984 (Siemens) for vision and sound IF (sound shelf: 14 dB).
    Picture-to-sound carrier ratio of transmitter PC/SC = 13 dB. Input level on pins VIF1 and VIF2 of
    $V_{i(SIF)}$ = 10 mV (RMS) sync level, 27 kHz FM deviation for sound carrier, f_{AF} = 400 Hz. Measurements in accordance with *“CCIR 468”*. De-emphasis is 50 µs.

25. The QSS signal output on pin SIOMAD is analysed by a test demodulator TDA9820. The S/N ratio of this device is more than 60 dB, related to a deviation of ±27 kHz, in accordance with *“CCIR 468”*.
26. Measurements taken with SAW filter K3953 for vision IF (suppressed sound carrier) and K9453 for sound IF (suppressed picture carrier). Input level $V_{i(SIF)}$ = 10 mV (RMS), 27 kHz (54% FM deviation).
27. Measurements taken with SAW filter K9453 (Siemens) for AM sound IF (suppressed picture carrier).
28. The value of C_x determines the accuracy of the resonance frequency of the crystal. It depends on the used type of crystal.
29. Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.
30. The SDA and SCL lines will not be pulled down if V_{CC} is switched off.
31. The AC characteristics are in accordance with the I^2C-bus specification for fast mode (maximum clock frequency is 400 kHz). Information about the I^2C-bus can be found in the brochure *“The I^2C-bus and how to use it”* (order number 9398 393 40011).
32. Port P1 and port P2 are open-collector outputs.

Table 20 Examples to note 22 (FM-PLL filter)

BL_{-3dB} (kHz)	C_S (nF)	C_P (pF)	R (kΩ)	ϑ
100	10	390	5.6	0.5
160	10	150	8.2	0.5

Table 21 Input frequencies and carrier ratios

DESCRIPTION	SYMBOL	B/G STANDARD	M/N STANDARD	L STANDARD	L ACCENT STANDARD	UNIT
VIF carrier	f_{PC}	38.9	45.75 or 58.75	38.9	33.9	MHz
SIF carrier	f_{SC1}	33.4	41.25 or 54.25	32.4	40.4	MHz
	f_{SC2}	33.158	–	–	–	MHz
Picture-to-sound carrier ratio	SC_1	13	7	10	10	dB
	SC_2	20	–	–	–	dB

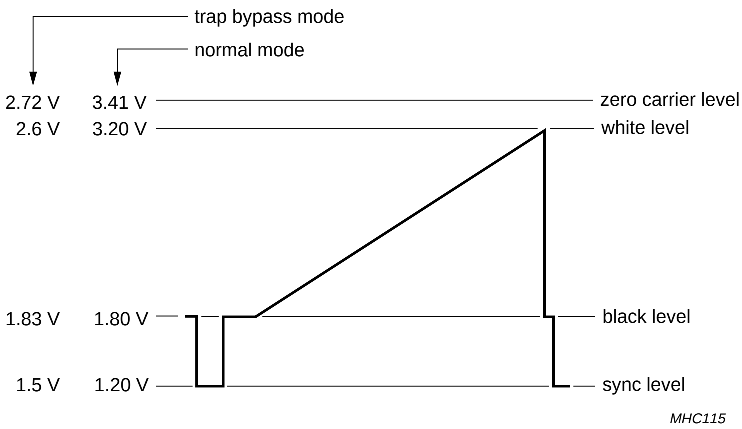


Fig.3 Typical video signal levels on output pin CVBS (sound carrier off).

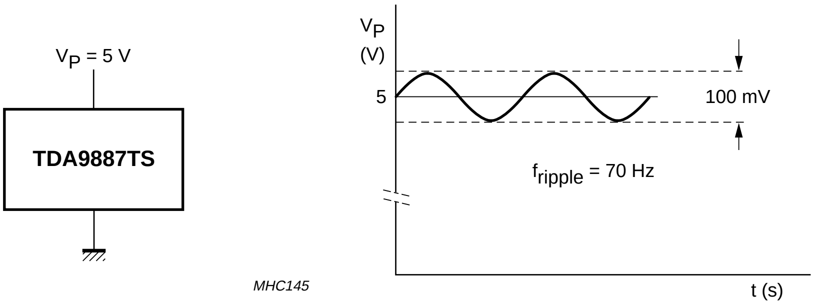
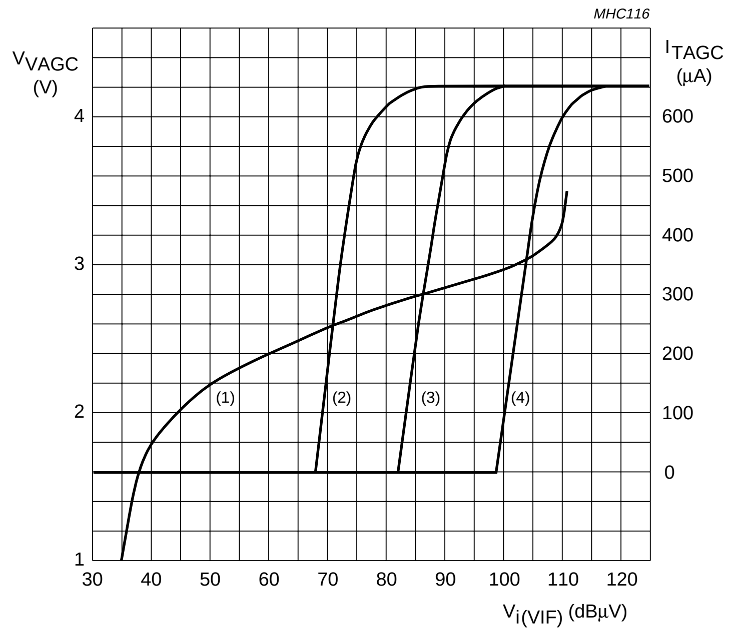


Fig.4 Ripple rejection condition.



(1) V_{VAGC} is VIF-AGC voltage and can only be measured at pin OP2 controlled by the I^2C-bus (see Table 15).
(2) I_{TAGC} is tuner current in TV mode with R_{TOP} = 22 kΩ or setting via I^2C-bus at −15 dB.
(3) I_{TAGC} is tuner current in TV mode with R_{TOP} = 10 kΩ or setting via I^2C-bus at 0 dB.
(4) I_{TAGC} is tuner current in TV mode with R_{TOP} = 0 kΩ or setting via I^2C-bus at +15 dB.

Fig.5 Typical VIF and tuner AGC characteristic.

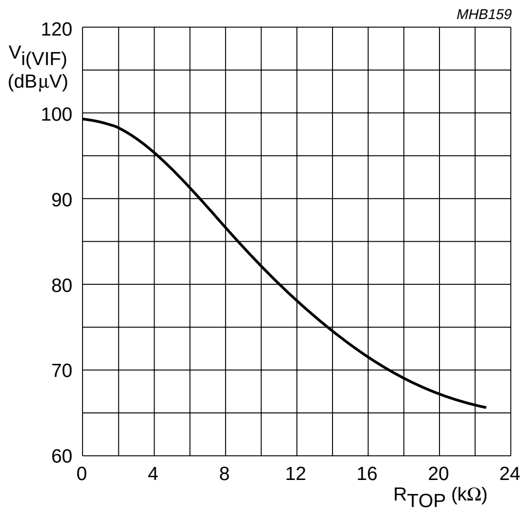


Fig.6 Typical tuner takeover point as a function of resistor R_{TOP}.

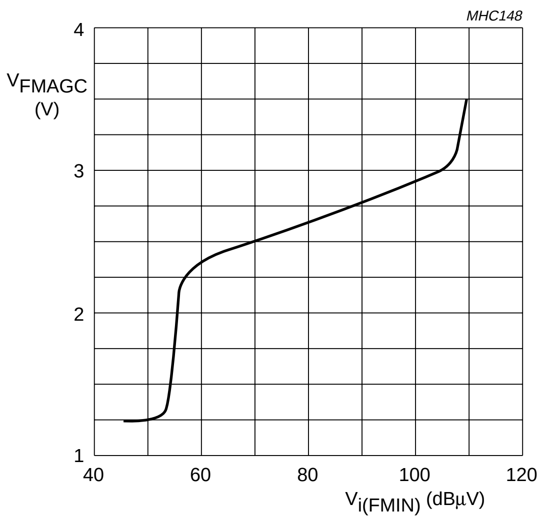
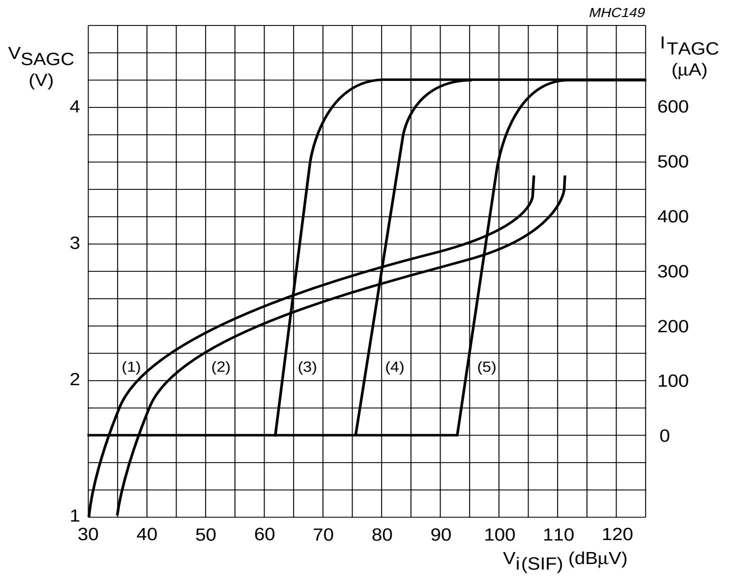


Fig.7 Typical FM-AGC characteristic.



(1) V_{SAGC} is SIF-AGC voltage in FM mode.
(2) V_{SAGC} is SIF-AGC voltage in AM mode.
(3) I_{TAGC} is tuner current in TV mode with R_{TOP} = 22 kΩ or setting via I²C-bus at –15 dB.
(4) I_{TAGC} is tuner current in TV mode with R_{TOP} = 10 kΩ or setting via I²C-bus at 0 dB.
(5) I_{TAGC} is tuner current in TV mode with R_{TOP} = 0 kΩ or setting via I²C-bus at +15 dB.

Fig.8 Typical SIF and tuner AGC characteristic.

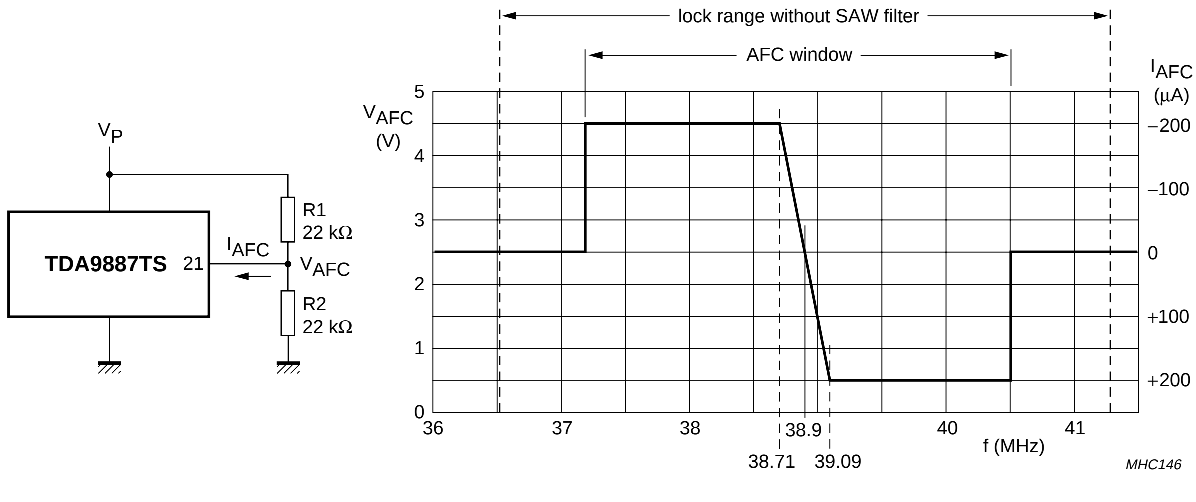


Fig.9 Typical analog AFC characteristic for VIF.

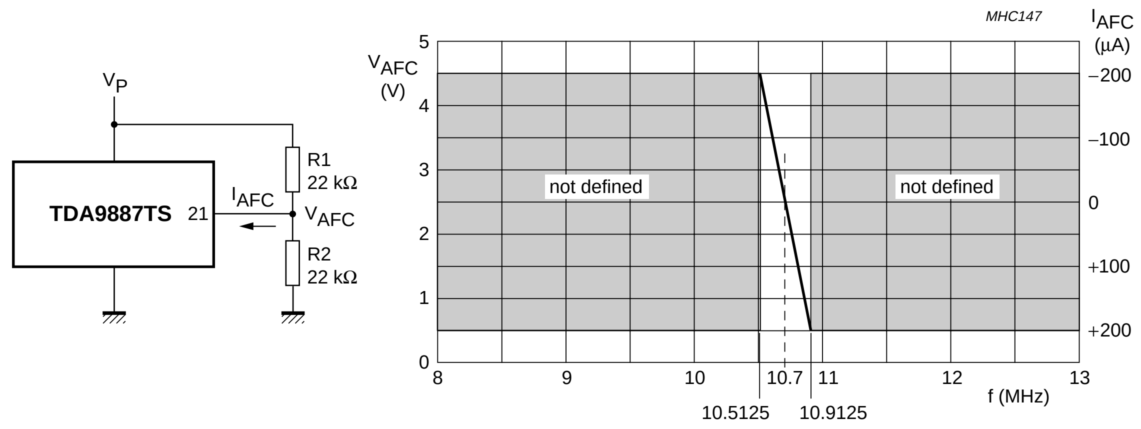


Fig.10 Typical analog AFC characteristic for RIF.

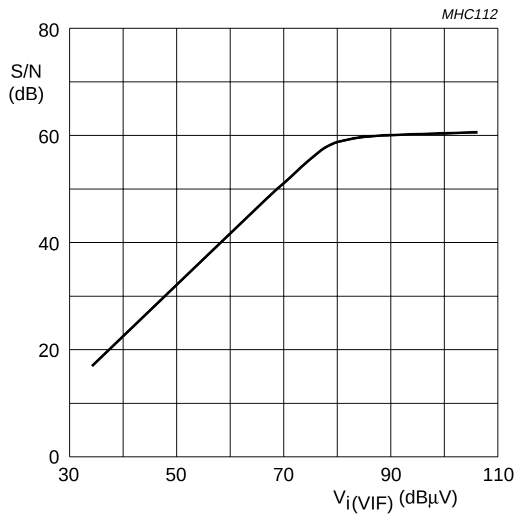
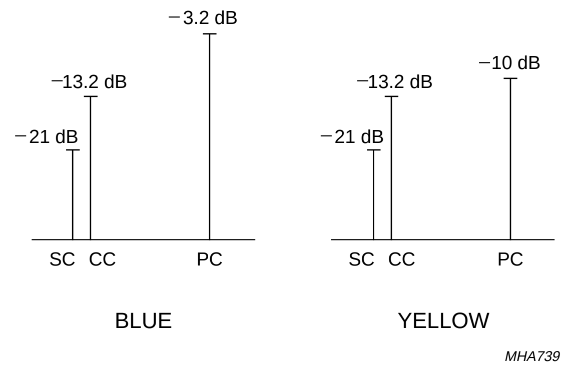


Fig.11 Typical signal-to-noise ratio as a function of VIF input voltage.



SC is sound carrier, with respect to sync level.

CC is chrominance carrier, with respect to sync level.

PC is picture carrier, with respect to sync level.

The sound carrier levels are taking into account a sound shelf attenuation of 14 dB (SAW filter G1984M).

Fig.12 Input signal conditions.

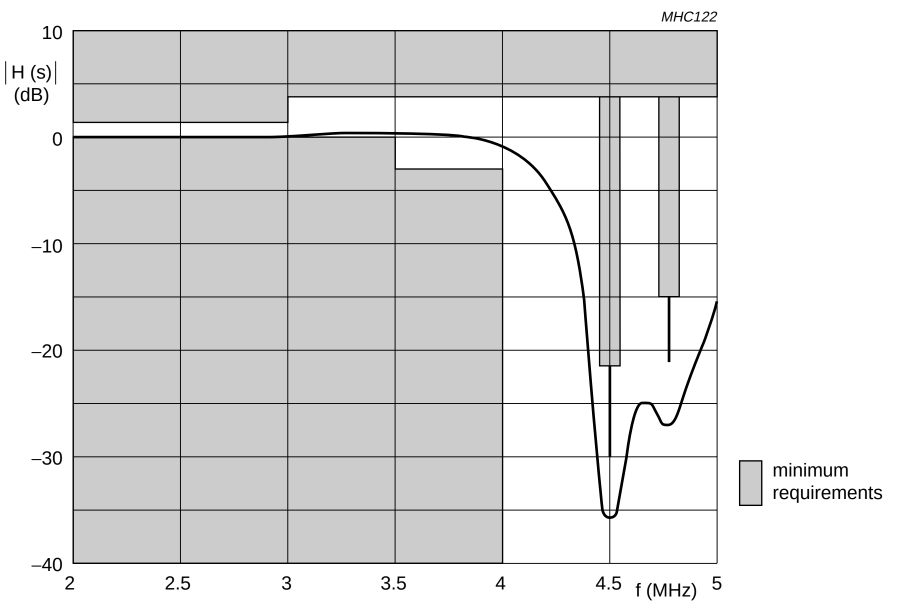
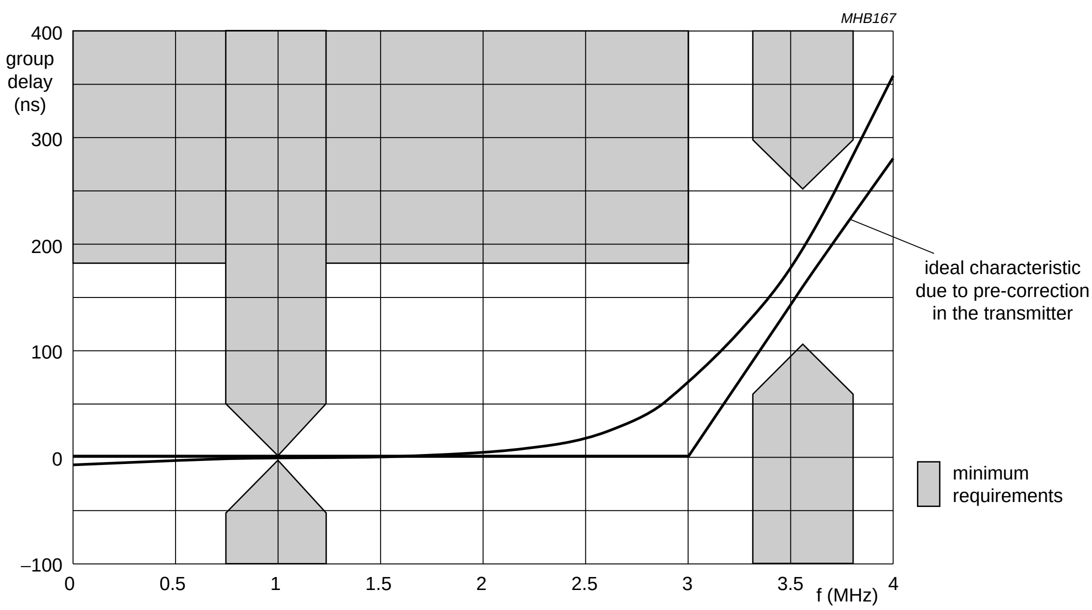


Fig.13 Typical amplitude response for sound trap at M/N standard (inclusive Korea).



Overall delay is not shown, here the maximum ripple is specified.

Fig.14 Typical group delay for sound trap at M/N standard.

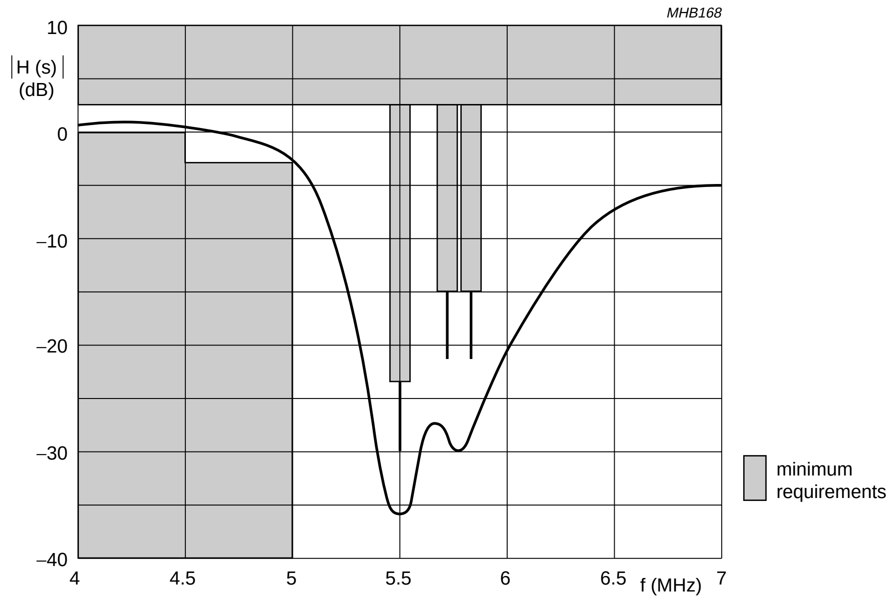
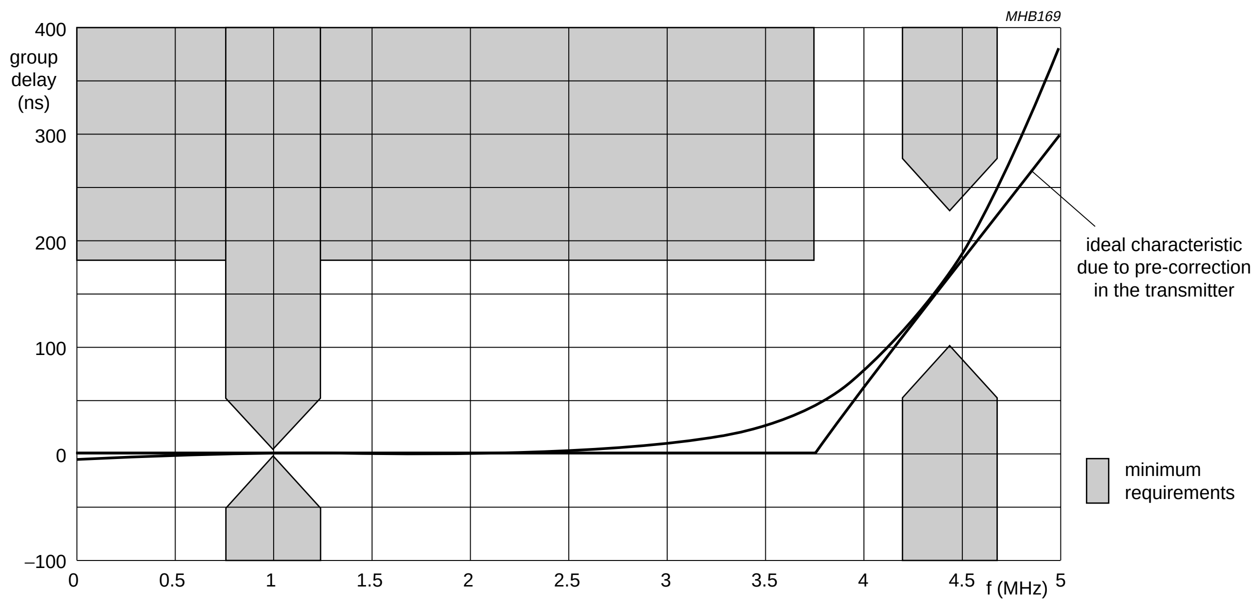


Fig.15 Typical amplitude response for sound trap at B/G standard.



Overall delay is not shown, here the maximum ripple is specified.

Fig.16 Typical group delay for sound trap at B/G standard.

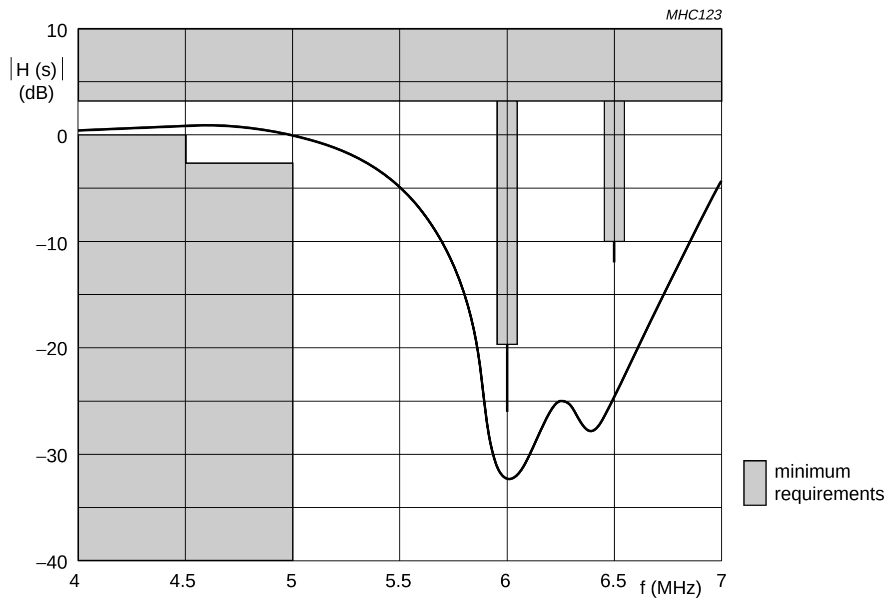


Fig.17 Typical amplitude response for sound trap at I standard.

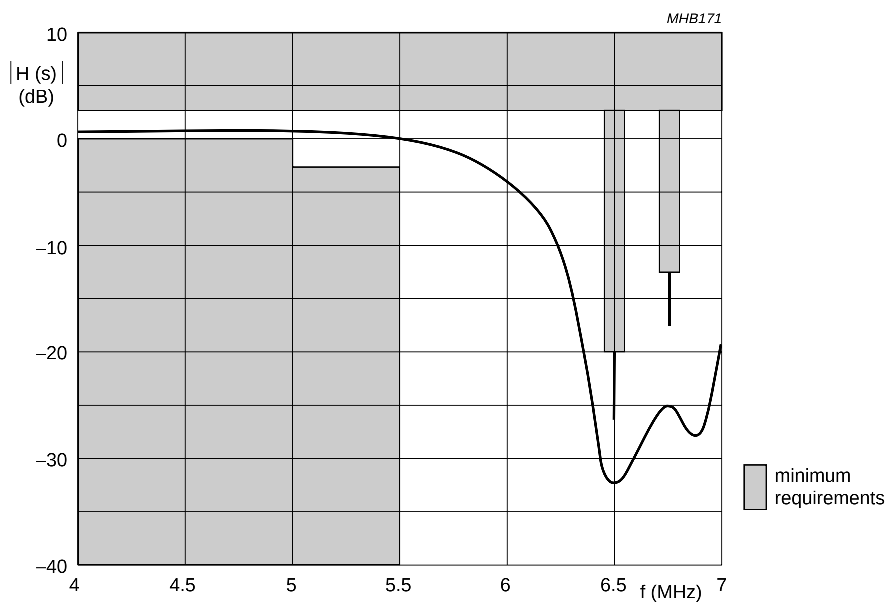
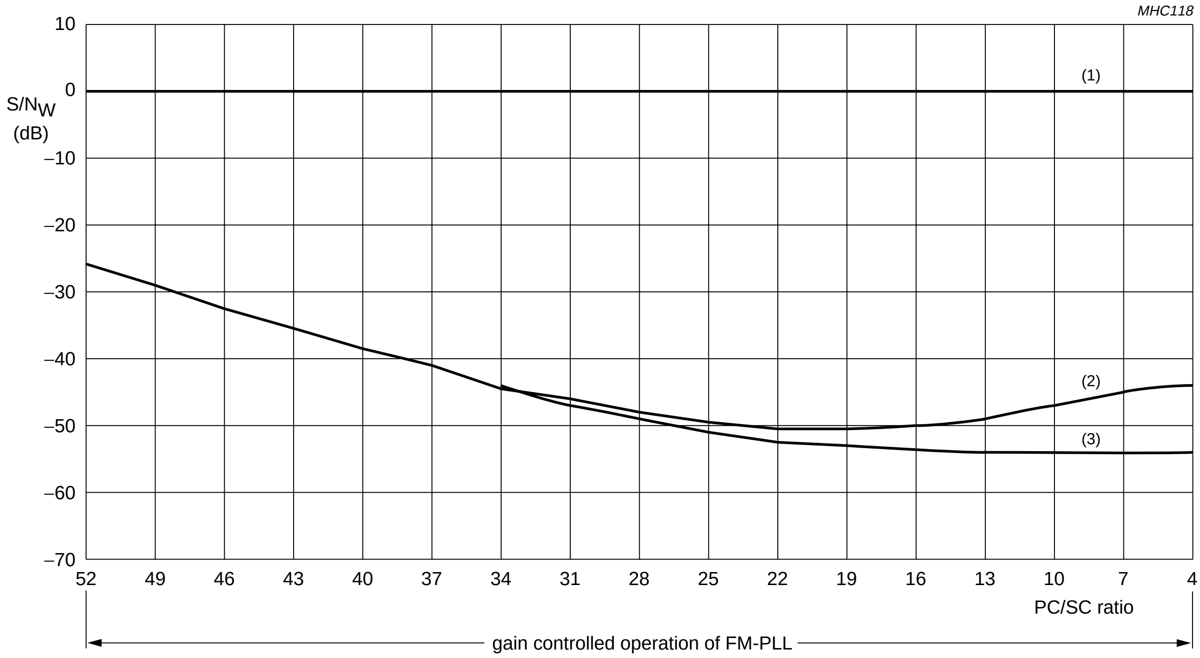


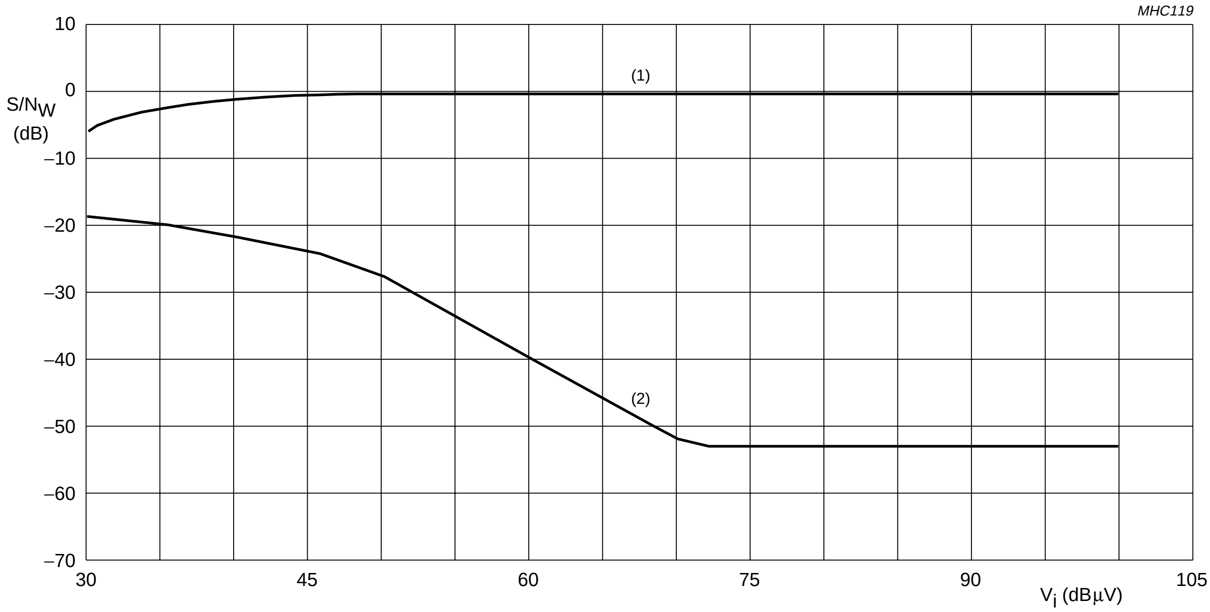
Fig.18 Typical amplitude response for sound trap at D/K standard.



(1) Signal.
(2) Noise at H-picture (CCIR weighted quasi peak).
(3) Noise at black picture (CCIR weighted quasi peak).

Conditions: PC/SC ratio measured at pins VIF1 and VIF2; via transformer; 27 kHz FM deviation; 50 µs de-emphasis.

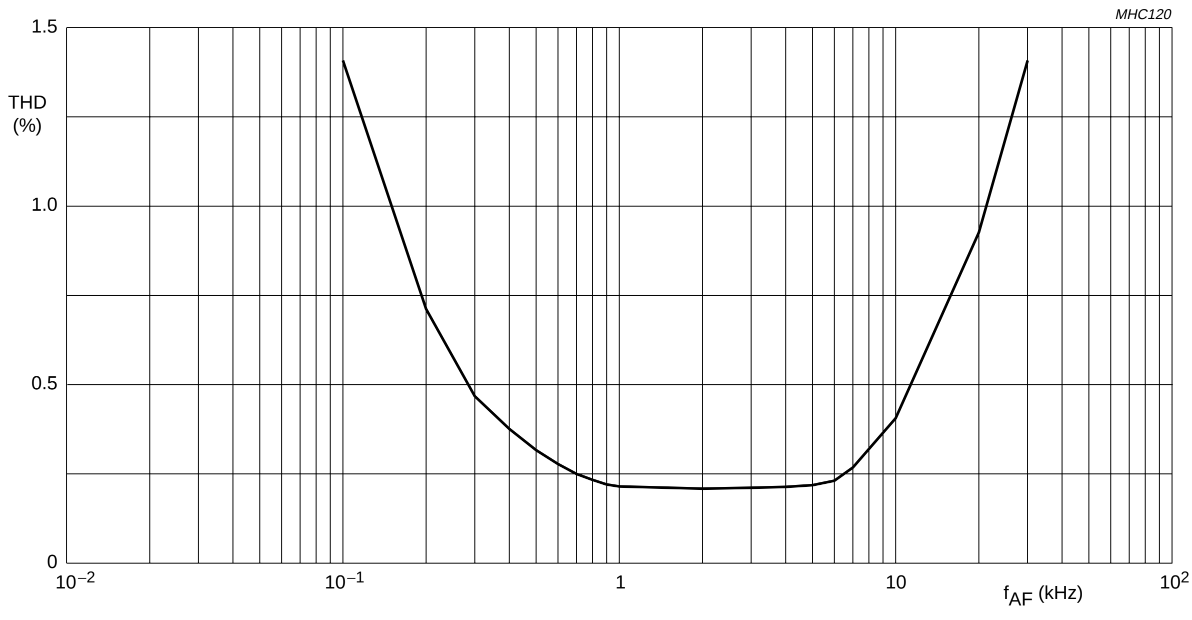
Fig.19 Audio signal-to-noise ratio as a function of picture-to-sound carrier ratio in intercarrier mode.



(1) Signal.
(2) Noise.

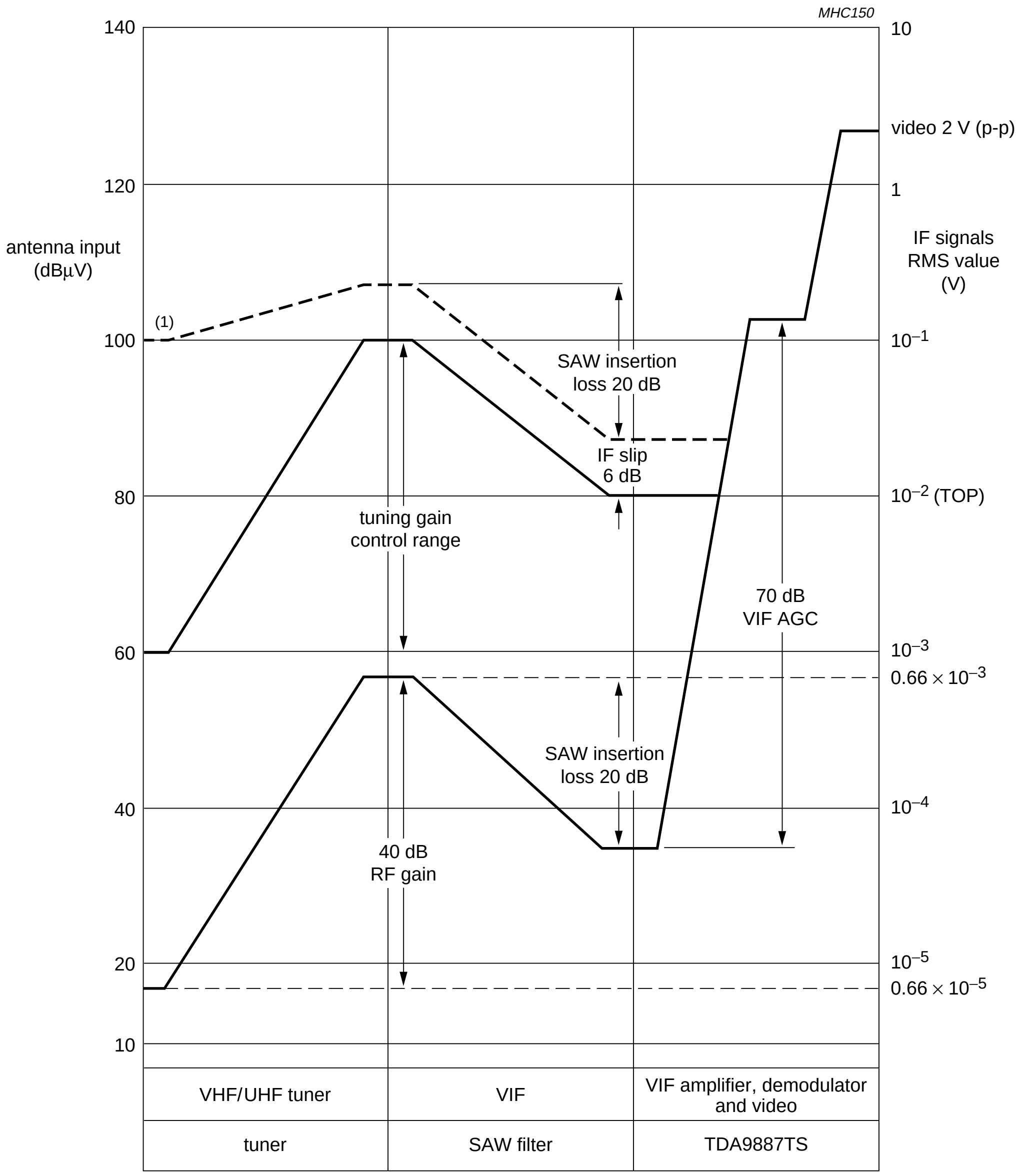
Condition: m = 54%.

Fig.20 Typical audio signal-to-noise ratio as a function of input signal at AM standard.



C_{AGC} = 2.2 μF; m = 54%.

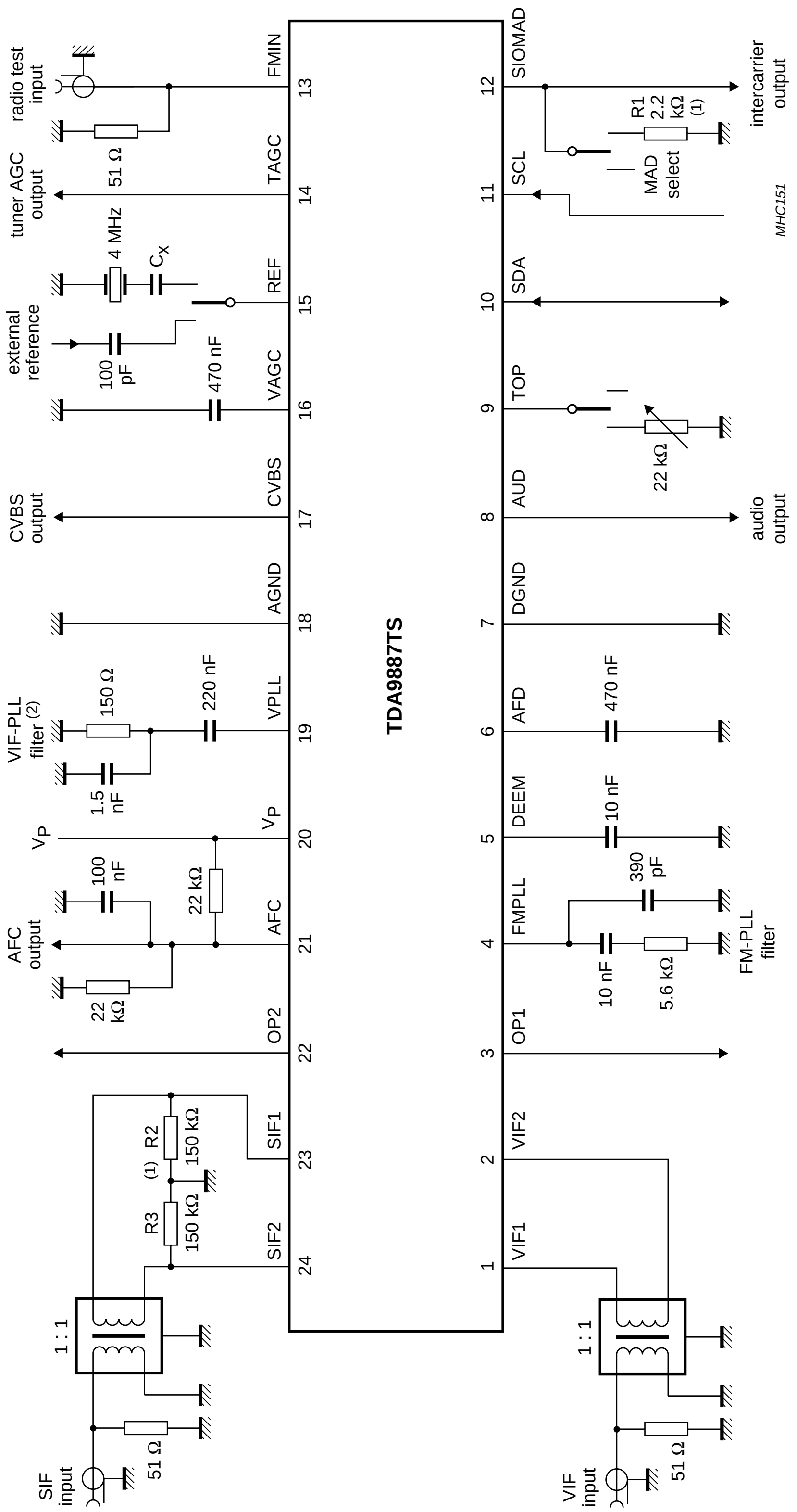
Fig.21 Typical total harmonic distortion as a function of audio frequency at AM standard.



(1) Depends on TOP.

Fig.22 Front-end level diagram.

13 TEST AND APPLICATION INFORMATION

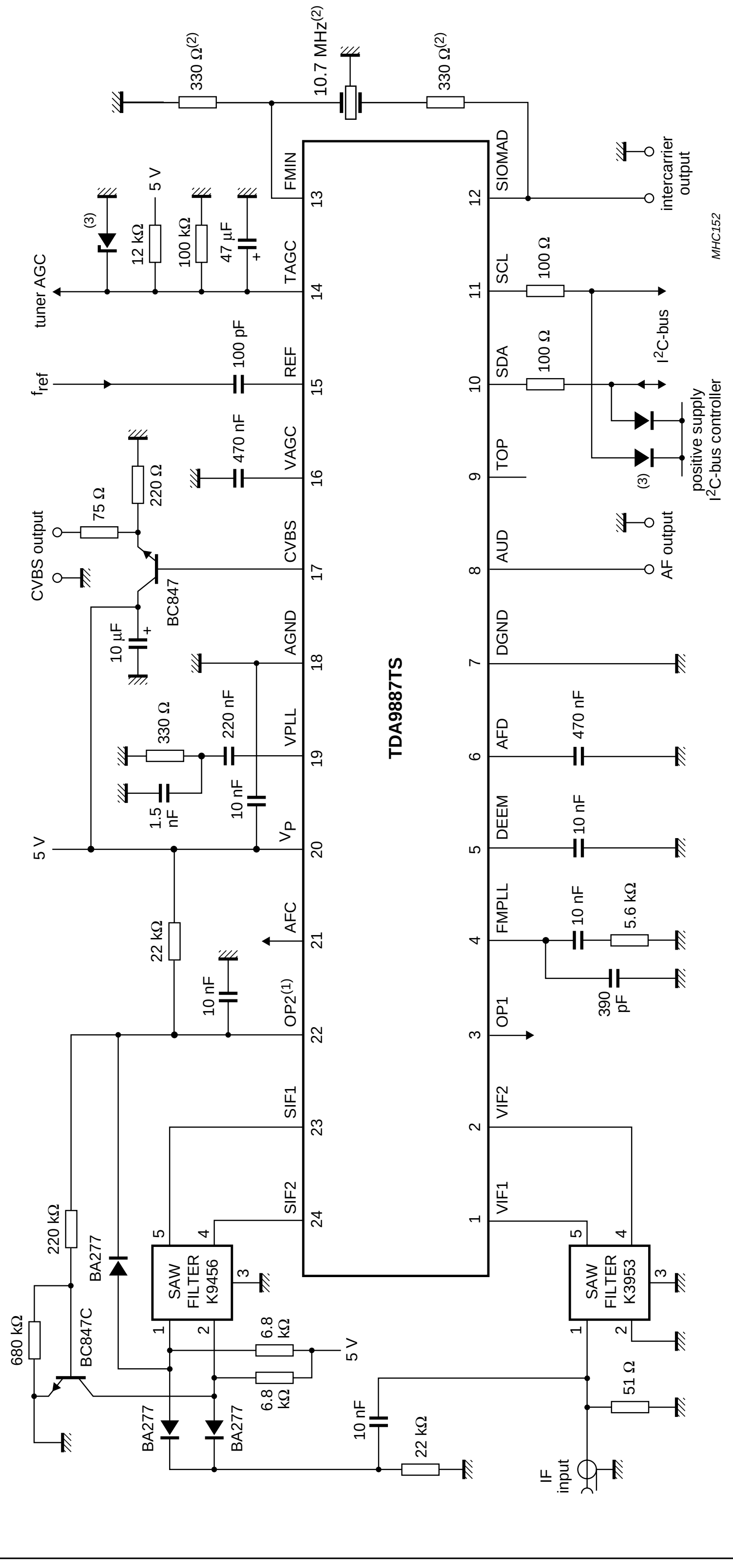


(1) Optional for I²C-bus address selection.

	R1 not used	R1 = 2.2 kΩ
R2 and R3 not used	1000 011 (R/$\overline{W}$)	1000 010 (R/$\overline{W}$)
R2 = R3 = 150 kΩ	1001 011 (R/$\overline{W}$)	1001 010 (R/$\overline{W}$)

(2) Different VIF loop filter in comparison with the application circuit due to different input characteristics (SAW filter or transformer).

Fig.23 Test circuit.



(1) If pin OP2 outputs VIF-AGC voltage, then pin OP1 can be used for SAW switching.

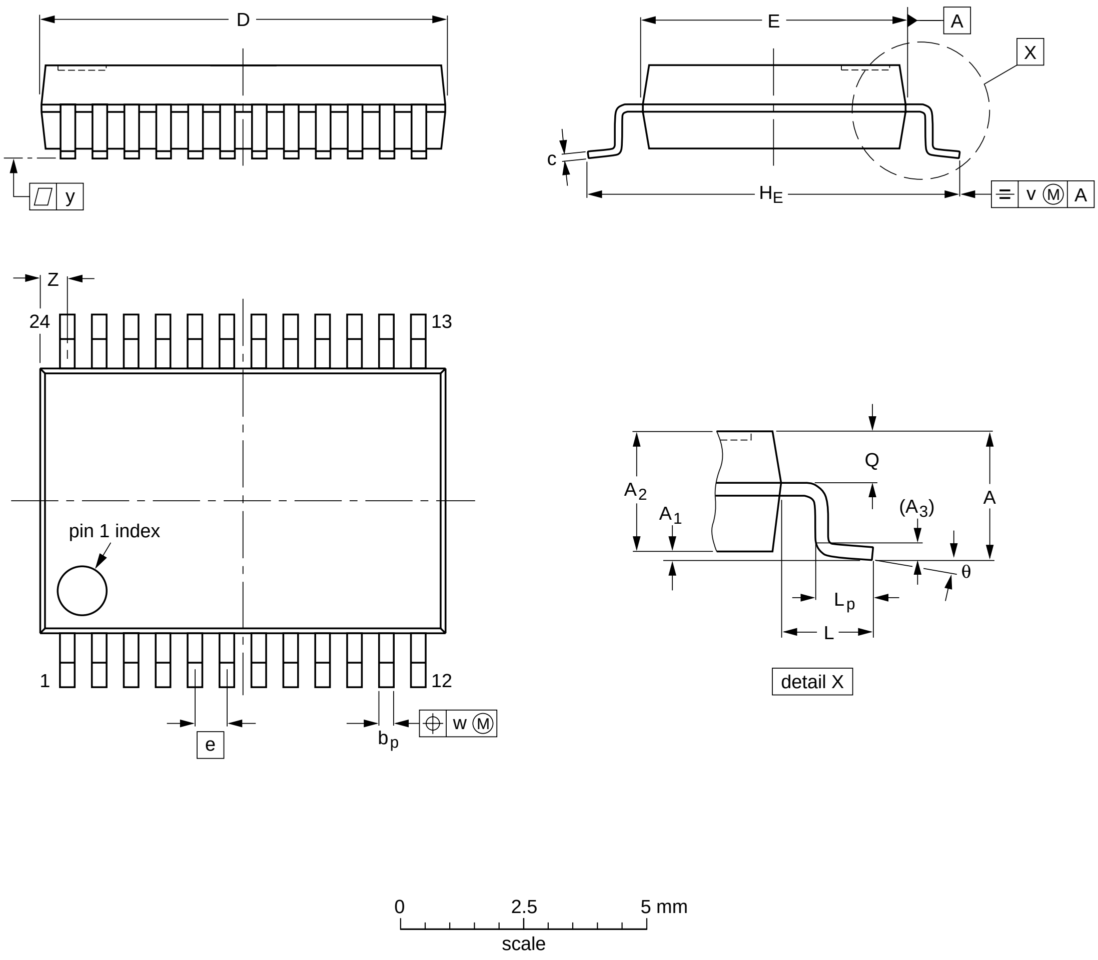
(2) Only for radio mode, not needed for external FM input mode.

(3) Optional measures to improve ESD performance within a TV-set application.

Fig.24 Application circuit.

14 PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

15 SOLDERING

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16 DATA SHEET STATUS

DATA SHEET STATUS(1)	PRODUCT STATUS(2)	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

17 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18 DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

19 PURCHASE OF PHILIPS I^{2}C COMPONENTS

Purchase of Philips I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C system provided the system conforms to the I^{2}C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit **http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**
For sales offices addresses send e-mail to: **sales.addresses@www.semiconductors.philips.com**.

SCA74

Printed in The Netherlands 753504/01/pp56 Date of release: 2002 Mar 05 Document order number: 9397 750 08986

Let's make things better.

Philips Semiconductors

PHILIPS