

Logic level TOPFET

PIP3106-D

DESCRIPTION

Monolithic temperature and overload protected logic level power MOSFET in **TOPFET2** technology assembled in a 3 pin surface mount plastic package.

APPLICATIONS

General purpose switch for driving

- lamps
- motors
- solenoids
- heaters

FEATURES

- TrenchMOS output stage
- Current limiting
- Overload protection
- Overtemperature protection
- Protection latched reset by input
- 5 V logic compatible input level
- Control of output stage and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Continuous drain source voltage	50	V
$I_D$	Continuous drain current	8	A
$P_D$	Total power dissipation	40	W
$T_j$	Continuous junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance	100	mΩ
$I_{ISL}$	Input supply current $V_{IS} = 5\text{ V}$	650	μA

FUNCTIONAL BLOCK DIAGRAM

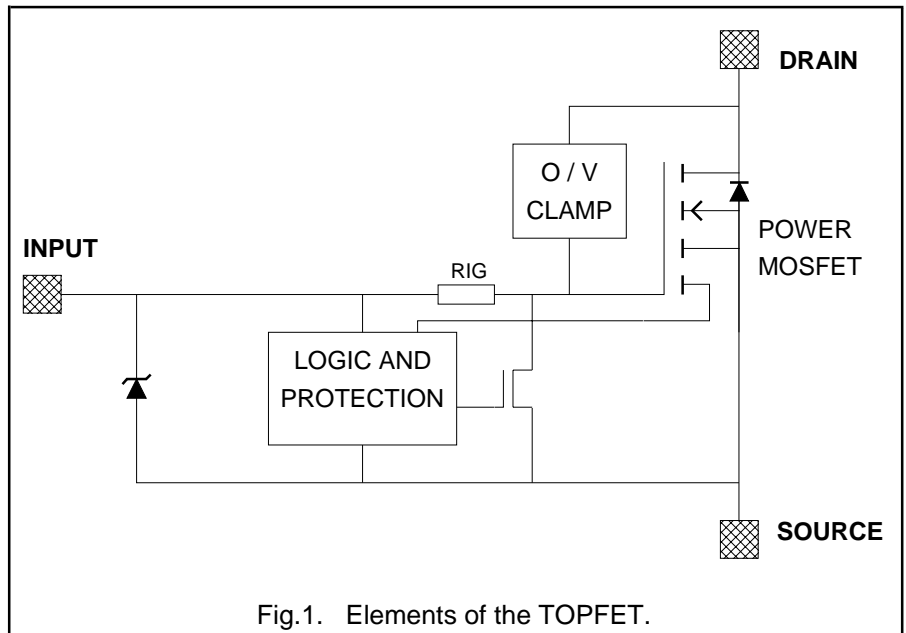
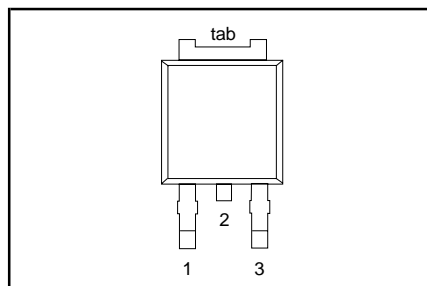


Fig.1. Elements of the TOPFET.

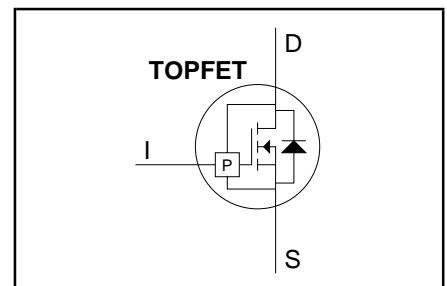
PINNING - SOT428

PIN	DESCRIPTION
1	input
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



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**LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Continuous drain source voltage <sup>1</sup>	-	-	50	V
$I_D$	Continuous drain current	$V_{IS} = 5\text{ V}; T_{mb} = 25\text{ °C}$	-	self - limited	A
$I_D$	Continuous drain current	$V_{IS} = 5\text{ V}; T_{mb} \leq 110\text{ °C}$	-	8	A
$I_I$	Continuous input current	-	-5	5	mA
$I_{IRM}$	Non-repetitive peak input current	$t_p \leq 1\text{ ms}$	-10	10	mA
$P_D$	Total power dissipation	$T_{mb} \leq 25\text{ °C}$	-	40	W
$T_{stg}$	Storage temperature	-	-55	175	°C
$T_j$	Continuous junction temperature <sup>2</sup>	normal operation	-	150	°C
$T_{sold}$	Case temperature	during soldering	-	260	°C

**ESD LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage	Human body model; $C = 250\text{ pF}; R = 1.5\text{ k}\Omega$	-	2	kV

**OVERVOLTAGE CLAMPING LIMITING VALUES**

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$E_{DSM}$	<b>Inductive load turn-off</b> Non-repetitive clamping energy	$I_{DM} = 8\text{ A}; V_{DD} \leq 20\text{ V}$ $T_{mb} \leq 25\text{ °C}$	-	100	mJ
$E_{DRM}$	Repetitive clamping energy	$T_{mb} \leq 95\text{ °C}; f = 250\text{ Hz}$	-	20	mJ

**OVERLOAD PROTECTION LIMITING VALUE**

With an adequate protection supply provided via the input pin, TOPFET can protect itself from two types of overload - overtemperature and short circuit load.

SYMBOL	PARAMETER	REQUIRED CONDITION	MIN.	MAX.	UNIT
$V_{DS}$	Drain source voltage <sup>3</sup>	$4\text{ V} \leq V_{IS} \leq 5.5\text{ V}$	0	35	V

**THERMAL CHARACTERISTIC**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	<b>Thermal resistance</b> Junction to mounting base	-	-	2.5	3.1	K/W
$R_{th\ j-a}$	Junction to ambient	minimum footprint FR4 PCB	-	70	-	K/W

<sup>1</sup> Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

<sup>2</sup> A higher  $T_j$  is allowed as an overload condition but at the threshold  $T_{j(TO)}$  the over temperature trip operates to protect the switch.

<sup>3</sup> All control logic and protection functions are disabled during conduction of the source drain diode.

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**OUTPUT CHARACTERISTICS**Limits are for  $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$ ; typicals are for  $T_{\text{mb}} = 25^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(\text{CL})\text{DSS}}$	<b>Off-state</b> Drain-source clamping voltage	$V_{\text{IS}} = 0 \text{ V}$	50	-	-	V
		$I_{\text{D}} = 10 \text{ mA}$ $I_{\text{DM}} = 1 \text{ A}; t_{\text{p}} \leq 300 \mu\text{s}; \delta \leq 0.01$	50	60	70	V
$I_{\text{DSS}}$	Drain source leakage current	$V_{\text{DS}} = 40 \text{ V}$	-	-	100	$\mu\text{A}$
		$T_{\text{mb}} = 25^{\circ}\text{C}$	-	0.1	10	$\mu\text{A}$
$R_{\text{DS(ON)}}$	<b>On-state</b> Drain-source resistance	$I_{\text{DM}} = 3 \text{ A}; t_{\text{p}} \leq 300 \mu\text{s}; \delta \leq 0.01$	-	-	190	$\text{m}\Omega$
		$V_{\text{IS}} \geq 4.4 \text{ V}$	-	68	100	$\text{m}\Omega$
		$V_{\text{IS}} \geq 4 \text{ V}$	-	-	200	$\text{m}\Omega$
		$T_{\text{mb}} = 25^{\circ}\text{C}$	-	72	105	$\text{m}\Omega$

**OVERLOAD CHARACTERISTICS** $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{\text{D}}$	<b>Short circuit load</b> Drain current limiting	$V_{\text{DS}} = 13 \text{ V}$	8	12	16	A
		$V_{\text{IS}} = 5 \text{ V};$ $4.4 \text{ V} \leq V_{\text{IS}} \leq 5.5 \text{ V}$	6	-	18	A
		$4 \text{ V} \leq V_{\text{IS}} \leq 5.5 \text{ V}$	5	-	18	A
$P_{\text{D(TO)}}$ $T_{\text{DSC}}$	<b>Overload protection</b> Overload power threshold Characteristic time	$V_{\text{IS}} = 5 \text{ V};$ device trips if $P_{\text{D}} > P_{\text{D(TO)}}$ which determines trip time <sup>1</sup>	20	55	80	W
		$T_{\text{mb}} = 25^{\circ}\text{C}$	200	350	600	$\mu\text{s}$
$T_{\text{j(TO)}}$	<b>Overtemperature protection</b> Threshold junction temperature <sup>2</sup>		150	170	-	$^{\circ}\text{C}$

<sup>1</sup> Trip time  $t_{\text{d,sc}}$  varies with overload dissipation  $P_{\text{D}}$  according to the formula  $t_{\text{d,sc}} \approx T_{\text{DSC}} / \ln[ P_{\text{D}} / P_{\text{D(TO)}} ]$ .<sup>2</sup> This is independent of the  $dV/dt$  of input voltage  $V_{\text{IS}}$ .

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**INPUT CHARACTERISTICS**

The supply for the logic and overload protection is taken from the input.

Limits are for  $-40^{\circ}\text{C} \leq T_{\text{mb}} \leq 150^{\circ}\text{C}$ ; typicals are for  $T_{\text{mb}} = 25^{\circ}\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{\text{IS(TO)}}$	Input threshold voltage	$V_{\text{DS}} = 5 \text{ V}; I_{\text{D}} = 1 \text{ mA}$ $T_{\text{mb}} = 25^{\circ}\text{C}$	0.6	-	2.4	V
			1.1	1.6	2.1	V
$I_{\text{IS}}$	Input supply current	normal operation; $V_{\text{IS}} = 5 \text{ V}$ $V_{\text{IS}} = 4 \text{ V}$	100	220	400	$\mu\text{A}$
			80	195	330	$\mu\text{A}$
$I_{\text{ISL}}$	Input supply current	protection latched; $V_{\text{IS}} = 5 \text{ V}$ $V_{\text{IS}} = 3 \text{ V}$	200	400	650	$\mu\text{A}$
			130	250	430	$\mu\text{A}$
$V_{\text{ISR}}$	Protection reset voltage <sup>1</sup>	reset time $t_{\text{r}} \geq 100 \mu\text{s}$	1.5	2	2.9	V
$t_{\text{r}}$	Latch reset time	$V_{\text{IS1}} = 5 \text{ V}, V_{\text{IS2}} < 1 \text{ V}$	10	40	100	$\mu\text{s}$
$V_{\text{(CL)IS}}$	Input clamping voltage	$I_{\text{I}} = 1.5 \text{ mA}$	5.5	-	8.5	V
$R_{\text{IG}}$	Input series resistance <sup>2</sup> to gate of power MOSFET	$T_{\text{mb}} = 25^{\circ}\text{C}$	-	33	-	$\text{k}\Omega$

**SWITCHING CHARACTERISTICS**

$T_{\text{mb}} = 25^{\circ}\text{C}$ ;  $V_{\text{DD}} = 13 \text{ V}$ ; resistive load  $R_{\text{L}} = 4 \Omega$ . Refer to waveform figure and test circuit.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{\text{d on}}$	Turn-on delay time	$V_{\text{IS}} = 5 \text{ V}$	-	10	20	$\mu\text{s}$
$t_{\text{r}}$	Rise time		-	20	40	$\mu\text{s}$
$t_{\text{d off}}$	Turn-off delay time	$V_{\text{IS}} = 0 \text{ V}$	-	30	60	$\mu\text{s}$
$t_{\text{f}}$	Fall time		-	20	40	$\mu\text{s}$

<sup>1</sup> The input voltage below which the overload protection circuits will be reset.

<sup>2</sup> Not directly measurable from device terminals.

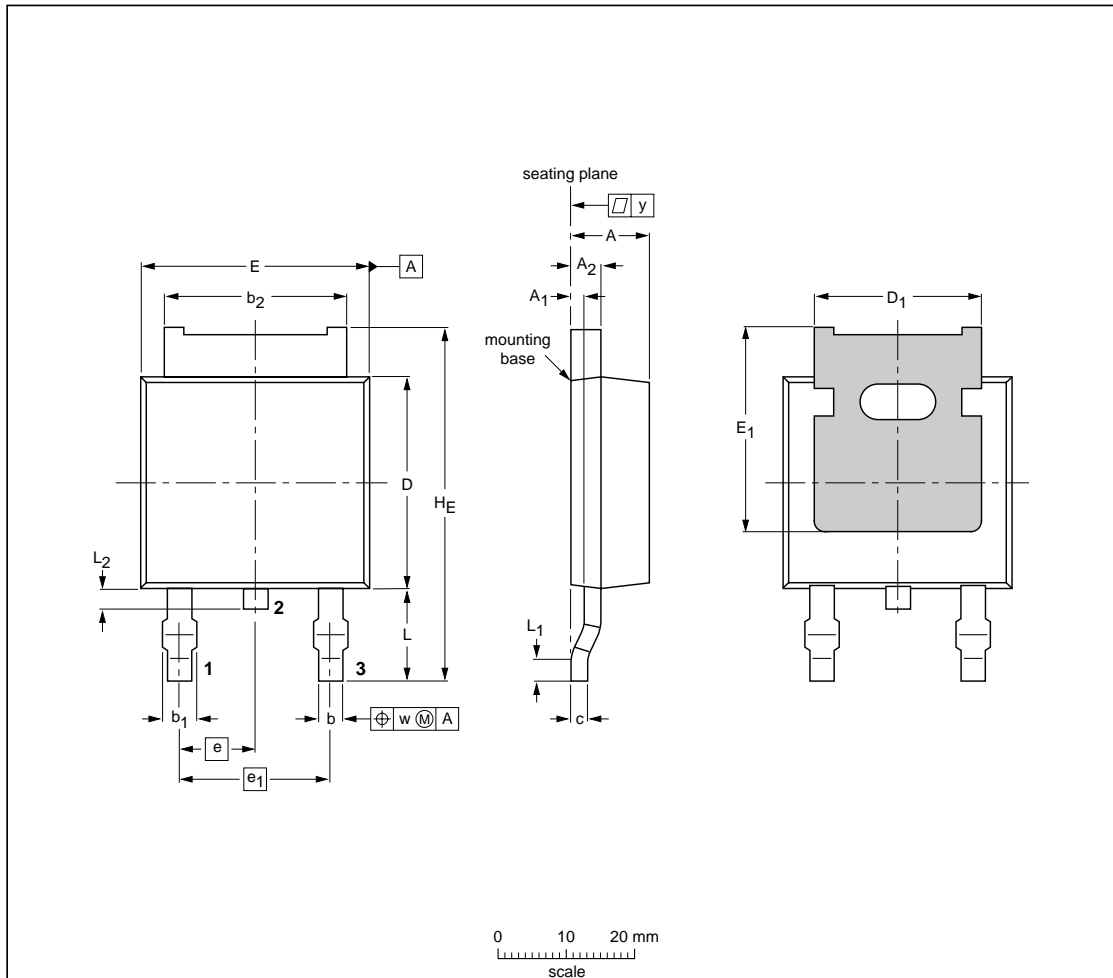
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MECHANICAL DATA

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads  
(one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub> (1)	A <sub>2</sub>	b	b <sub>1</sub> max.	b <sub>2</sub>	c	D max.	D <sub>1</sub> max.	E max.	E <sub>1</sub> min.	e	e <sub>1</sub>	H <sub>E</sub> max.	L	L <sub>1</sub> min.	L <sub>2</sub>	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT428					98-04-07

Fig.2. SOT428 surface mounting package<sup>1</sup>, centre pin connected to mounting base.

<sup>1</sup> Epoxy meets UL94 V0 at 1/8". Net mass: 1.1 g  
For soldering guidelines and SMD footprint design, please refer to Data Handbook SC18.

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**DEFINITIONS**

<b>DATA SHEET STATUS</b>		
<b>DATA SHEET STATUS<sup>1</sup></b>	<b>PRODUCT STATUS<sup>2</sup></b>	<b>DEFINITIONS</b>
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A
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<b>Application information</b>		
Where application information is given, it is advisory and does not form part of the specification.		
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