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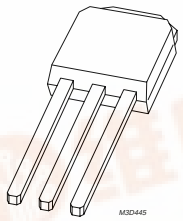



# PHU11NQ10T

TrenchMOS™ standard level FET

**Rev. 01 — 28 May 2002** **Product data**

## 1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHU11NQ10T in SOT533 (I-pak).

## 2. Features

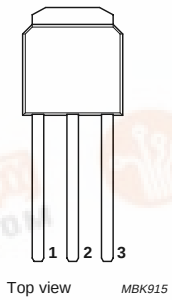
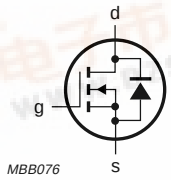
- TrenchMOS™ technology
- Fast switching
- Low on-state resistance.

## 3. Applications

- Relay driver
- High speed line driver
- General purpose switch.

## 4. Pinning information

**Table 1: Pinning - SOT533, simplified outline and symbol**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | gate (g) |   SOT533 |   |
| 2 | drain (d) | | |
| 3 | source (s) | | |
| tab | drain (d) | | |

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## 5. Quick reference data

**Table 2: Quick reference data**

| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 175 °C | - | 100 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V | - | 10.9 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C | - | 57.7 | W |
| $T_j$ | junction temperature | | - | 175 | °C |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 9 A; $T_j$ = 25 °C | 150 | 180 | mΩ |

## 6. Limiting values

**Table 3: Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | 25 °C ≤ $T_j$ ≤ 175 °C | - | 100 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ | - | 100 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±20 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; Figure 2 and 3 | - | 10.9 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 10 V; Figure 2 | - | 7.7 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; Figure 3 | - | 43.6 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Figure 1 | - | 57.7 | W |
| $T_{stg}$ | storage temperature | | –55 | +175 | °C |
| $T_j$ | junction temperature | | –55 | +175 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source (diode forward) current (DC) | $T_{mb}$ = 25 °C | - | 10.9 | A |
| $I_{SM}$ | peak source (diode forward) current | $T_{mb}$ = 25 °C; $t_p$ ≤ 10 µs | - | 43.6 | A |
| **Avalanche ruggedness** | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D$ = 3.2 A; $t_p$ = 0.2 ms; $V_{DD}$ ≤ 15 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; starting $T_j$ = 25 °C | - | 35 | mJ |


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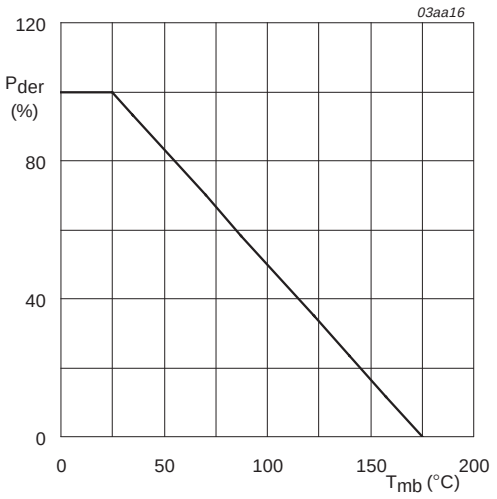
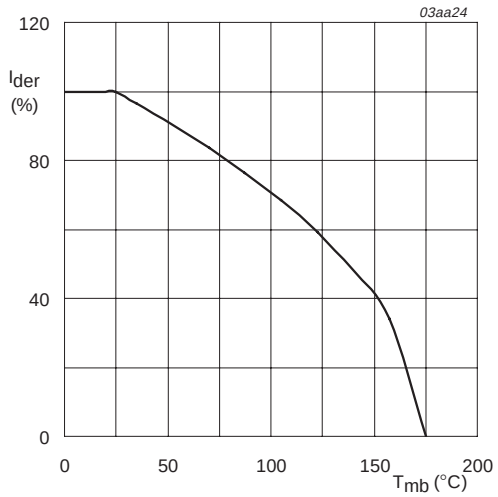


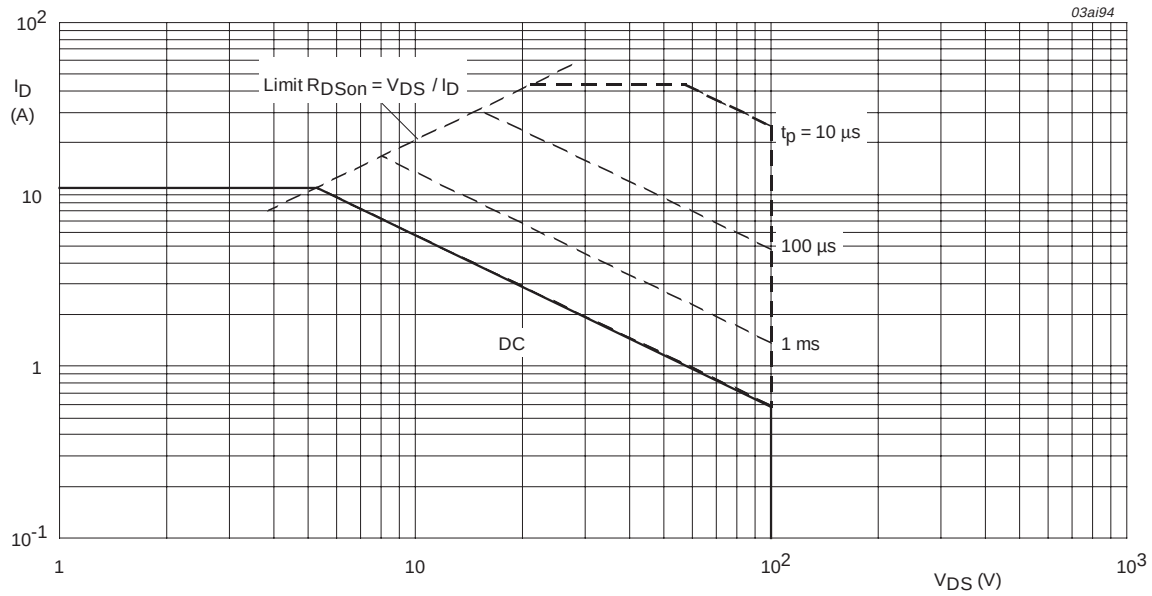

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**




$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature.**




$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse; $V_{GS}$ = 10V.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**



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# 7. Thermal characteristics

**Table 4: Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | - | - | 2.6 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | SOT533 package; vertical in still air | - | 70 | - | K/W |

## 7.1 Transient thermal impedance

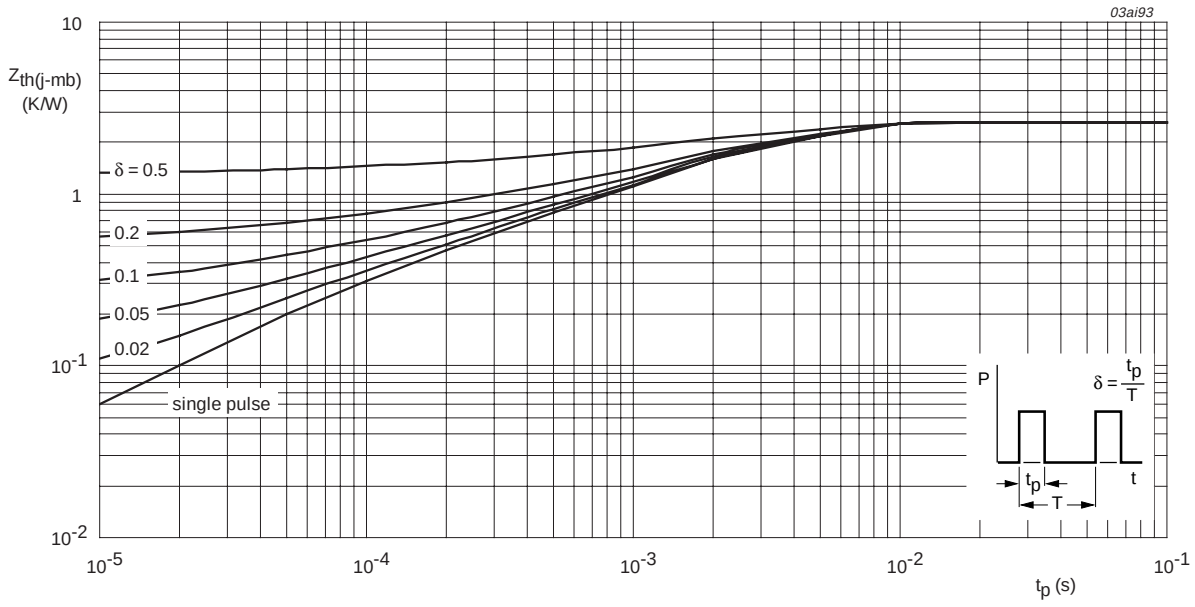


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**



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## 8. Characteristics

**Table 5: Characteristics**

*$T_j$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 250 µA | | | | |
| | | $T_j$ = 25 °C | 100 | 130 | - | V |
| | | $T_j$ = –55 °C | 89 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS}$ = $V_{GS}$; $I_D$ = 1 mA; Figure 9 | | | | |
| | | $T_j$ = 25 °C | 1 | 3 | 4 | V |
| | | $T_j$ = 175 °C | 0.6 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 4.6 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 100 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | 0.05 | 10 | µA |
| | | $T_j$ = 175 °C | - | 10 | 500 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{DS}$ = 0 V; $V_{GS}$ = ±10 V | - | 10 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 9 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 150 | 180 | mΩ |
| | | $T_j$ = 175 °C | - | - | 485 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $I_D$ = 11 A; $V_{DS}$ = 80 V; $V_{GS}$ = 10 V; Figure 13 | - | 14.7 | - | nC |
| $Q_{gs}$ | gate-source charge | | - | 2.3 | - | nC |
| $Q_{gd}$ | gate-drain (Miller) charge | | - | 5.3 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; Figure 11 | - | 360 | - | pF |
| $C_{oss}$ | output capacitance | | - | 60 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 40 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 50 V; $R_D$ = 4.7 Ω; $V_{GS}$ = 10 V; $R_G$ = 5.6 Ω | - | 5.5 | - | ns |
| $t_r$ | rise time | | - | 23 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 11.5 | - | ns |
| $t_f$ | fall time | | - | 7.2 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 11 A; $V_{GS}$ = 0 V; Figure 12 | - | 1 | 1.5 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 4 A; $dI_S/dt$ = –100 A/µs; $V_{GS}$ = 0 V | - | 55 | - | ns |
| $Q_r$ | recovered charge | | - | 85 | - | nC |


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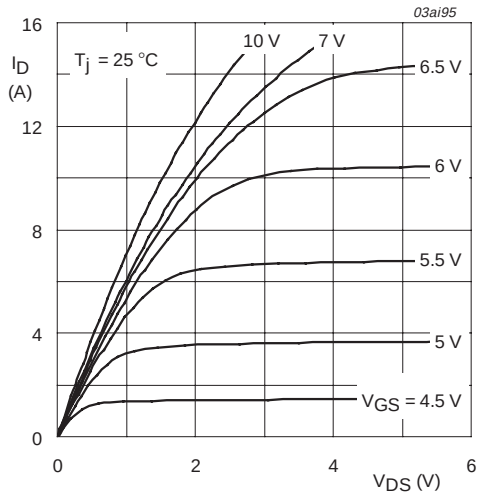
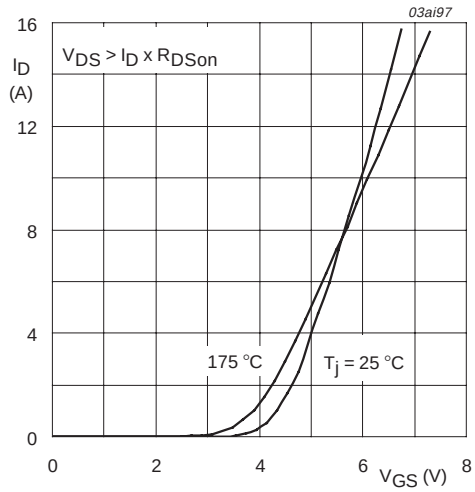


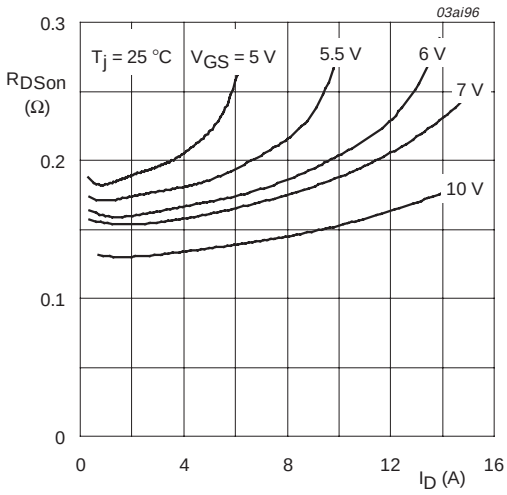

$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



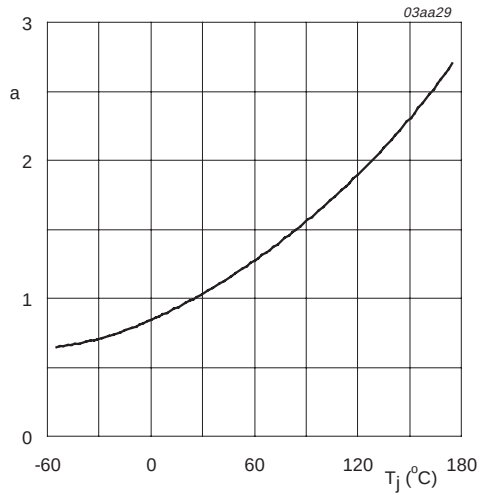

$T_j$ = 25 °C and 175 °C; $V_{DS}$ > $I_D$ x $R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**




$T_j$ = 25 °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



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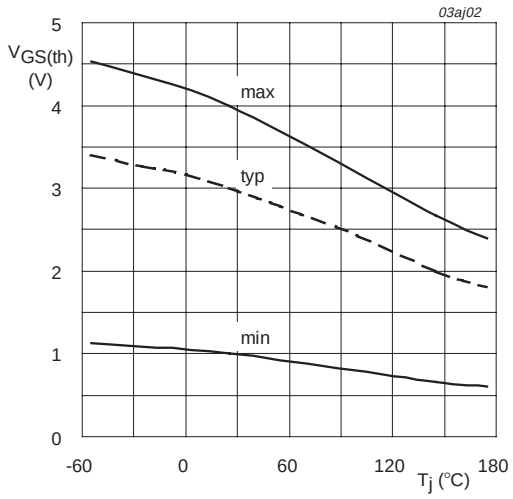
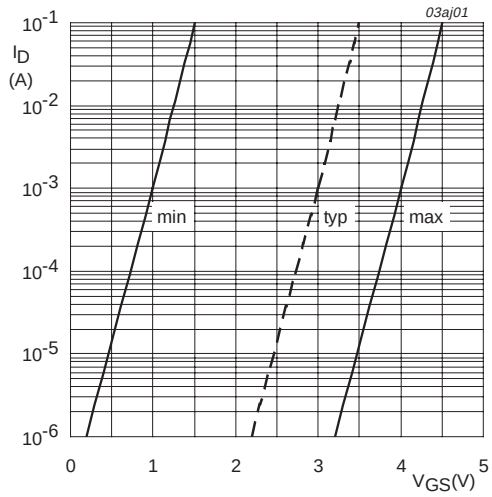


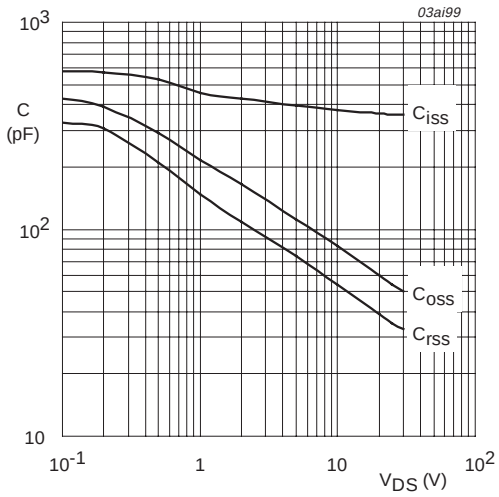

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**




$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



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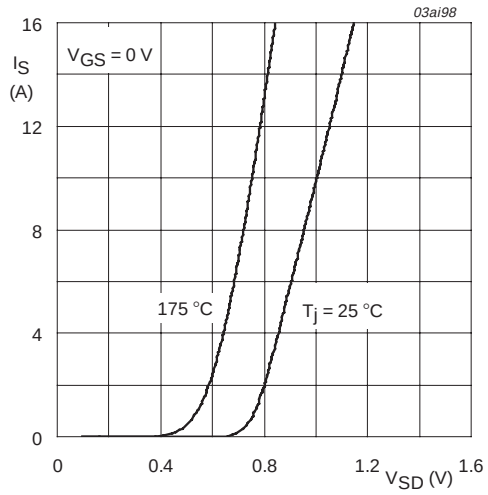
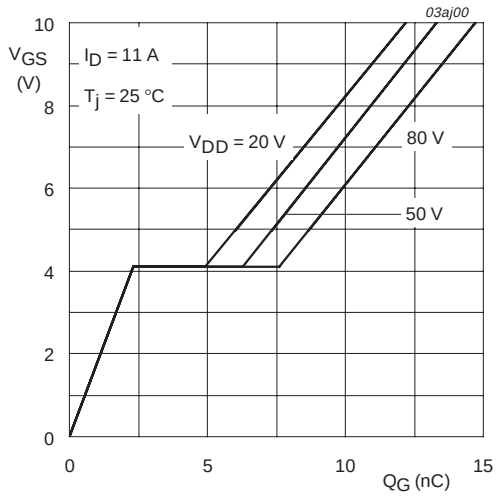



$T_j$ = 25 °C and 175 °C; $V_{GS}$ = 0 V

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**




$I_D$ = 11 A; $V_{DD}$ = 20 V, 50 V, 80 V

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**



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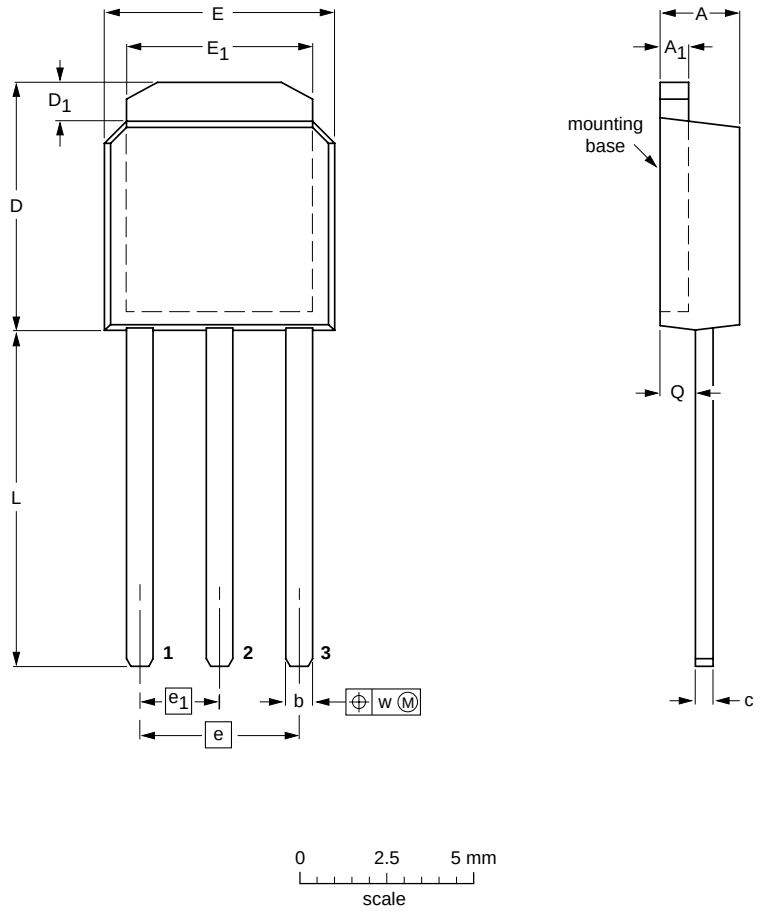
## 9. Package outline

**Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line)** **SOT533**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | b | c | D | $D_1$ | E | $E_1$ | e | $e_1$ | L | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.89<br>0.71 | 0.89<br>0.71 | 0.56<br>0.46 | 7.28<br>6.94 | 1.06<br>0.96 | 6.73<br>6.47 | 5.36<br>5.26 | 4.57 | 2.285 | 9.8<br>9.4 | 1.00<br>1.10 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT533 | | TO-251 | | | | 99-02-18 |

**Fig 14. SOT533. (I-PAK)**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## 10. Revision history

Table 6: Revision history

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 1 | 20020528 | - | Product data; initial version. |


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## 11. Data sheet status

| Data sheet status[1] | Product status[2] | Definition |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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