

# DATA SHEET

**PCK2002PL**

533 MHz PCI-X clock buffer

Product data

Supersedes data of 2002 Mar 15

2002 Oct 10

## 533 MHz PCI-X clock buffer

## PCK2002PL

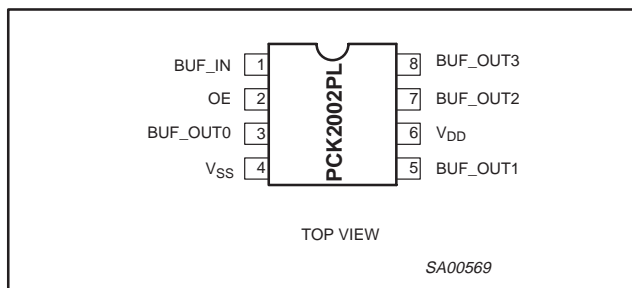
## FEATURES

- General purpose and PCI-X 1:4 clock buffer
- 8-pin TSSOP 3.1 × 4.4 mm package
- Same form, fit, and function as CDCV304
- See PCK2001P for 3.1 × 3.1 mm TSSOP-8 package
- See PCK2001 or PCK2002 for 48-pin 1:18 buffer part
- See PCK2001M to PCK2002M for 28-pin 1:10 buffer part
- See PCK2001R for 16-pin 1:6 buffer part
- Operating frequency: 0 – 533 MHz
- Part-to-part skew < 500 ps
- Low output skew: <200 ps
- 3.3 V operation
- ESD classification testing is done to JEDEC Standard JESD22. Protection exceeds 2000 V to HBM per method A114.

## DESCRIPTION

The PCK2002PL is a 1–4 fanout buffer used as a high-performance, low skew, general purpose and PCI-X clock buffer. It distributes one input clock (BUF\_IN) signal to four output clocks (BUF\_OUT<sub>n</sub>).

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	I/O TYPE	SYMBOL	FUNCTION
1	Input	BUF_IN	Buffered clock input
3, 5, 7, 8	Output	BUF_OUT (0–3)	Buffered clock outputs
6	Input	V <sub>DD</sub>	3.3 V supply
2	Input	OE	Output Enable
4	Input	V <sub>SS</sub>	Ground

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay BUF_IN to BUF_OUT <sub>n</sub>	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 25 pF	2.9 2.8	ns
t <sub>r</sub>	Rise time	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 10 pF, 0.2V <sub>DD</sub> to 0.6V <sub>DD</sub>	450	ps
t <sub>f</sub>	Fall time	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 10 pF, 0.6V <sub>DD</sub> to 0.2V <sub>DD</sub>	400	ps
I <sub>CC</sub>	Total supply current	V <sub>CC</sub> = 3.6 V	50	μA

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
8-Pin Plastic TSSOP	–40 to +85 °C	PCK2002PLPW	SOT530-1

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## FUNCTION TABLE

OE	BUF_IN	BUF_OUTn
L	X	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134).  
 Voltages are referenced to  $V_{SS}$  ( $V_{SS} = 0$  V).

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
$V_{DD}$	DC 3.3 V supply voltage		-0.5	+4.3	V
$I_{IK}$	DC input diode current	$V_I < 0$	—	-50	mA
$V_I$	DC input voltage	Note 2	-0.5	$V_{DD} + 0.5$	V
$I_{OK}$	DC output diode current	$V_O > V_{DD}$ or $V_O < 0$	—	±50	mA
$V_O$	DC output voltage	Note 2	-0.5	$V_{DD} + 0.5$	V
$I_O$	DC output source or sink current	$V_O \geq 0$ to $V_{DD}$	—	±50	mA
$T_{stg}$	Storage temperature range		-65	+150	°C
$P_{tot}$	Power dissipation per package plastic medium-shrink SO (SSOP)	For temperature range: 0 to +70 °C above +55 °C derate linearly with 11.3 mW/K	—	850	mW

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{DD}$	DC 3.3V supply voltage		3.0	3.6	V
$C_L$	Capacitive load		20	30	pF
$V_I$	DC input voltage range		0	$V_{DD}$	V
$V_O$	DC output voltage range		0	$V_{DD}$	V
$T_{amb}$	Operating ambient temperature range in free air		-40	+85	°C

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## DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS			LIMITS		UNIT
					$T_{\text{amb}} = -40 \text{ to } +85\text{ }^{\circ}\text{C}$		
		$V_{\text{DD}}$ (V)	OTHER		MIN	MAX	
$V_{\text{IH}}$	HIGH level input voltage	3.0 to 3.6	—	—	2.0	$V_{\text{DD}} + 0.3$	V
$V_{\text{IL}}$	LOW level input voltage	3.0 to 3.6	—	—	$V_{\text{SS}} - 0.3$	0.8	V
$V_{\text{OH}}$	Output HIGH voltage	3.0 to 3.6	$I_{\text{OH}} = -1\text{ mA}$	—	$V_{\text{DD}} - 0.2$	—	V
		3.0	$I_{\text{OH}} = -24\text{ mA}$	—	2.0	—	V
		3.0	$I_{\text{OH}} = -12\text{ mA}$	—	2.4	—	V
$V_{\text{OL}}$	Output LOW voltage	3.0 to 3.6	$I_{\text{OL}} = 1\text{ mA}$	—	—	0.2	V
		3.0	$I_{\text{OL}} = 24\text{ mA}$	—	—	0.8	V
		3.0	$I_{\text{OL}} = 12\text{ mA}$	—	—	0.55	V
$I_{\text{OH}}$	Output HIGH current	3.0	$V_{\text{OUT}} = 1\text{ V}$	—	-50	—	mA
		3.3	$V_{\text{OUT}} = 1.65\text{ V}$	—	—	-150	mA
$I_{\text{OL}}$	Output LOW current	3.0	$V_{\text{OUT}} = 2.0\text{ V}$	—	60	—	mA
		3.3	$V_{\text{OUT}} = 1.65\text{ V}$	—	—	150	mA
$\pm I_{\text{I}}$	Input leakage current	3.6	$V_{\text{I}} = V_{\text{DD}}$ or GND	—	—	$\pm 5$	$\mu\text{A}$
$I_{\text{CC}}$	Quiescent supply current	3.6	$V_{\text{I}} = V_{\text{DD}}$ or GND	$I_{\text{O}} = 0$	—	100	$\mu\text{A}$

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## AC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS $T_{amb} = -40 \text{ to } +85 \text{ }^{\circ}\text{C}$			UNIT
				MIN	TYP <sup>6</sup>	MAX	
$T_H$	CLK HIGH time	66 MHz	2	6.0	—	—	ns
$T_L$	CLK LOW time		3	6.0	—	—	ns
$T_H$	CLK HIGH time	140 MHz	2	2.9	—	—	ns
$T_L$	CLK LOW time		3	3.0	—	—	ns
$T_R$	Output rise slew rate		4	2.15	3.3	4.1	V/ns
$T_F$	Output fall slew rate		4	2.5	3.3	4.4	V/ns
$T_{PLH}$	Buffer LH propagation delay		5	1.8	2.9	3.4	ns
$T_{PHL}$	Buffer HL propagation delay		5	1.8	2.8	3.4	ns
$T_{SKW}$	Bus CLK skew		1	—	—	200	ps
$T_{DDSKW}$	Device to device skew		1	—	—	500	ps

### NOTES:

1. CLK skew is only valid for equal loading of all outputs.
2.  $T_H$  is measured at  $0.5 V_{DD}$  as shown in Figure 2.
3.  $T_L$  is measured at  $0.35 V_{DD}$  as shown in Figure 2.
4.  $T_R$  and  $T_F$  are measured as a transition through the threshold region  $0.2 V_{DD}$  to  $0.6 V_{DD}$  and  $0.6 V_{DD}$  to  $0.2 V_{DD}$ .
5. Input edge rate for these tests must be faster than  $1 \text{ V/ns}$ .
6. All typical values are at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ .

## AC WAVEFORMS

$V_M = 50\% V_{DD}$

$C_L = 10 \text{ pF}$

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

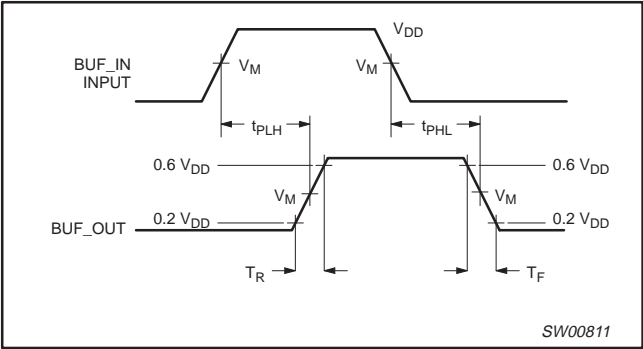


Figure 1. Load circuitry for switching times.

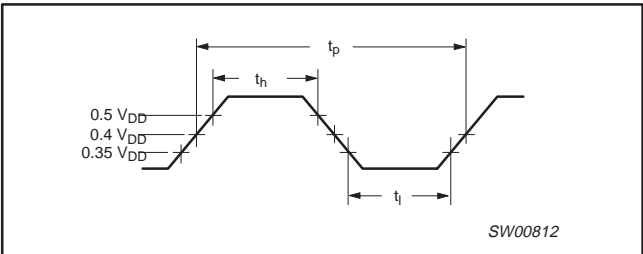


Figure 2. Buffer Output clock

## TEST CIRCUIT

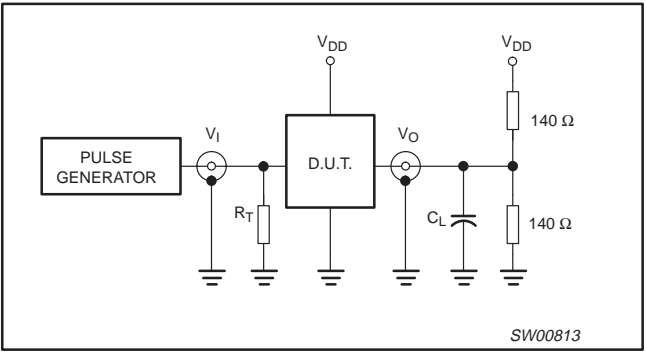


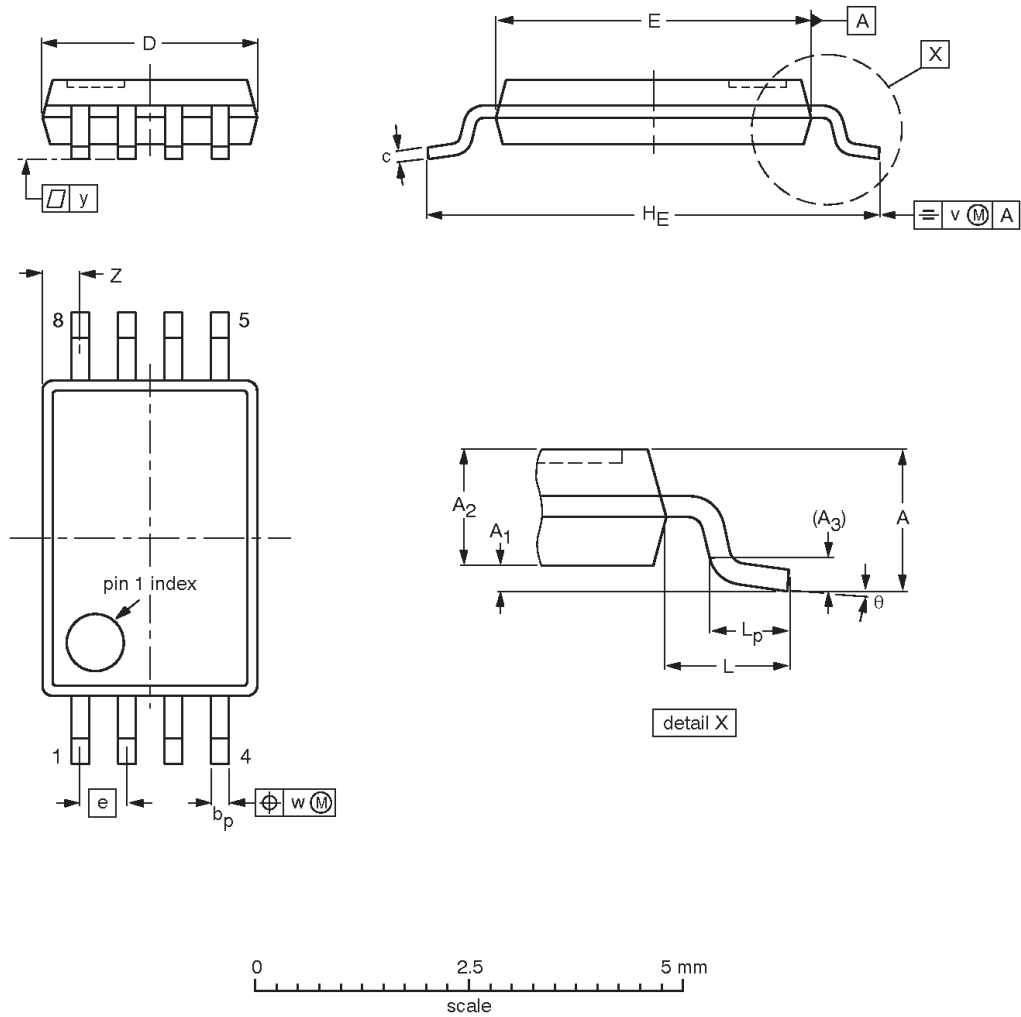
Figure 3. Load circuitry for switching times

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TSSOP8: plastic thin shrink small outline; 8 leads; body width 4.4 mm

SOT530-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.10 2.90	4.50 4.30	0.65	6.50 6.30	0.94	0.70 0.50	0.10	0.10	0.10	0.70 0.35	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT530-1		MO-153				99-12-27 00-02-24

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**REVISION HISTORY**

Rev	Date	Description
_3	2002 Oct 10	Product data (9397 750 10537); third version supersedes Product data second version, 2002 Mar 15. Engineering Change Notice: 853-2243 29056 (2002 Oct 09). Modifications: Update and change to Operating Frequency values.
_2	2002 Mar 15	Product data, second version Engineering Change Notice: 853-2256 27859 (date: 2002 Mar 15).

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## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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