

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4585B

MSI

4-bit magnitude comparator

Product specification
File under Integrated Circuits, IC04

January 1995

4-bit magnitude comparator

HEF4585B

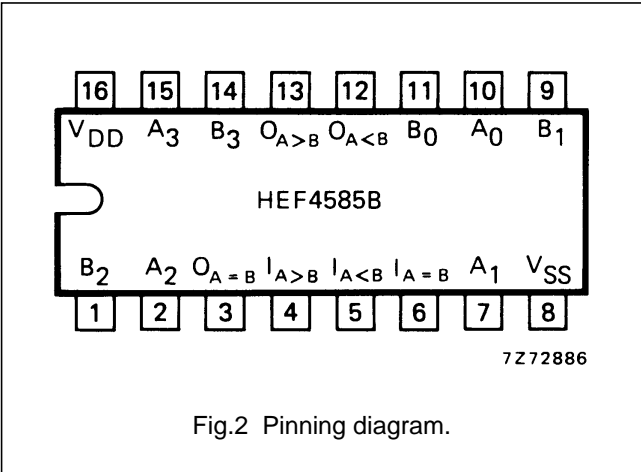
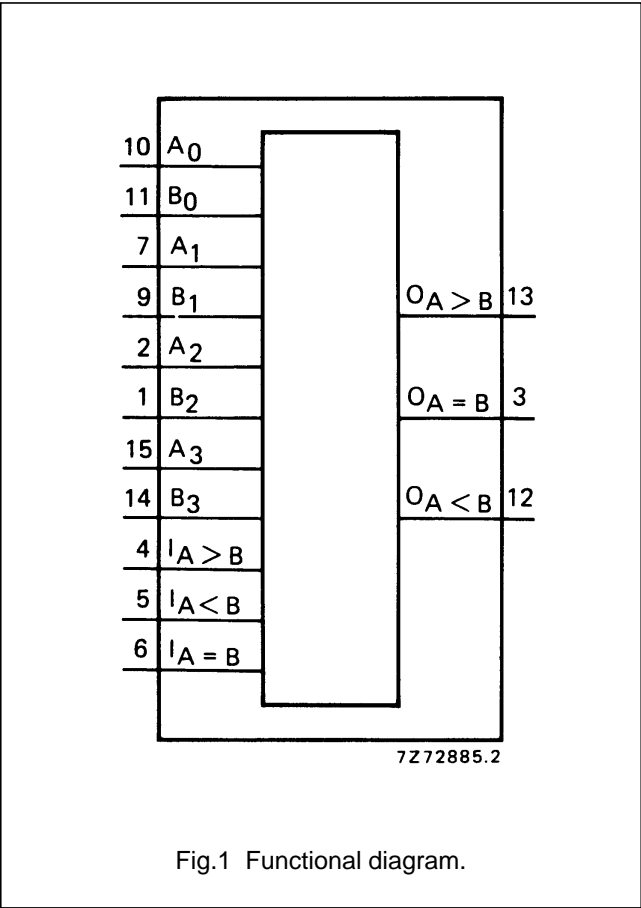
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DESCRIPTION

The HEF4585B is a 4-bit magnitude comparator which compares two 4-bit words (A and B), whether they are 'less than', 'equal to', or 'greater than'. Each word has four parallel inputs (A_0 to A_3 and B_0 to B_3); A_3 and B_3 being the most significant inputs. Three outputs are provided; A greater than B ($O_{A > B}$), A less than B ($O_{A < B}$) and A equal to B ($O_{A = B}$). Three expander inputs ($I_{A > B}$, $I_{A < B}$ and $I_{A = B}$) allow cascading of the devices without external gates.

For proper compare operation the expander inputs to the least significant position must be connected as follows: $I_{A = B} = I_{A > B} = \text{HIGH}$, $I_{A < B} = \text{LOW}$. For words greater than 4-bits, units can be cascaded by connecting outputs $O_{A < B}$ and $O_{A = B}$ to the corresponding inputs of the next significant comparator (input $I_{A > B}$ is connected to a HIGH).

Operation is not restricted to binary codes, the devices will work with any monotonic code. The function table describes the operation of the device under all possible logic conditions.



- HEF4585BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4585BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4585BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

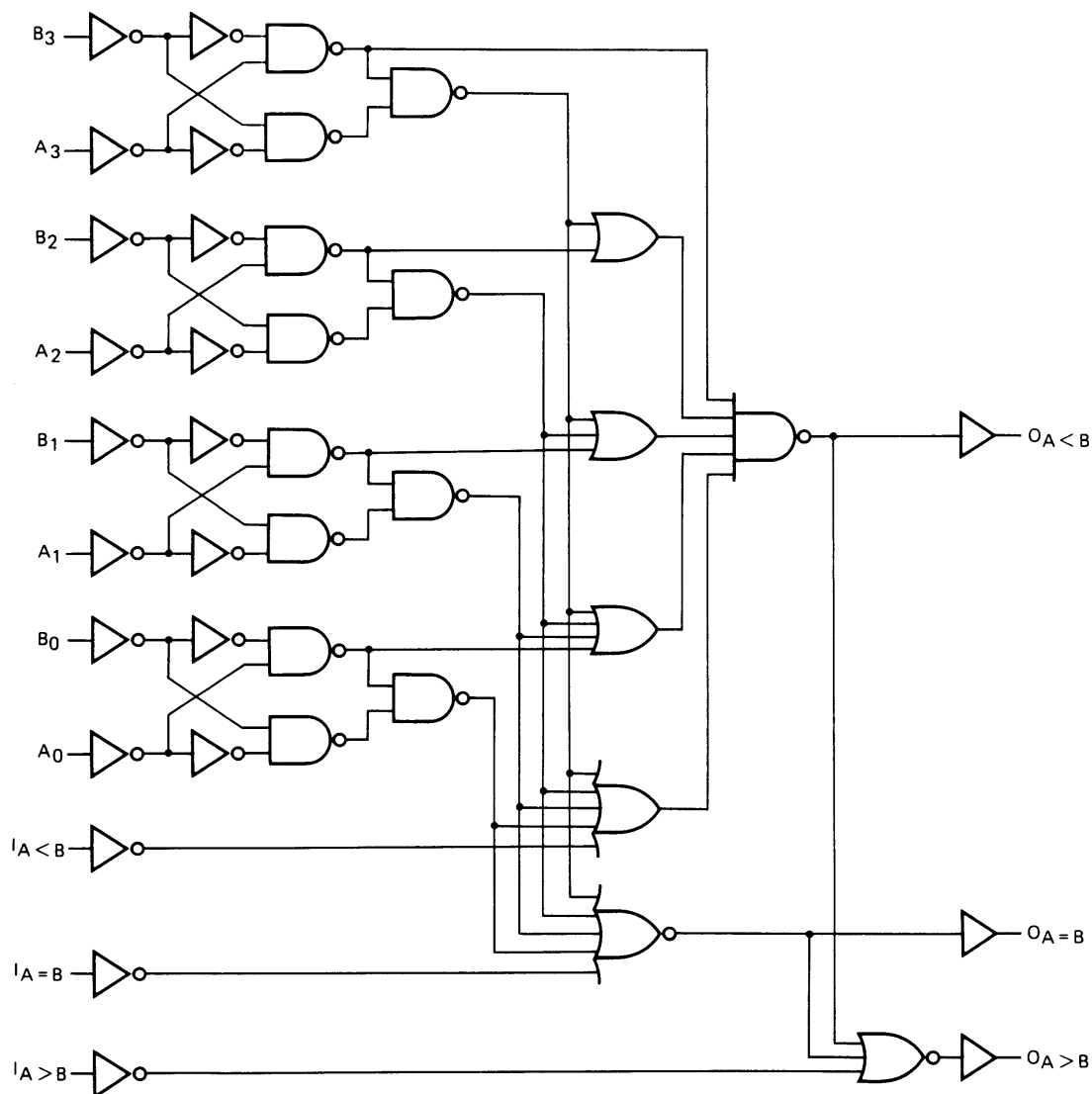
PINNING

- A_0 to A_3 word A parallel inputs
- B_0 to B_3 word B parallel inputs
- $I_{A > B}$, $I_{A < B}$, $I_{A = B}$ expander inputs
- $O_{A > B}$ A greater than B output
- $O_{A < B}$ A less than B output
- $O_{A = B}$ A equal to B output

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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Fig.3 Logic diagram.

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FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A > B}	I _{A < B}	I _{A = B}	O _{A > B}	O _{A < B}	O _{A = B}
A ₃ > B ₃	X	X	X	H	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	H	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	H	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	H	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	L	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	H	H	L	H	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	L	L	L

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a serial expansion scheme.

The lower 2 lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $A_n, B_n \rightarrow O_n$ HIGH to LOW LOW to HIGH $I_n \rightarrow O_n$ HIGH to LOW LOW to HIGH	5	t_{PHL}		160	320 ns	133 ns + (0,55 ns/pF) C_L
	10			65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5	t_{PLH}		150	300 ns	123 ns + (0,55 ns/pF) C_L
	10			60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5	t_{PHL}		110	220 ns	83 ns + (0,55 ns/pF) C_L
	10			45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}		120	240 ns	93 ns + (0,55 ns/pF) C_L
	10			50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW LOW to HIGH	5	t_{THL}		60	120 ns	10 ns + (1,0 ns/pF) C_L
	10			30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C_L
	10			30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1250 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$15\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

APPLICATION INFORMATION

Some examples of applications for the HEF4585B are:

- Process controllers.
- Servo-motor control.

4-bit magnitude comparator

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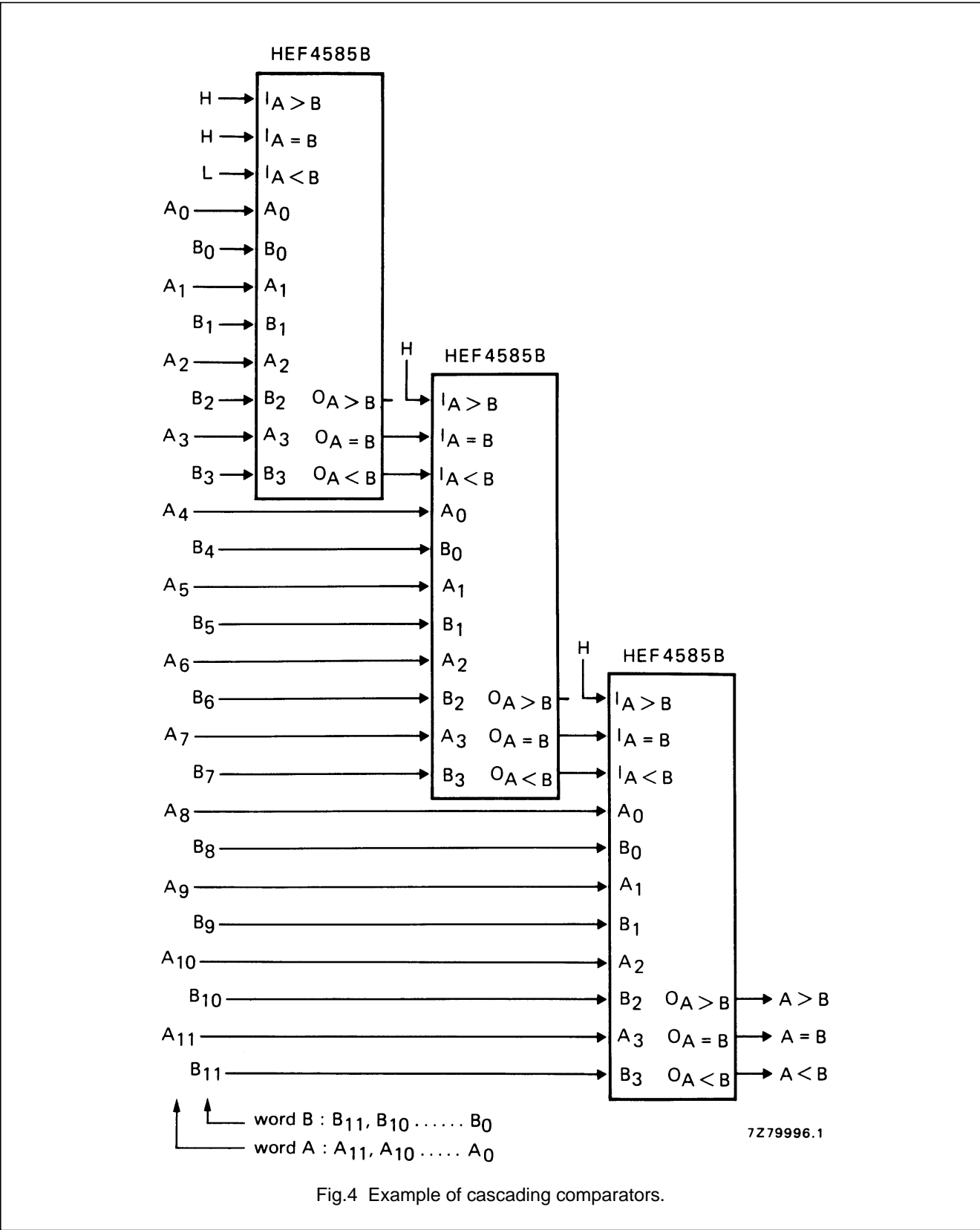


Fig.4 Example of cascading comparators.