DATA SHEET

74LVT16245B
3.3 V LVT 16-bit transceiver (3-State)

Product data
Supersedes data of 1998 Feb 19

2002 Oct 31

Philips
Semiconductors

3.3 V LVT 16-bit transceiver (3-State) 74LVT16245B

FEATURES

- 16-bit bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA / –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74LVT16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

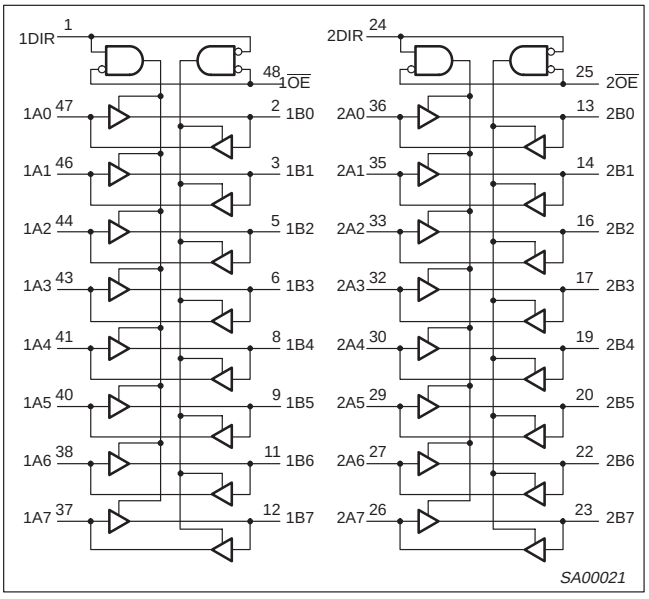
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF; V_{CC} = 3.3 V	1.9	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0 V or 3.0 V	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O}$ = 0 V or 3.0 V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6 V	70	µA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	TEMPERATURE RANGE	DWG NUMBER
74LVT16245BDL	48-Pin Plastic SSOP Type III	–40 °C to +85 °C	SOT370-1
74LVT16245BDGG	48-Pin Plastic TSSOP Type II	–40 °C to +85 °C	SOT362-1
74LVT16245BEV	56VFBGA Ball Grid Array	–40 °C to +85 °C	SOT702-1

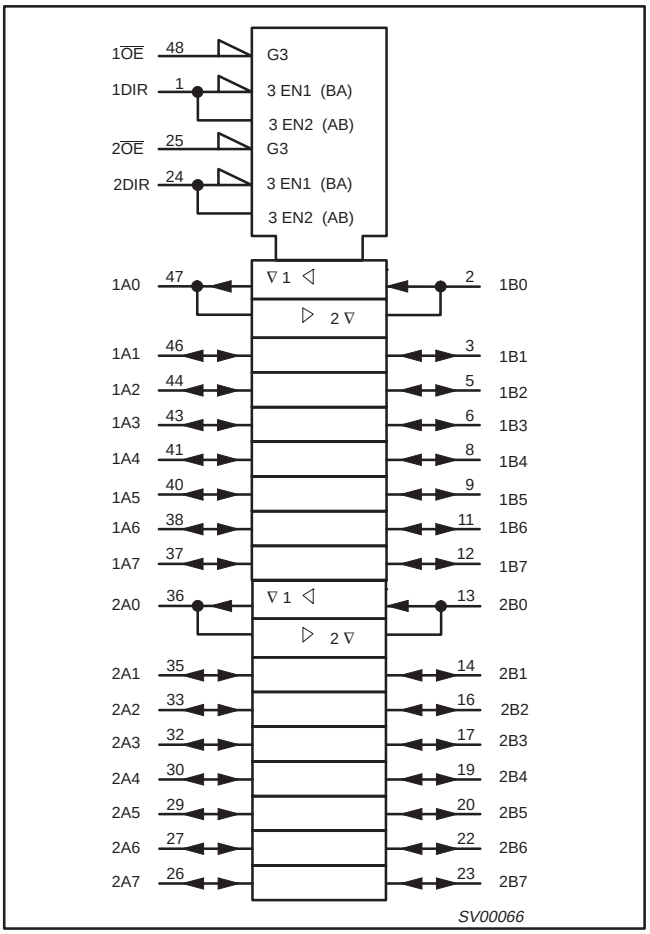
LOGIC SYMBOL



NOTE:
Pin numbers are shown for SSOP and TSSOP packages only.

3.3 V LVT 16-bit transceiver (3-State) 74LVT16245B

LOGIC SYMBOL (IEEE/IEC)



NOTE:
Pin numbers are shown for SSOP and TSSOP packages only.

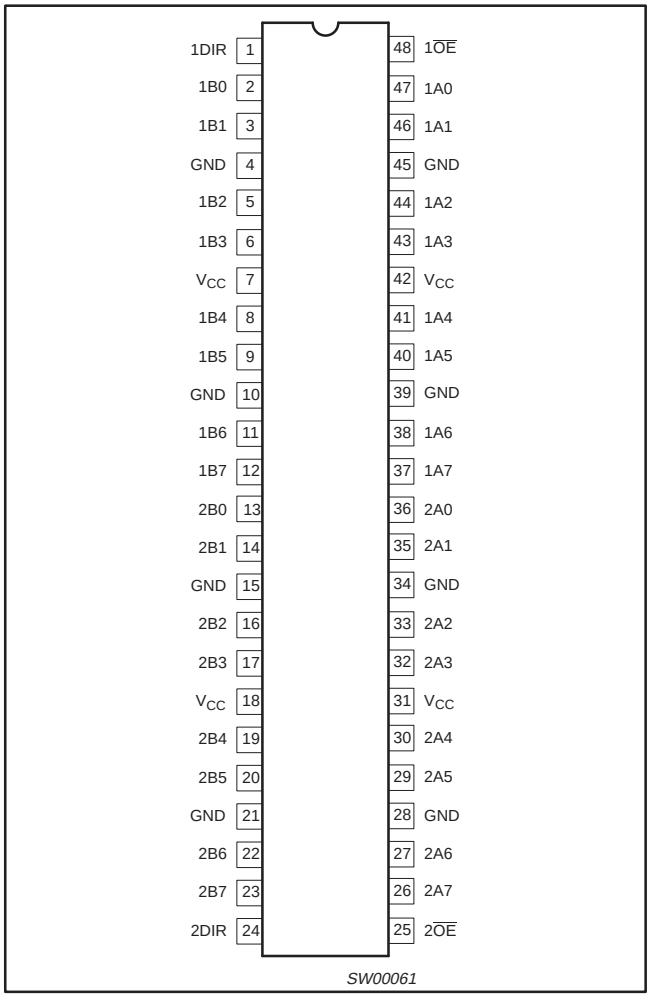
FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
n$\overline{OE}$	**nDIR**	**nAx**	**nBx**
L	L	nAx = nBx	Inputs
L	H	Inputs	nBx = nAx
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance "off" state

PIN CONFIGURATION

48-pin SSOP and TSSOP



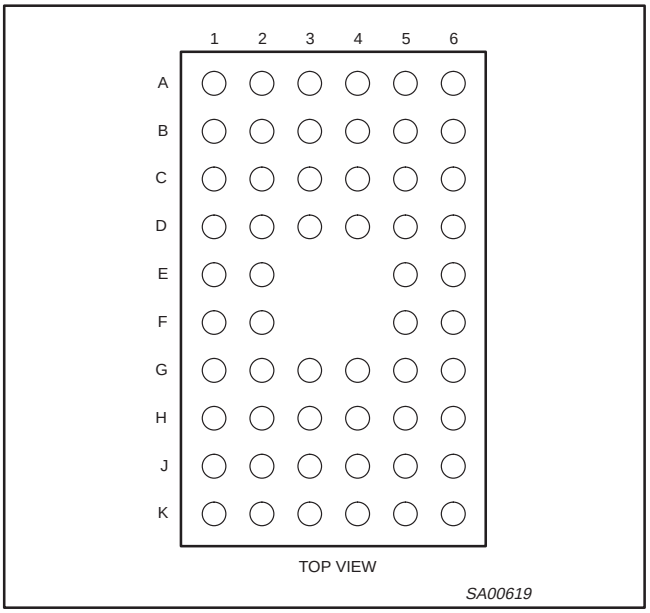
PIN DESCRIPTION

48-pin SSOP and TSSOP

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 24	nDIR	Direction control input
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	nA0 – nA7	Data inputs/outputs (A side)
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	nB0 – nB7	Data inputs/outputs (B side)
25, 48	n$\overline{OE}$	Output enable input (active-Low)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

PIN CONFIGURATION

56-ball VFBGA terminal assignments



PIN DESCRIPTION

56-ball VFBGA terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1B1	1B0	GND	GND	1A0	1A1
C	1B3	1B2	V_{CC}	V_{CC}	1A2	1A3
D	1B5	1B4	GND	GND	1A4	1A5
E	1B7	1B6			1A6	1A7
F	2B0	2B1			2A1	2A0
G	2B2	2B3	GND	GND	2A3	2A2
H	2B4	2B5	V_{CC}	V_{CC}	2A5	2A4
J	2B6	2B7	GND	GND	2A7	2A6
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

ABSOLUTE MAXIMUM RATINGS[1,2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in OFF or HIGH state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in LOW state	128	mA
		Output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	HIGH-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	HIGH-level output current		–32	mA
I_{OL}	LOW-level output current		32	mA
	LOW-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = –40 °C to +85 °C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA			–0.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = –100 µA		V_{CC}–0.2	V_{CC}		V
		V_{CC} = 2.7 V; I_{OH} = –8 mA		2.4	2.5		
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA			0.07	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA			0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 16 mA			0.25	0.4	
		V_{CC} = 3.0 V; I_{OL} = 32 mA			0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 64 mA			0.4	0.55	
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V			0.1	10	
		V_{CC} = 3.6 V; V_I = 5.5 V	I/O Data pins[4]		0.1	20	
		V_{CC} = 3.6 V; V_I = V_{CC}			0.5	10	
		V_{CC} = 3.6 V; V_I = 0			0.1	–5	
I_{OFF}	Output off current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V			0.1	±100	µA
I_{HOLD}	Bus Hold current A or B outputs[6]	V_{CC} = 3 V; V_I = 0.8 V		75	135		µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–135		
		V_{CC} = 0 V to 3.6 V; V_{CC} = 3.6 V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5 V; V_{CC} = 3.0 V			75	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			40	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6 V; Outputs HIGH, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6 V; Outputs LOW, V_I = GND or V_{CC}, I_O = 0			4.7	6	
I_{CCZ}		V_{CC} = 3.6 V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[5]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; One input at V_{CC}–0.6 V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
6. This is the bus-hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

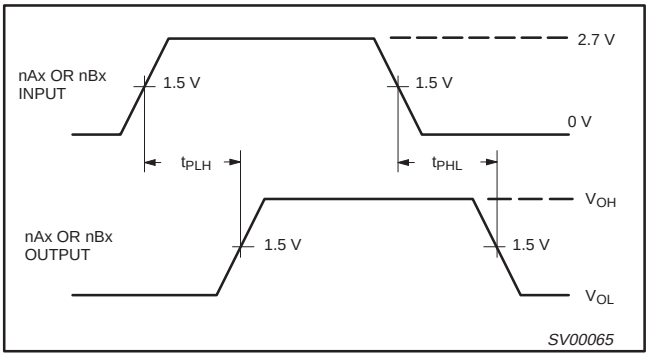
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3 V +0.3 V			V_{CC} = 2.7 V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx or nBx to nAx	1	1.0 1.0	1.9 1.7	3.3 3.3	3.5 3.5	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	2	1.0 1.0	2.8 2.8	4.5 4.1	5.3 5.1	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW Level	2	1.5 1.5	3.2 3.0	5.1 4.6	5.7 4.6	ns

NOTE:

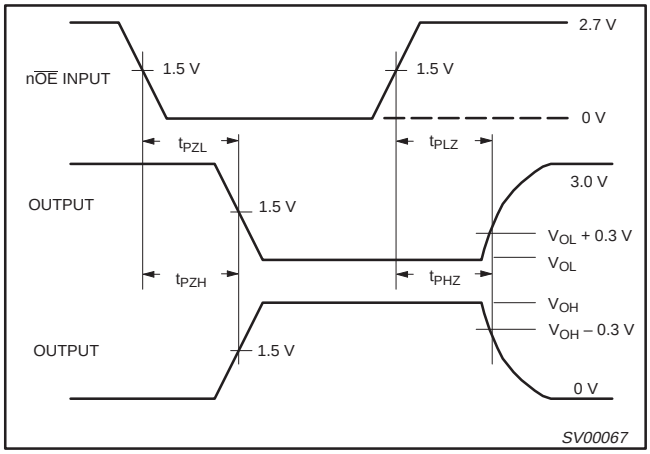
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC WAVEFORMS

V_M = 1.5 V; V_{IN} = GND to 2.7 V.

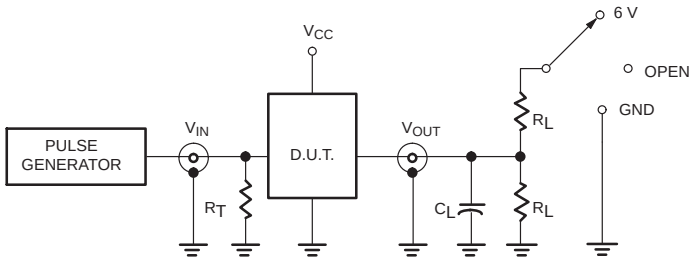


Waveform 1. Input to Output Propagation Delays

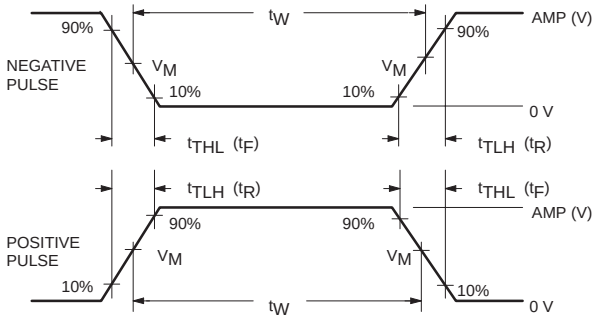


Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6 V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

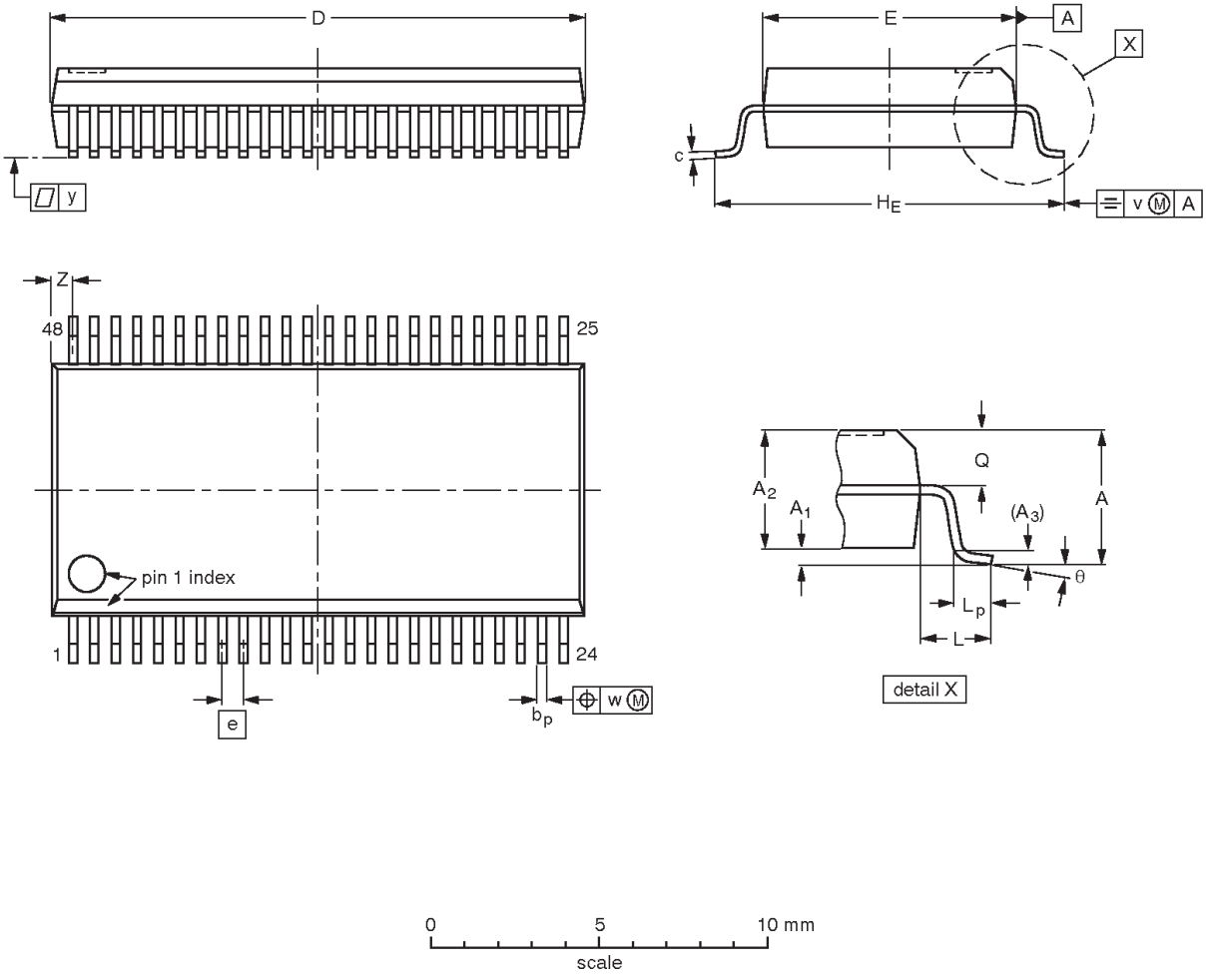
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7 V	≤10 MHz	500 ns	≤2.5 ns	≤2.5 ns

SW00003

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

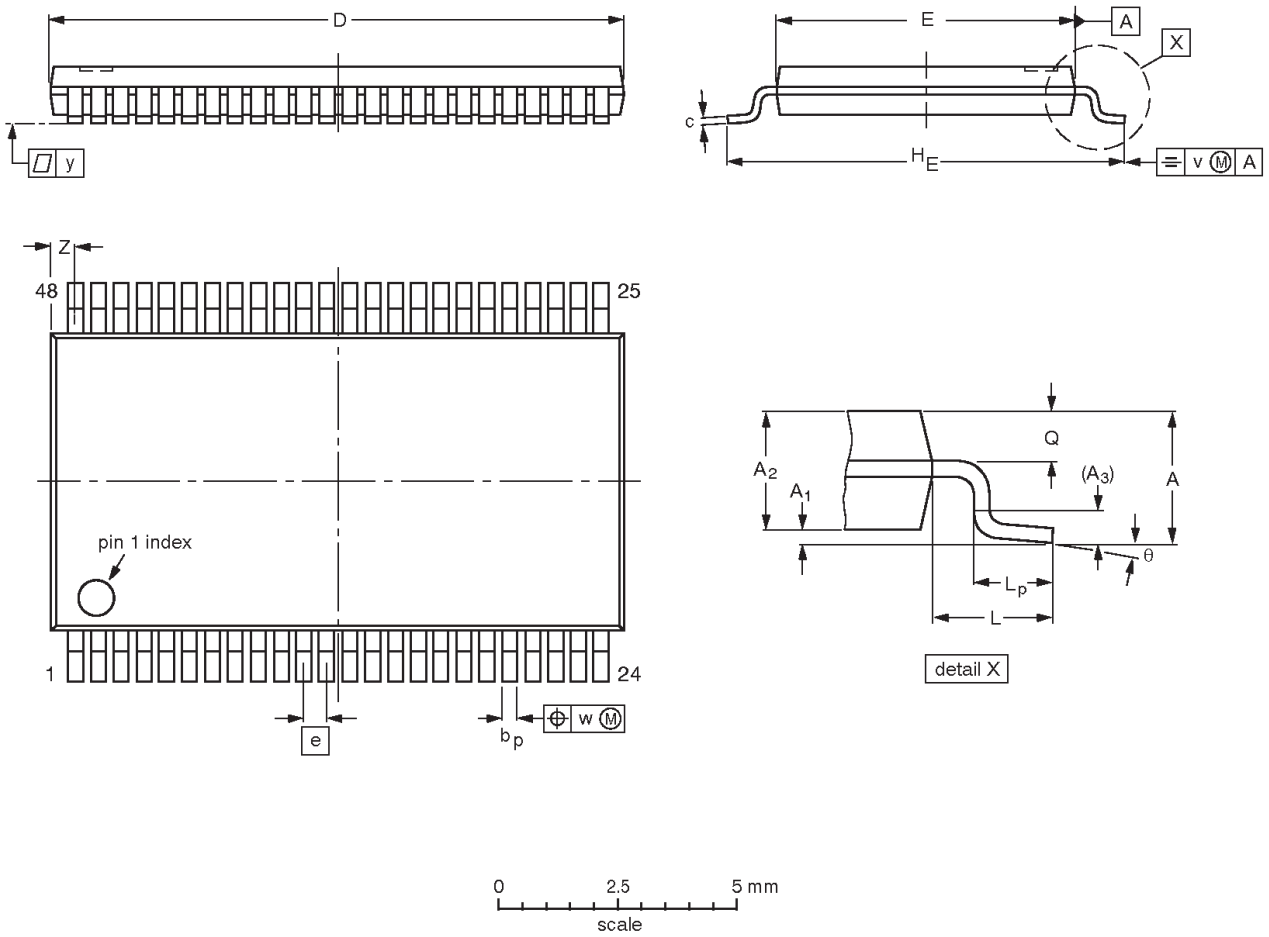
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118				~~95-02-04~~ 99-12-27

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

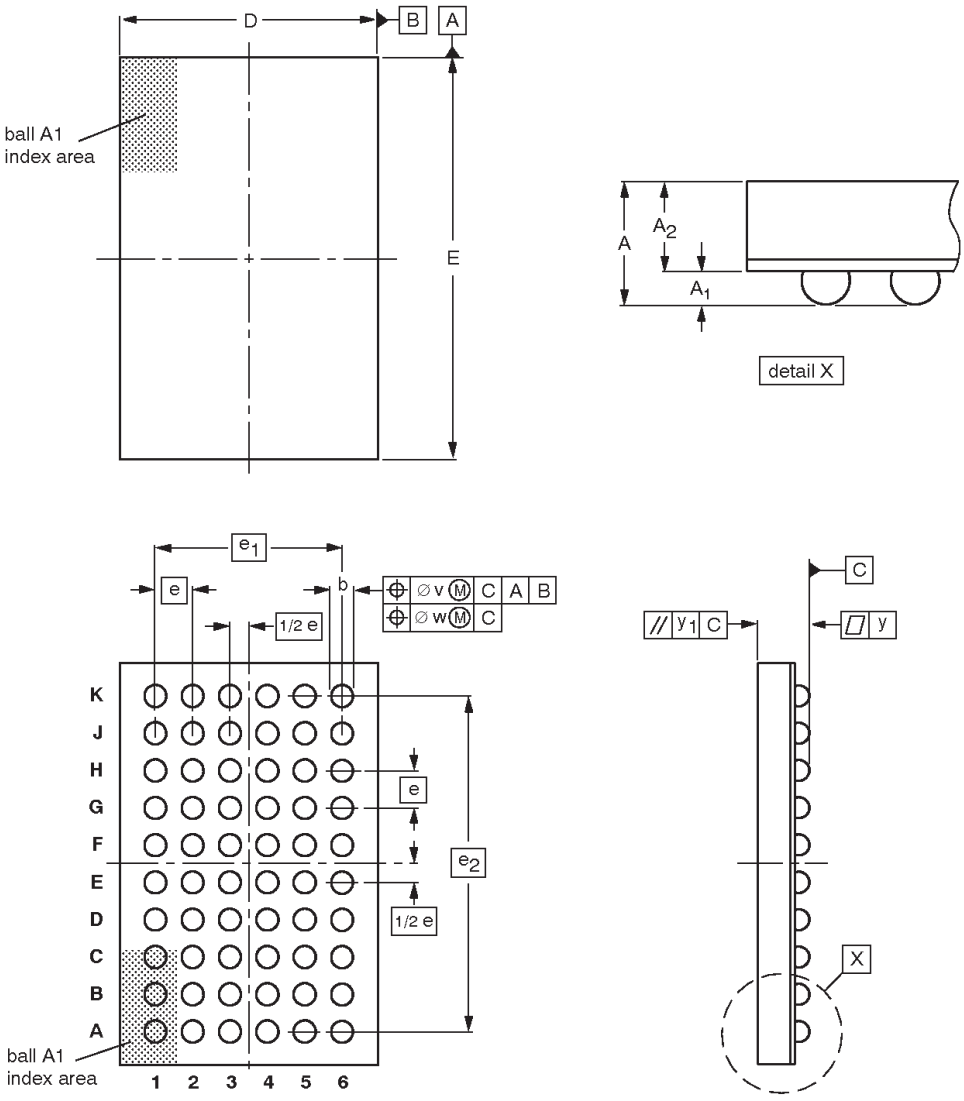
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1

0 2.5 5 mm
scale

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~01-06-25~~ 02-08-08

REVISION HISTORY

Rev	Date	Description
_3	20021031	**Product data (9397 750 09135); supersedes 74LVT16245B_2 of 1998 Feb 19 (9397 750 03552).** Engineering Change Notice 853–1753 27400 (date: 20011203). Modifications: • Add VFBGA56 (EV) package option.

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Contact information

For additional information please visit
http://www.semiconductors.philips.com. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com.

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