

DATA SHEET

74LVC16241A 16-bit buffer/line driver (3-State)

Product specification
Supersedes data of 1995 Dec 26
IC24 Data Handbook

1997 Jul 29

16-bit buffer/line driver (3-State)

74LVC16241A

FEATURES

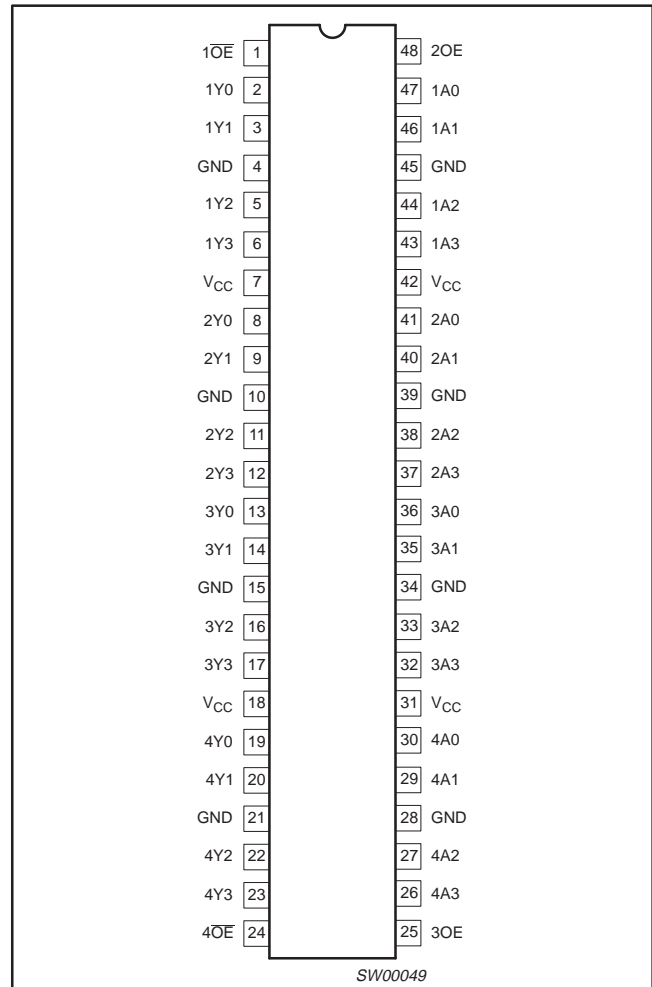
- 5 volt tolerant inputs/outputs for interfacing with 5V logic
- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels

DESCRIPTION

The 74LVC16241A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families. Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. These features allow the use of these devices in a mixed 3.3V/5V environment.

The 74LVC16241A is a 16-bit buffer/line driver with 3-State outputs. The 3-State outputs are controlled by the output enable inputs \overline{nOE} and \overline{nOE} . Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer.

PIN CONFIGURATION



QUICK REFERENCE DATA

$V_{DD} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f \leq 2.5\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|--|---|---------|------|
| t_{PHL}/t_{PLH} | Propagation delay nAn to nYn | $C_L = 50\text{ pF}$ $V_{CC} = 3.3\text{ V}$ | 2.9 | ns |
| C_I | Input capacitance | | 5.0 | pF |
| C_{PD} | Power dissipation capacitance per buffer | $V_I = \text{GND to } V_{CC}^1$ | 25 | pF |

NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|-------------------|-----------------------|---------------|------------|
| 48-Pin Plastic SSOP Type III | -40°C to +85°C | 74LVC16241A DL | VC16241A DL | SOT370-1 |
| 48-Pin Plastic TSSOP Type II | -40°C to +85°C | 74LVC16241A DGG | VC16241A DGG | SOT362-1 |

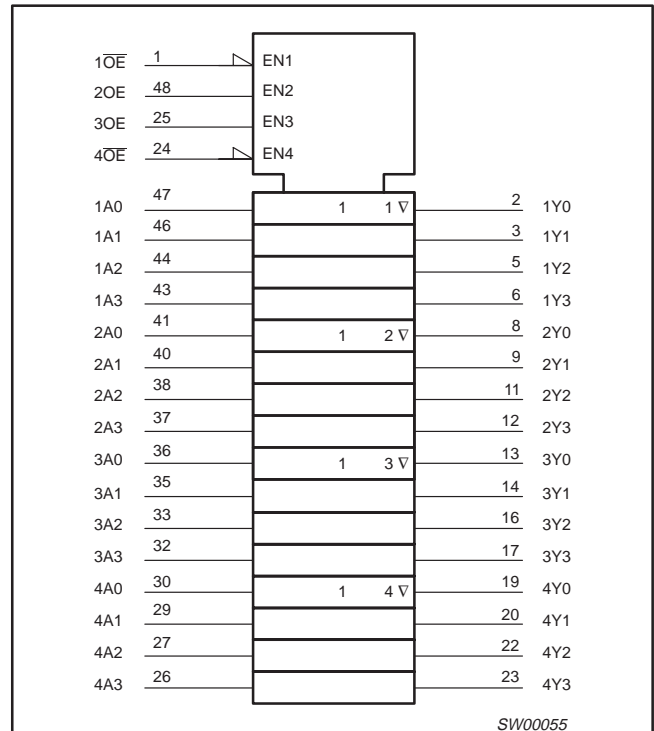
16-bit buffer/line driver (3-State)

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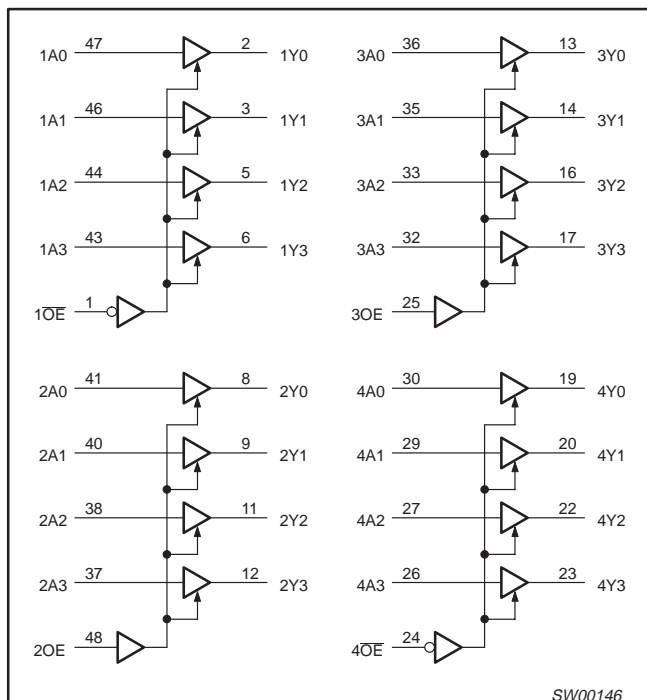
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|-------------------------------|-----------------|----------------------------------|
| 1 | 1OE | Output enable input (active LOW) |
| 2, 3, 5, 6 | 1Y0 to 1Y3 | Data outputs |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | Ground (0V) |
| 7, 18, 31, 42 | V _{CC} | Positive supply voltage |
| 8, 9, 11, 12 | 2Y0 to 2Y3 | Data outputs |
| 13, 14, 16, 17 | 3Y0 to 3Y3 | Data outputs |
| 19, 20, 22, 23 | 4Y0 to 4Y3 | Data outputs |
| 24 | 4OE | Output enable input (active LOW) |
| 25 | 3OE | Output enable input (active LOW) |
| 30, 29, 27, 26 | 4A0 to 4A3 | Data inputs |
| 36, 35, 33, 32 | 3A0 to 3A3 | Data inputs |
| 41, 40, 38, 37 | 2A0 to 2A3 | Data inputs |
| 47, 46, 44, 43 | 1A0 to 1A3 | Data inputs |
| 48 | 2OE | Output enable input (active LOW) |

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLES

| INPUTS | | OUTPUT |
|--------|----------|----------|
| nOE | 1An, 4An | 1Yn, 4Yn |
| L | H | H |
| L | L | L |
| H | X | Z |

| INPUTS | | OUTPUT |
|--------|----------|----------|
| nOE | 2An, 3An | 2Yn, 3Yn |
| H | H | H |
| H | L | L |
| L | X | Z |

H = HIGH voltage level
 L = LOW voltage level
 X = don't care
 Z = high impedance OFF-state

16-bit buffer/line driver (3-State)

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|------------|---|--|--------|----------|------|
| | | | MIN. | MAX. | |
| V_{CC} | DC supply voltage (for max. speed performance) | | 2.7 | 3.6 | V |
| V_{CC} | DC supply voltage (for low-voltage applications) | | 1.2 | 3.6 | V |
| V_I | DC Input voltage range | | 0 | 5.5 | V |
| V_O | DC output voltage range; output HIGH or LOW state | | 0 | V_{CC} | V |
| V_O | DC output voltage range; output 3-State | | 0 | 5.5 | V |
| T_{amb} | Operating ambient temperature range in free air | See DC and AC characteristics for individual device | -40 | +85 | °C |
| t_r, t_f | Input rise and fall times | $V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$ | 0 0 | 20 10 | ns/V |

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|-------------------|---|--|--------|----------------|------|
| | | | MIN | MAX | |
| V_{CC} | DC supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | DC input diode current | $V_I < 0$ | - | -50 | mA |
| V_I | DC input voltage | Note 2 | -0.5 | +6.5 | V |
| I_{OK} | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | - | ±50 | mA |
| V_O | DC output voltage; output HIGH or LOW state | Note 2 | -0.5 | $V_{CC} + 0.5$ | V |
| V_O | DC output voltage; output 3-State | Note 2 | -0.5 | 6.5 | V |
| I_O | DC output source or sink current | $V_O = 0$ to V_{CC} | - | ±50 | mA |
| I_{GND}, I_{CC} | DC V_{CC} or GND current | | - | ±100 | mA |
| T_{stg} | Storage temperature range | | -65 | +150 | °C |
| P_{tot} | Power dissipation per package – SO package – SSOP and TSSOP package | Above +70°C derate linearly 8mW/K Above +60°C derate linearly 5.5mW/K | | 500 500 | mW |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

16-bit buffer/line driver (3-State)

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|------------------|---|--|-----------------------|------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IH} | HIGH level Input voltage | V _{CC} = 1.2V | V _{CC} | | | V |
| | | V _{CC} = 2.7 to 3.6V | 2.0 | | | |
| V _{IL} | LOW level Input voltage | V _{CC} = 1.2V | | | GND | V |
| | | V _{CC} = 2.7 to 3.6V | | | 0.8 | |
| V _{OH} | HIGH level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA | V _{CC} - 0.5 | | | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100µA | V _{CC} - 0.2 | V _{CC} | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA | V _{CC} - 0.6 | | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA | V _{CC} - 0.8 | | | |
| V _{OL} | LOW level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA | | | 0.40 | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA | | GND | 0.20 | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA | | | 0.55 | |
| I _I | Input leakage current | V _{CC} = 3.6V; V _I = 5.5V or GND | | ±0.1 | ±5 | µA |
| I _{OZ} | 3-State output OFF-state current | V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND | | 0.1 | ±5 | µA |
| I _{off} | Power off leakage supply | V _{CC} = 0.0V; V _I or V _O = 5.5V | | 0.1 | ±10 | µA |
| I _{CC} | Quiescent supply current | V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0 | | 0.1 | 20 | µA |
| ΔI _{CC} | Additional quiescent supply current per input pin | V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0 | | 5 | 500 | µA |

NOTE:1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.**AC CHARACTERISTICS**GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT | |
|--------------------------------------|---|----------|------------------------------|------------------|-----|------------------------|-----|------|------------------------|
| | | | V _{CC} = 3.3V ±0.3V | | | V _{CC} = 2.7V | | | V _{CC} = 1.2V |
| | | | MIN | TYP ¹ | MAX | MIN | MAX | | TYP |
| t _{PHL} t _{PLH} | Propagation delay nAn to nYn; nAn to nYn | 1, 4 | 1.5 | 2.9 | 4.4 | 1.5 | 5.4 | 13 | ns |
| t _{PZH} t _{PZL} | 3-State output enable time 1OE to 1Yn; 4OE to 4Yn | 3, 4 | 1.5 | 4.4 | 5.8 | 1.5 | 6.8 | 17 | ns |
| t _{PHZ} t _{PLZ} | 3-State output disable time 1OE to 1Yn; 4OE to 4Yn | 3, 4 | 1.5 | 4.3 | 5.8 | 1.5 | 6.8 | 11 | ns |
| t _{PZH} t _{PZL} | 3-State output enable time 2OE to 2Yn; 3OE to 3Yn | 2, 4 | 1.5 | 4.4 | 5.5 | 1.5 | 6.5 | 19 | ns |
| t _{PHZ} t _{PLZ} | 3-State output disable time 2OE to 2Yn; 3OE to 3Yn | 2, 4 | 1.5 | 4.9 | 5.4 | 1.5 | 6.4 | 12 | ns |

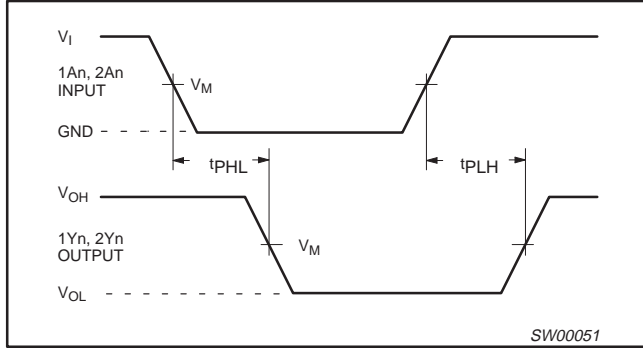
NOTE:1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

16-bit buffer/line driver (3-State)

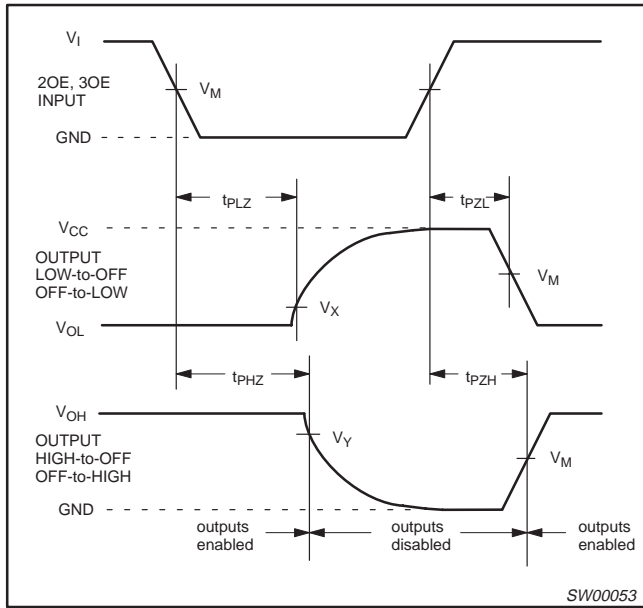
74LVC16241A

AC WAVEFORMS

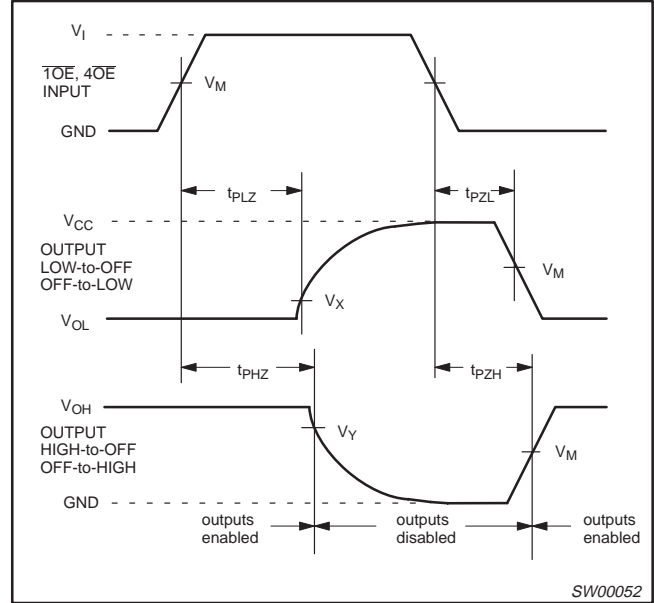
$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$



Waveform 1. Input (nAn) to output (nYn) propagation times

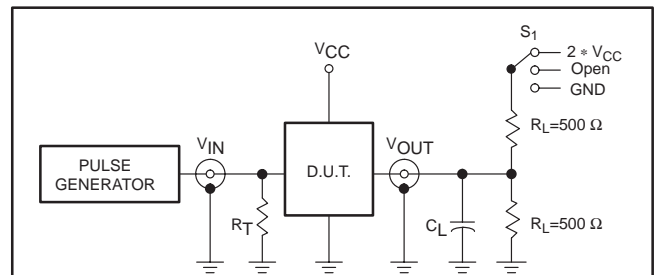


Waveform 2. 3-State enable and disable times for the input (2OE, 3OE)



Waveform 3. 3-State enable and disable times for the input (1OE, 4OE)

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

| TEST | SWITCH |
|-------------------|--------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 * V_{CC}$ |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | V_{IN} |
|--------------|----------|
| $< 2.7V$ | V_{CC} |
| $2.7 - 3.6V$ | $2.7V$ |

DEFINITIONS

R_L = Load resistor
 C_L = Load capacitance includes jig and probe capacitance
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

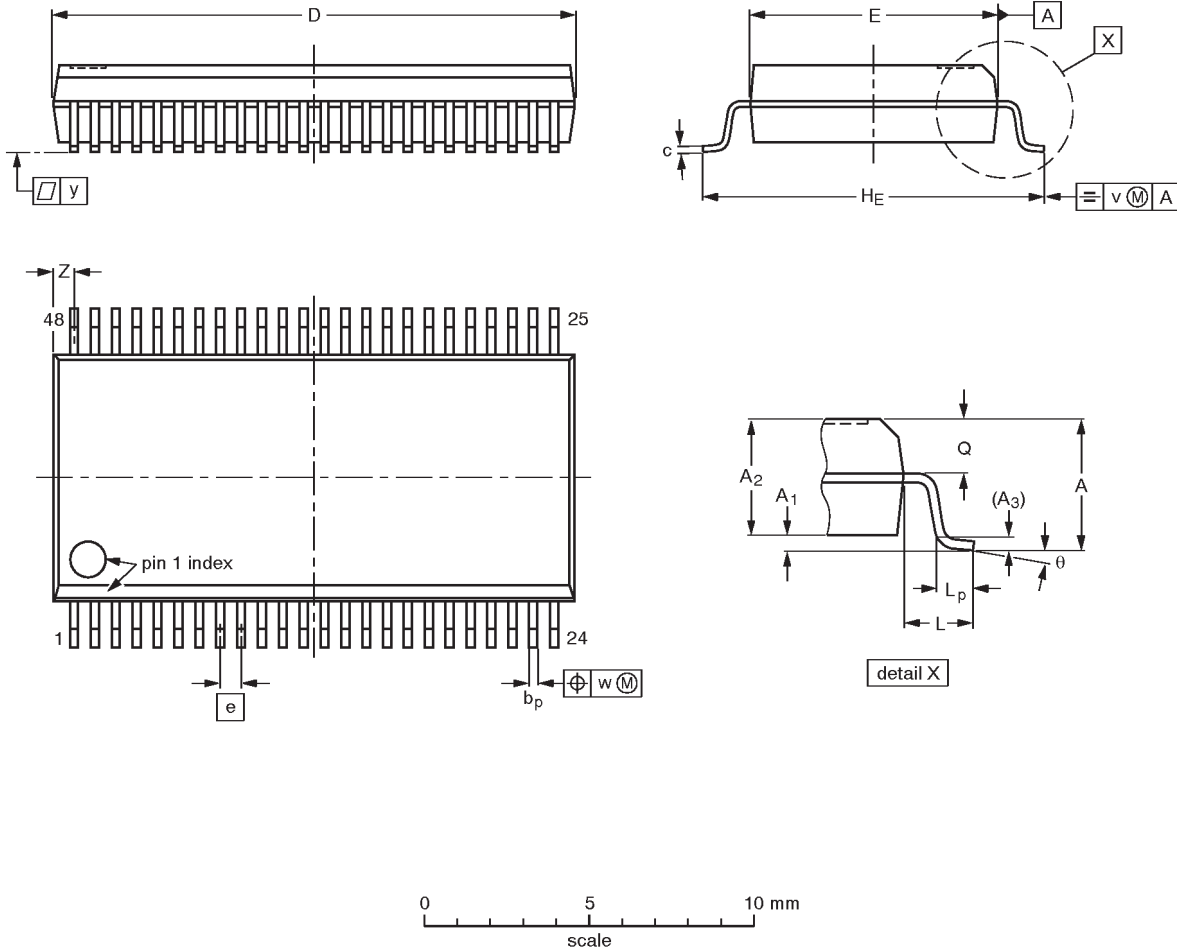
Waveform 4. Load circuitry for switching times

16-bit buffer/line driver (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|-------|----------------|-----|----------------|------------|------|------|-----|------------------|----------|
| mm | 2.8 | 0.4 0.2 | 2.35 2.20 | 0.25 | 0.3 0.2 | 0.22 0.13 | 16.00 15.75 | 7.6 7.4 | 0.635 | 10.4 10.1 | 1.4 | 1.0 0.6 | 1.2 1.0 | 0.25 | 0.18 | 0.1 | 0.85 0.40 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

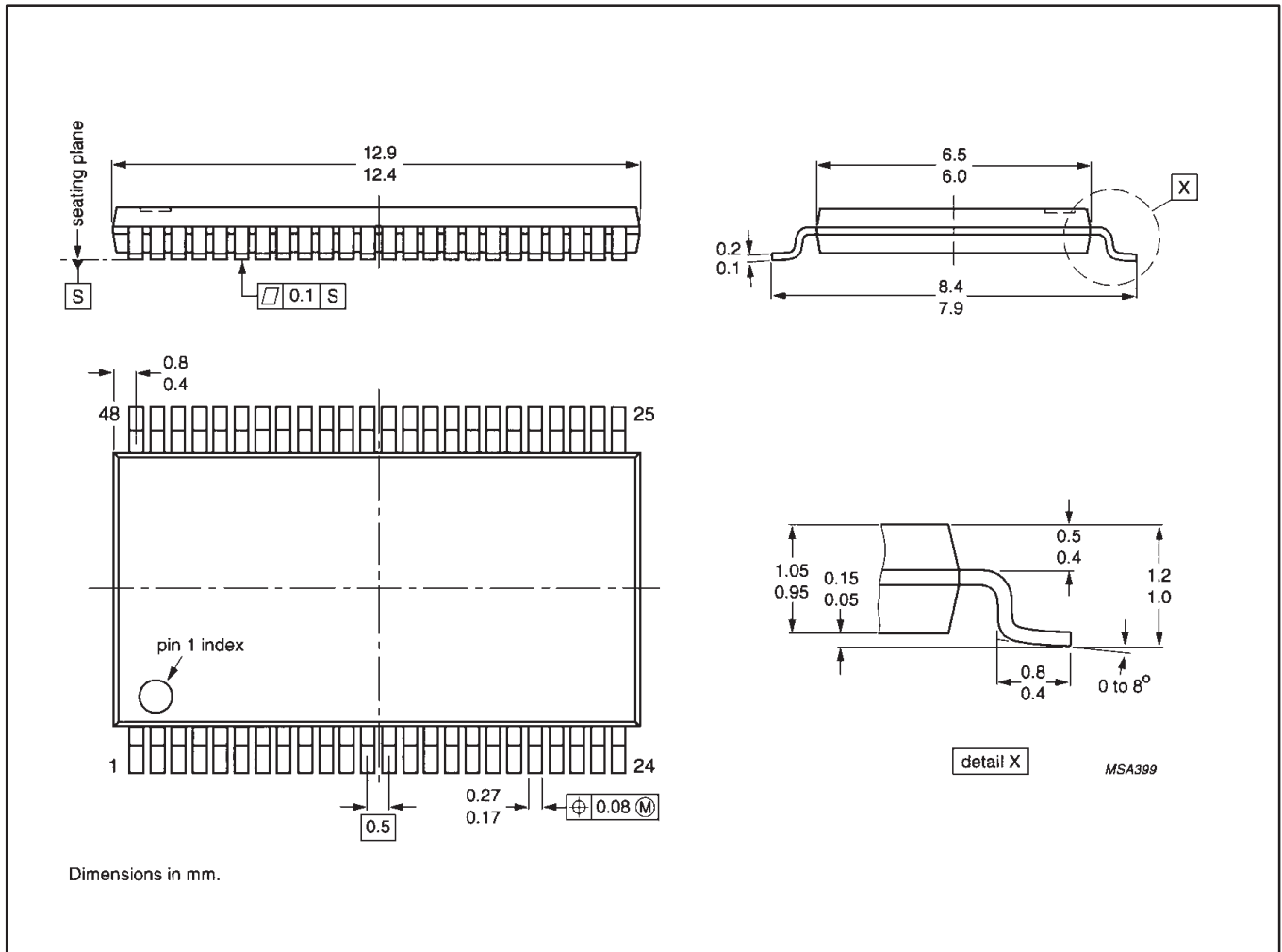
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT370-1 | | MO-118AA | | | | 93-11-02- 95-02-04 |

16-bit buffer/line driver (3-State)

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



16-bit buffer/line driver (3-State)

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NOTES

16-bit buffer/line driver (3-State)

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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