



28LV64A

64K (8K x 8) Low Voltage CMOS EEPROM

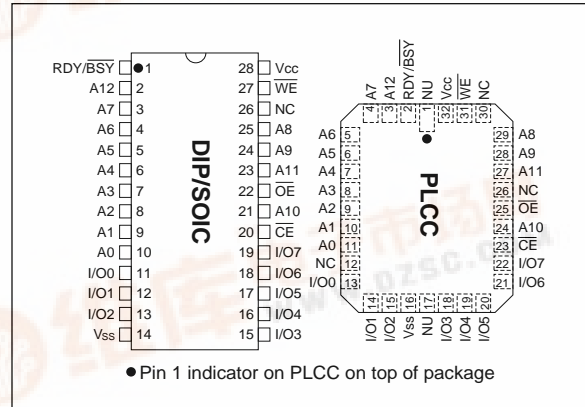
FEATURES

- 2.7V to 3.6V Supply
- Read Access Time—300 ns
- CMOS Technology for Low Power Dissipation
 - 8 mA Active
 - 50 μ A CMOS Standby Current
- Byte Write Time—3 ms
- Data Retention >200 years
- High Endurance - Minimum 100,000 Erase/Write Cycles
- Automatic Write Operation
 - Internal Control Timer
 - Auto-Clear Before Write Operation
 - On-Chip Address and Data Latches
- Data Polling
- Ready/Busy
- Chip Clear Operation
- Enhanced Data Protection
 - Vcc Detector
 - Pulse Filter
 - Write Inhibit
- Electronic Signature for Device Identification
- Organized 8Kx8 JEDEC Standard Pinout
 - 28-pin Dual-In-Line Package
 - 32-pin Chip Carrier (Leadless or Plastic)
- Available for Extended Temperature Ranges:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C

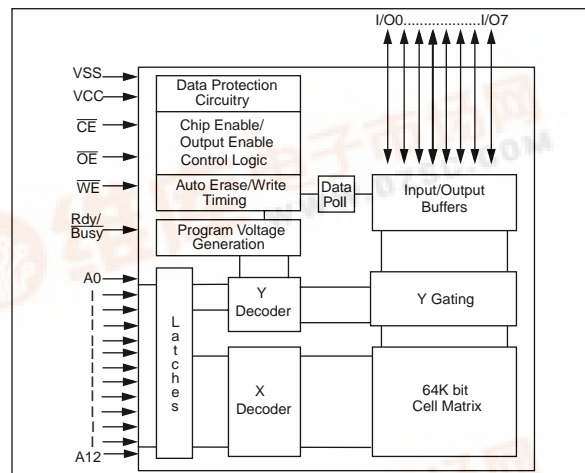
DESCRIPTION

The Microchip Technology Inc. 28LV64A is a CMOS 64K non-volatile electrically Erasable PROM organized as 8K words by 8 bits. The 28LV64A is accessed like a static RAM for the read or write cycles without the need of external components. During a "byte write", the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. To determine when the write cycle is complete, the user has a choice of monitoring the Ready/Busy output or using Data polling. The Ready/Busy pin is an open drain output, which allows easy configuration in 'wired-or' systems. Alternatively, Data polling allows the user to read the location last written to when the write operation is complete. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are required. A complete family of packages is offered to provide the utmost flexibility in applications.

PACKAGE TYPES



BLOCK DIAGRAM



VCC = 2.7 to 3.6V Commercial (C): Tamb = 0°C to 70°C Industrial (I): Tamb = -40°C to 85°C						
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "2"	V _{IH} V _{IL}	2.0	0.6	V V	
Input Leakage	—	I _{LI}	—	5	μA	V _{IN} = 0V to V _{CC} +1
Input Capacitance	—	C _{IN}	—	6	pF	V _{in} = 0V; Tamb = 25°C; f = 1 MHz (Note 1)
Output Voltages	Logic "1" Logic "0"	V _{OH} V _{OL}	2.0	0.3	V V	I _{OH} = -100μA I _{OL} = 1.0 mA I _{OL} = 2.0 mA for RDY/Busy
Output Leakage	—	I _{LO}	—	5	μA	V _{OUT} = 0V to V _{CC} +0.1V
Output Capacitance	—	C _{OUT}	—	12	pF	V _{OUT} = 0V; Tamb = 25°C; f = 1 MHz (Note 1)
Power Supply Current, Activity	TTL input	I _{CC}	—	8	mA	f = 5 MHz (Note 2) I _o = 0mA V _{CC} = 3.3 CE = V _{IL}
Power Supply Current, Standby	TTL input TTL input CMOS input	I _{CC} (s) _{TTL} I _{CC} (s) _{TTL} I _{CC} (s) _{CMOS}	—	2 3 100	mA mA μA	CE = V _{IH} (0°C to 70°C°) CE = V _{IH} (-40°C to 85°C°) CE = V _{CC} -3.0 to V _{CC} +1 OE = WE = V _{CC} All other inputs equal V _{CC} or V _{SS}

Note 1: Not 100% tested.
2: AC power supply current above 5 MHz: 2 mA/Mhz.

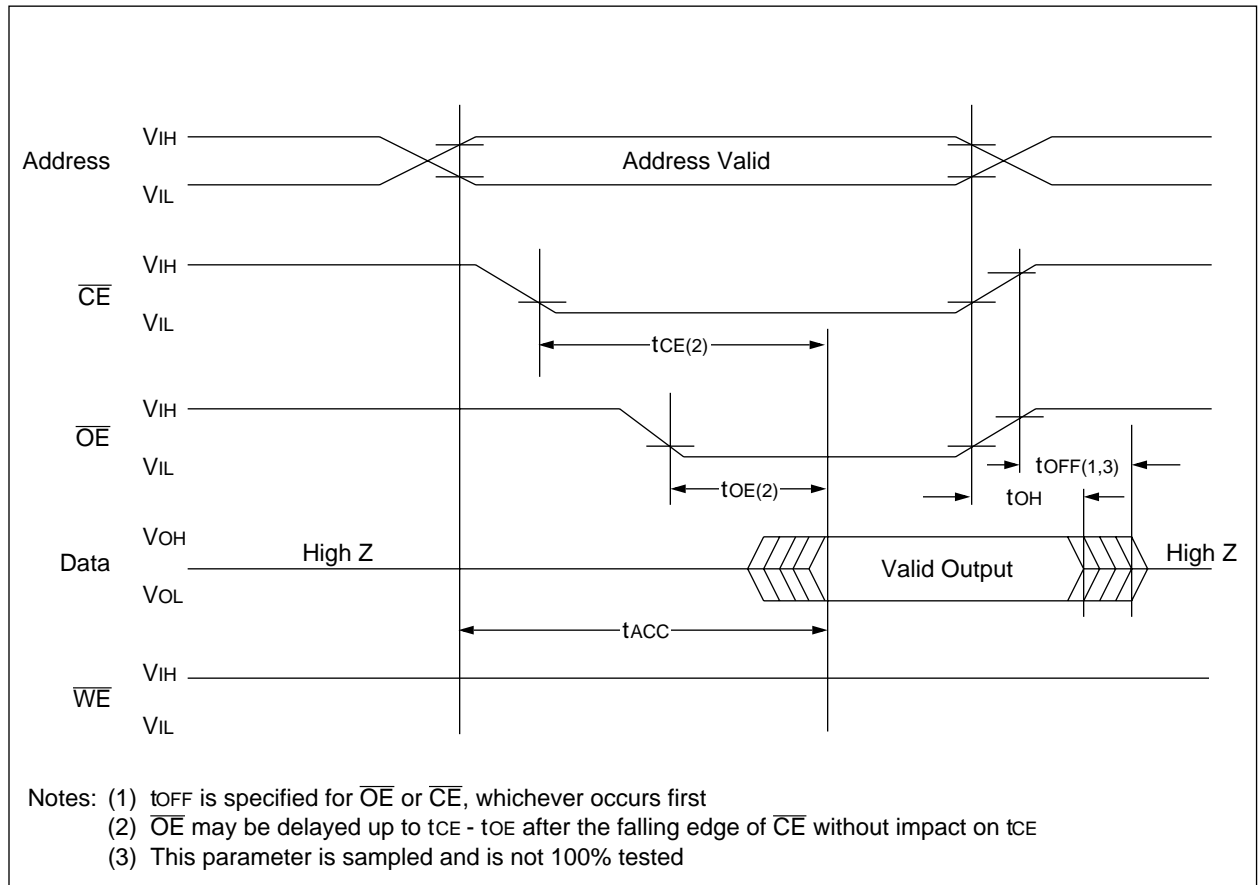
TABLE 1-3: READ OPERATION AC CHARACTERISTICS

		AC Testing Waveform:		$V_{IH} = 2.0V$; $V_{IL} = 0.6V$; $V_{OH} = V_{OL} = V_{CC}/2$	
		Output Load:		1 TTL Load + 100 pF	
		Input Rise and Fall Times:		20 ns	
		Ambient Temperature:		Commercial (C): $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial (I) : $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$	
Parameter	Sym	28LV64-30		Units	Conditions
		Min	Max		
Address to Output Delay	t_{ACC}	—	300	ns	$\overline{OE} = \overline{CE} = V_{IL}$
\overline{CE} to Output Delay	t_{CE}	—	300	ns	$\overline{OE} = V_{IL}$
\overline{OE} to Output Delay	t_{OE}	—	150	ns	$\overline{CE} = V_{IL}$
\overline{CE} or \overline{OE} High to Output Float	t_{OFF}	0	60	ns	(Note 1)
Output Hold from Address, \overline{CE} or \overline{OE} , whichever occurs first.	t_{OH}	0	—	ns	(Note 1)
Endurance	—	10M	—	cycles	$25^{\circ}C$, $V_{CC} = 5.0V$, Block Mode (Note 2)

Note 1: Not 100% tested.

2: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: READ WAVEFORMS



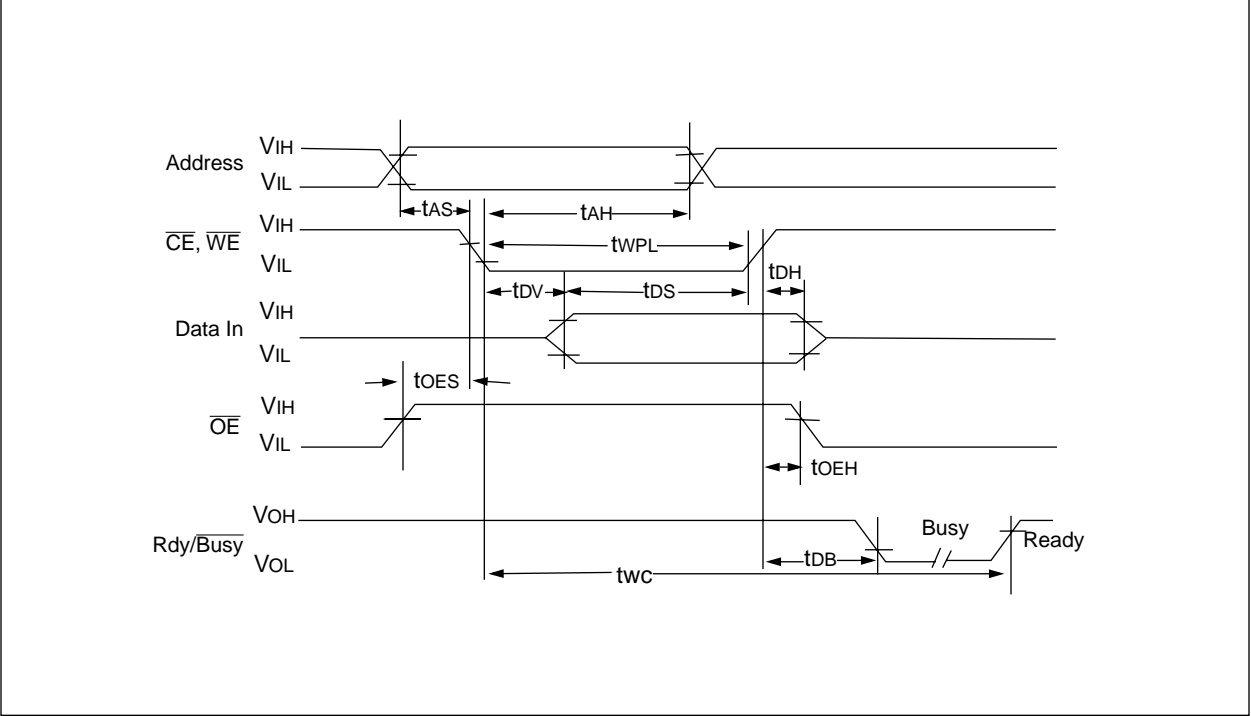
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TABLE 1-4: BYTE WRITE AC CHARACTERISTICS

		AC Testing Waveform: Output Load: Input Rise/Fall Times: Ambient Temperature:		V _{IH} = 2.0V; V _{IL} = 0.6V; V _{OH} = V _{OL} = V _{CC} /2 1 TTL Load + 100 pF 20 ns Commercial (C): T _{amb} = 0°C to +70°C Industrial (I) : T _{amb} = -40°C to +85°C	
Parameter	Sym	Min	Max	Units	Remarks
Address Set-Up Time	t _{AS}	10		ns	
Address Hold Time	t _{AH}	100		ns	
Data Set-Up Time	t _{DS}	120		ns	
Data Hold Time	t _{DH}	10		ns	
Write Pulse Width	t _{WPL}	150		ns	(Note 1)
$\overline{\text{OE}}$ Hold Time	t _{OE H}	10		ns	
$\overline{\text{OE}}$ Set-Up Time	t _{OE S}	10		ns	
Data Valid Time	t _{DV}		1000	ns	(Note 2)
Time to Device Busy	t _{DB}		50	ns	
Write Cycle Time (28LV64A)	t _{WC}		3	ms	1.5 ms typical

- Note 1: A write cycle can be initiated by $\overline{\text{CE}}$ or $\overline{\text{WE}}$ going low, whichever occurs last. The data is latched on the positive edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs first.
- 2: Data must be valid within 1000ns max. after a write cycle is initiated and must be stable at least until t_{DH} after the positive edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurs first.

FIGURE 1-2: PROGRAMMING WAVEFORMS



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2.0 DEVICE OPERATION

The Microchip Technology Inc. 28LV64A has four basic modes of operation—read, standby, write inhibit, and byte write—as outlined in the following table.

Operation Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	Rdy/Busy ⁽¹⁾
Read	L	L	H	DOUT	H
Standby	H	X	X	High Z	H
Write Inhibit	H	X	X	High Z	H
Write Inhibit	X	L	X	High Z	H
Write Inhibit	X	X	H	High Z	H
Byte Write	L	H	L	DIN	L
Byte Clear	Automatic Before Each "Write"				

Note: (1) Open drain output.

2.1 Read Mode

The 28LV64A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the output t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{\text{ACC}}-t_{\text{OE}}$.

2.2 Standby Mode

The 28LV64A is placed in the standby mode by applying a high signal to the $\overline{\text{CE}}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

First, an internal V_{CC} detect (2.0 volts typical) will inhibit the initiation of non-volatile programming operation when V_{CC} is less than the V_{CC} detect circuit trip.

Second, holding $\overline{\text{WE}}$ or $\overline{\text{CE}}$ high or $\overline{\text{OE}}$ low, inhibits a write cycle during power-on and power-off (V_{CC}).

2.4 Write Mode

The 28LV64A has a write cycle similar to that of a static RAM. The write cycle is completely self-timed and initiated by a low going pulse on the $\overline{\text{WE}}$ pin. On the falling edge of $\overline{\text{WE}}$, the address information is latched. On rising edge, the data and the control pins ($\overline{\text{CE}}$ and $\overline{\text{OE}}$) are latched. The Ready/Busy pin goes to a logic low level indicating that the 28LV64A is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/Busy goes back to a high, the 28LV64A has completed writing and is ready to accept another cycle.

2.5 Data Polling

The 28LV64A features $\overline{\text{Data}}$ polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of I/O7 (I/O0 to I/O6 can not be determined). After completion of the write cycle, true data is available. Data polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

2.6 Electronic Signature for Device Identification

An extra row of 32 bytes of EEPROM memory is available to the user for device identification. By raising A9 to 12V ± 0.5 V and using address locations 1FEO to 1FFF, the additional bytes can be written to or read from in the same manner as the regular memory array.

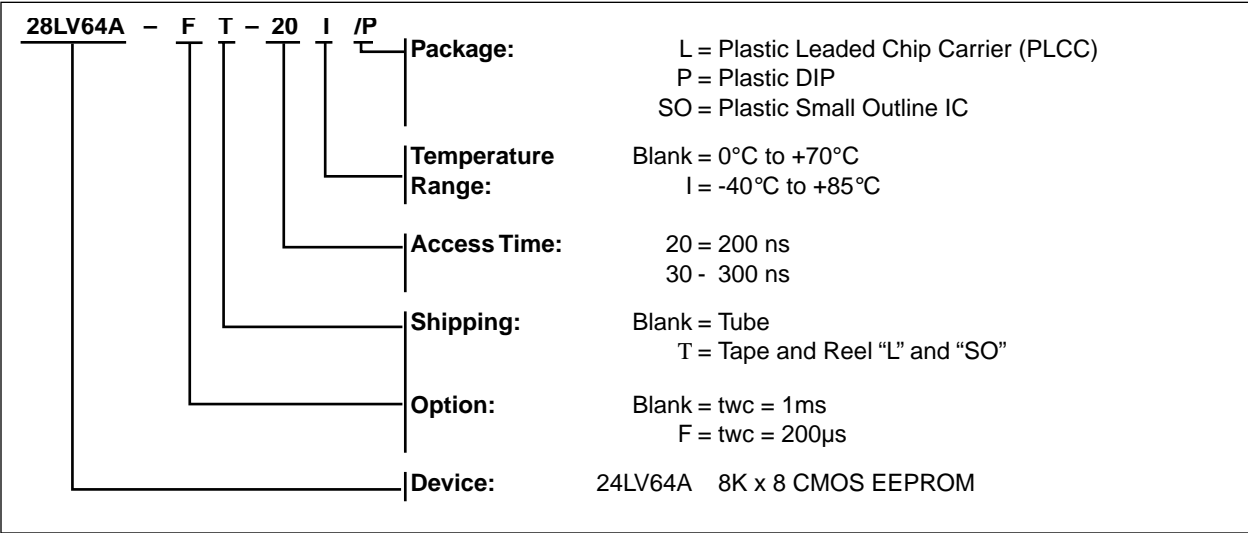
2.7 Chip Clear

All data may be cleared to 1's in a chip clear cycle by raising $\overline{\text{OE}}$ to 12 volts and bringing the $\overline{\text{WE}}$ and $\overline{\text{CE}}$ low. This procedure clears all data, except for the extra row.

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28LV64A Product Identification System

To order or to obtain information (e.g., on pricing or delivery), please use the listed part numbers, and refer to the factory or the listed sales offices.





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Microchip received ISO 9001 Quality System certification for its worldwide headquarters, design, and wafer fabrication facilities in January, 1997. Our field-programmable PICmicro™ 8-bit MCUs, Serial EEPROMs, related specialty memory products and development systems conform to the stringent quality standards of the International Standard Organization (ISO).