

# DATA SHEET

**74LV164**

**8-bit serial-in/parallel-out shift register**

Product specification  
Supersedes data of 1997 Mar 28  
IC24 Data Handbook

1998 May 07

## 8-bit serial-in/parallel-out shift register

74LV164

## FEATURES

- Wide operating voltage: 1.0 to 5.5V
- Optimized for Low Voltage applications: 1.0 to 3.6V
- Accepts TTL input levels between  $V_{CC} = 2.7V$  and  $V_{CC} = 3.6V$
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8V$  @  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2V$  @  $V_{CC} = 3.3V$ ,  $T_{amb} = 25^{\circ}C$
- Gated serial data inputs
- Asynchronous master reset
- Output capability: standard
- $I_{CC}$  category: MSI

## DESCRIPTION

The 74LV164 is a low-voltage Si-gate CMOS device and is pin and function compatible with the 74HC/HCT164.

The 74LV164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs ( $D_{sa}$  or  $D_{sb}$ ); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into  $Q_0$ , which is the logical AND of the two data inputs ( $D_{sa}$ ,  $D_{sb}$ ) that existed one set-up time prior to the rising clock edge.

A LOW on the master reset (MR) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \leq 2.5$  ns

| SYMBOL            | PARAMETER                                       | CONDITIONS                       | TYPICAL  | UNIT |
|-------------------|---|----------------------------------|----------|------|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>CP to $Q_n$<br>MR to $Q_n$ | $C_L = 15pF$<br>$V_{CC} = 3.3V$  | 12<br>12 | ns   |
| $f_{max}$         | Maximum clock frequency                         |                                  | 78       | MHz  |
| $C_I$             | Input capacitance                               |                                  | 3.5      | pF   |
| $C_{PD}$          | Power dissipation capacitance per gate          | $V_{CC} = 3.3V$<br>Notes 1 and 2 | 40       | pF   |

## NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_I = GND$  to  $V_{CC}$

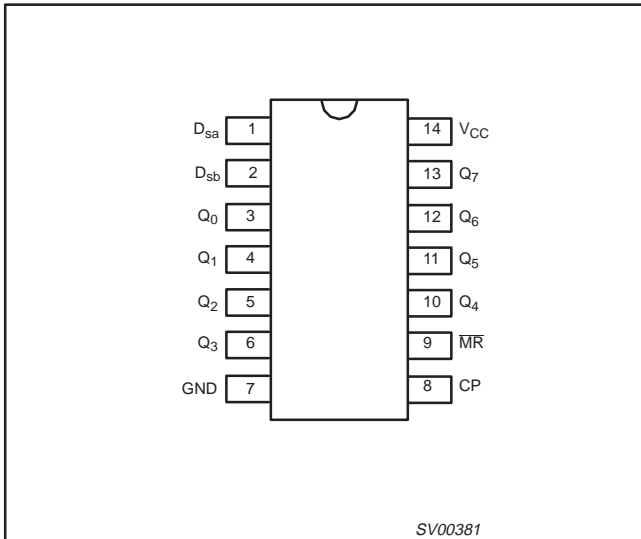
## ORDERING INFORMATION

| PACKAGES                    | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|-----------------------------|-------------------|-----------------------|---------------|-------------|
| 14-Pin Plastic DIL          | -40°C to +125°C   | 74LV164 N             | 74LV164 N     | SOT27-1     |
| 14-Pin Plastic SO           | -40°C to +125°C   | 74LV164 D             | 74LV164 D     | SOT108-1    |
| 14-Pin Plastic SSOP Type II | -40°C to +125°C   | 74LV164 DB            | 74LV164 DB    | SOT337-1    |
| 14-Pin Plastic TSSOP Type I | -40°C to +125°C   | 74LV164 PW            | 74LV164PW DH  | SOT402-1    |

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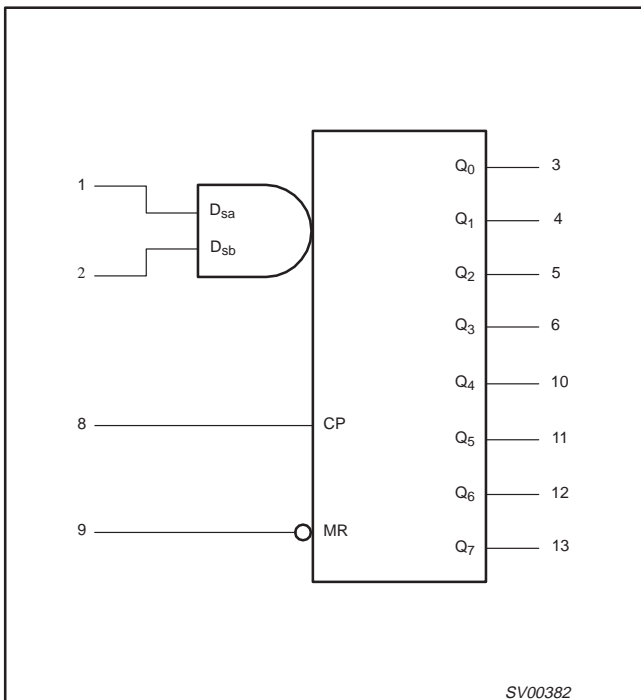
### PIN CONFIGURATION



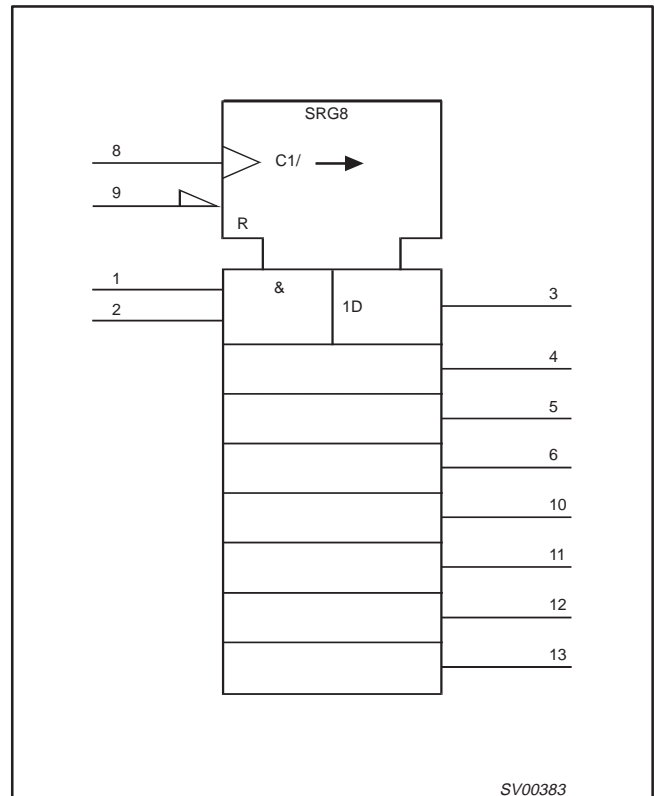
### PIN DESCRIPTION

| PIN NUMBER                 | SYMBOL                            | FUNCTION                                  |
|----------------------------|-----------------------------------|---|
| 1,2                        | D <sub>sa</sub> , D <sub>sb</sub> | Data inputs                               |
| 3, 4, 5, 6, 10, 11, 12, 13 | Q <sub>0</sub> to Q <sub>7</sub>  | Outputs                                   |
| 7                          | GND                               | Ground (0V)                               |
| 8                          | CP                                | Clock input (LOW-to-HIGH, edge-triggered) |
| 9                          | $\overline{\text{MR}}$            | Master reset input (active LOW)           |
| 14                         | V <sub>CC</sub>                   | Positive supply voltage                   |

### LOGIC SYMBOL



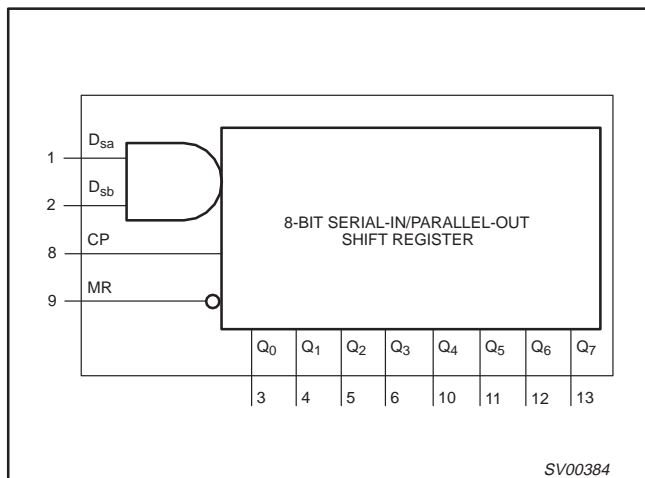
### LOGIC SYMBOL (IEEE/IEC)



# 8-bit serial-in/parallel-out shift register

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## FUNCTIONAL DIAGRAM



## FUNCTION TABLE

| OPERATING MODES | INPUTS |    |                 |                 | OUTPUTS        |                                 |
|-----------------|--------|----|-----------------|-----------------|----------------|---------------------------------|
|                 | MR     | CP | D <sub>sa</sub> | D <sub>sb</sub> | Q <sub>0</sub> | Q <sub>1</sub> - Q <sub>7</sub> |
| Reset (clear)   | L      | X  | x               | x               | L              | L - L                           |
| Shift           | H      | ↑  | l               | l               | L              | q <sub>0</sub> - q <sub>6</sub> |
|                 | H      | ↑  | l               | h               | L              | q <sub>0</sub> - q <sub>6</sub> |
|                 | H      | ↑  | h               | l               | L              | q <sub>0</sub> - q <sub>6</sub> |
|                 | H      | ↑  | h               | h               | H              | q <sub>0</sub> - q <sub>6</sub> |

H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 q = Lower case letter indicates the state of referenced input one set-up time prior to the LOW-to-HIGH CP transition  
 ↑ = LOW-to-HIGH clock transition

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)  
 Voltages are referenced to GND (ground = 0V)

| SYMBOL                                  | PARAMETER  | CONDITIONS  | RATING            | UNIT |
|---|--|---|-------------------|------|
| V <sub>CC</sub>                         | DC supply voltage  |   | -0.5 to +7.0      | V    |
| ±I <sub>IK</sub>                        | DC input diode current   | V <sub>I</sub> < -0.5 or V <sub>I</sub> > V <sub>CC</sub> + 0.5V  | 20                | mA   |
| ±I <sub>OK</sub>                        | DC output diode current  | V <sub>O</sub> < -0.5 or V <sub>O</sub> > V <sub>CC</sub> + 0.5V  | 50                | mA   |
| ±I <sub>O</sub>                         | DC output source or sink current<br>- standard outputs   | -0.5V < V <sub>O</sub> < V <sub>CC</sub> + 0.5V   | 25                | mA   |
| ±I <sub>GND</sub> ,<br>±I <sub>CC</sub> | DC V <sub>CC</sub> or GND current for types with<br>-standard outputs  |   | 50                | mA   |
| T <sub>stg</sub>                        | Storage temperature range  |   | -65 to +150       | °C   |
| P <sub>TOT</sub>                        | Power dissipation per package<br>-plastic DIL<br>-plastic mini-pack (SO)<br>-plastic shrink mini-pack (SSOP and TSSOP) | for temperature range: -40 to +125°C<br>above +70°C derate linearly with 12mW/K<br>above +70°C derate linearly with 8 mW/K<br>above +60°C derate linearly with 5.5 mW/K | 750<br>500<br>400 | mW   |

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL                          | PARAMETER                                       | CONDITIONS   | MIN              | TYP.             | MAX                     | UNIT |
|---------------------------------|---|--|------------------|------------------|-------------------------|------|
| V <sub>CC</sub>                 | DC supply voltage                               | See Note 1   | 1.0              | 3.3              | 5.5                     | V    |
| V <sub>I</sub>                  | Input voltage                                   |  | 0                | -                | V <sub>CC</sub>         | V    |
| V <sub>O</sub>                  | Output voltage                                  |  | 0                | -                | V <sub>CC</sub>         | V    |
| T <sub>amb</sub>                | Operating ambient temperature range in free air | See DC and AC characteristics  | -40<br>-40       |                  | +85<br>+125             | °C   |
| t <sub>r</sub> , t <sub>f</sub> | Input rise and fall times                       | V <sub>CC</sub> = 1.0V to 2.0V<br>V <sub>CC</sub> = 2.0V to 2.7V<br>V <sub>CC</sub> = 2.7V to 3.6V<br>V <sub>CC</sub> = 3.6V to 5.5V | -<br>-<br>-<br>- | -<br>-<br>-<br>- | 500<br>200<br>100<br>50 | ns/V |

### NOTES:

- The LV is guaranteed to function down to V<sub>CC</sub> = 1.0V (input levels GND or V<sub>CC</sub>); DC characteristics are guaranteed from V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 5.5V.

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**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

| SYMBOL           | PARAMETER                                     | TEST CONDITIONS   | LIMITS              |                  |                     |                     |     | UNIT |
|------------------|---|---|---------------------|------------------|---------------------|---------------------|-----|------|
|                  |   |   | -40°C to +85°C      |                  |                     | -40°C to +125°C     |     |      |
|                  |   |   | MIN                 | TYP <sup>1</sup> | MAX                 | MIN                 | MAX |      |
| V <sub>IH</sub>  | HIGH level Input voltage                      | V <sub>CC</sub> = 1.2V  | 0.9                 |                  |                     | 0.9                 |     | V    |
|                  |   | V <sub>CC</sub> = 2.0V  | 1.4                 |                  |                     | 1.4                 |     |      |
|                  |   | V <sub>CC</sub> = 2.7 to 3.6V   | 2.0                 |                  |                     | 2.0                 |     |      |
|                  |   | V <sub>CC</sub> = 4.5 to 5.5V   | 0.7*V <sub>CC</sub> |                  |                     | 0.7*V <sub>CC</sub> |     |      |
| V <sub>IL</sub>  | LOW level Input voltage                       | V <sub>CC</sub> = 1.2V  |                     |                  | 0.3                 | 0.3                 | V   |      |
|                  |   | V <sub>CC</sub> = 2.0V  |                     |                  | 0.6                 | 0.6                 |     |      |
|                  |   | V <sub>CC</sub> = 2.7 to 3.6V   |                     |                  | 0.8                 | 0.8                 |     |      |
|                  |   | V <sub>CC</sub> = 4.5 to 5.5  |                     |                  | 0.3*V <sub>CC</sub> | 0.3*V <sub>CC</sub> |     |      |
| V <sub>OH</sub>  | HIGH level output voltage; all outputs        | V <sub>CC</sub> = 1.2V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA |                     | 1.2              |                     |                     | V   |      |
|                  |   | V <sub>CC</sub> = 2.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA | 1.8                 | 2.0              |                     | 1.8                 |     |      |
|                  |   | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA | 2.5                 | 2.7              |                     | 2.5                 |     |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA | 2.8                 | 3.0              |                     | 2.8                 |     |      |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 100µA | 4.3                 | 4.5              |                     | 4.3                 |     |      |
| V <sub>OH</sub>  | HIGH level output voltage; STANDARD outputs   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 6mA   | 2.40                | 2.82             |                     | 2.20                | V   |      |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; -I <sub>O</sub> = 12mA  | 3.60                | 4.20             |                     | 3.50                |     |      |
| V <sub>OL</sub>  | LOW level output voltage; all outputs         | V <sub>CC</sub> = 1.2V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA  |                     | 0                |                     |                     | V   |      |
|                  |   | V <sub>CC</sub> = 2.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA  |                     | 0                | 0.2                 | 0.2                 |     |      |
|                  |   | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA  |                     | 0                | 0.2                 | 0.2                 |     |      |
|                  |   | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA  |                     | 0                | 0.2                 | 0.2                 |     |      |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100µA  |                     | 0                | 0.2                 | 0.2                 |     |      |
| V <sub>OL</sub>  | LOW level output voltage; STANDARD outputs    | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA    |                     | 0.25             | 0.40                | 0.50                | V   |      |
|                  |   | V <sub>CC</sub> = 4.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA   |                     | 0.35             | 0.55                | 0.65                |     |      |
| I <sub>I</sub>   | Input leakage current                         | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND                                       |                     |                  | 1.0                 | 1.0                 | µA  |      |
| I <sub>CC</sub>  | Quiescent supply current; MSI                 | V <sub>CC</sub> = 5.5V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0                   |                     |                  | 20.0                | 160                 | µA  |      |
| ΔI <sub>CC</sub> | Additional quiescent supply current per input | V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V                               |                     |                  | 500                 | 850                 | µA  |      |

**NOTES:**1. All typical values are measured at T<sub>amb</sub> = 25°C.

## 8-bit serial-in/parallel-out shift register

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## AC CHARACTERISTICS

GND = 0V;  $t_r = t_f \leq 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 1\text{k}\Omega$ 

| SYMBOL                          | PARAMETER  | WAVEFORM | CONDITION  | LIMITS<br>-40 to +85 °C |                  |     | LIMITS<br>-40 to +125 °C |     | UNIT |
|---------------------------------|--|----------|------------|-------------------------|------------------|-----|--------------------------|-----|------|
|                                 |  |          |            | MIN                     | TYP <sup>1</sup> | MAX | MIN                      | MAX |      |
| $t_{\text{PHL}}/t_{\text{PLH}}$ | Propagation delay<br>CP to $Q_n$                       | Figure 1 | 1.2        | –                       | 75               | –   | –                        | –   | ns   |
|                                 |  |          | 2.0        | –                       | 26               | 39  | –                        | 49  |      |
|                                 |  |          | 2.7        | –                       | 19               | 29  | –                        | 36  |      |
|                                 |  |          | 3.0 to 3.6 | –                       | 14 <sup>2</sup>  | 23  | –                        | 29  |      |
|                                 |  |          | 4.5 to 5.5 | –                       | 12 <sup>2</sup>  | 19  | –                        | 24  |      |
| $t_{\text{PHL}}$                | Propagation delay<br>MR to $Q_n$                       | Figure 2 | 1.2        | –                       | 75               | –   | –                        | –   | ns   |
|                                 |  |          | 2.0        | –                       | 26               | 39  | –                        | 49  |      |
|                                 |  |          | 2.7        | –                       | 19               | 29  | –                        | 36  |      |
|                                 |  |          | 3.0 to 3.6 | –                       | 14 <sup>2</sup>  | 23  | –                        | 29  |      |
|                                 |  |          | 4.5 to 5.5 | –                       | 12 <sup>2</sup>  | 19  | –                        | 24  |      |
| $t_w$                           | Clock pulse width<br>HIGH to LOW                       | Figure 1 | 2.0        | 34                      | 9                | –   | 41                       | –   | ns   |
|                                 |  |          | 2.7        | 25                      | 6                | –   | 30                       | –   |      |
|                                 |  |          | 3.0 to 3.6 | 20                      | 5 <sup>2</sup>   | –   | 24                       | –   |      |
|                                 |  |          | 4.5 to 5.5 | 13                      | 4 <sup>2</sup>   | –   | 16                       | –   |      |
| $t_w$                           | Master reset pulse<br>width; LOW                       | Figure 2 | 2.0        | 34                      | 10               | –   | 41                       | –   | ns   |
|                                 |  |          | 2.7        | 25                      | 8                | –   | 30                       | –   |      |
|                                 |  |          | 3.0 to 3.6 | 20                      | 6 <sup>2</sup>   | –   | 24                       | –   |      |
|                                 |  |          | 4.5 to 5.5 | 13                      | 5 <sup>2</sup>   | –   | 16                       | –   |      |
| $t_{\text{rem}}$                | Removal time<br>MR to CP                               | Figure 2 | 1.2        | –                       | 30               | –   | –                        | –   | ns   |
|                                 |  |          | 2.0        | 19                      | 10               | –   | 24                       | –   |      |
|                                 |  |          | 2.7        | 14                      | 8                | –   | 18                       | –   |      |
|                                 |  |          | 3.0 to 3.6 | 11                      | 6 <sup>2</sup>   | –   | 14                       | –   |      |
|                                 |  |          | 4.5 to 5.5 | 8                       | 5 <sup>2</sup>   | –   | 10                       | –   |      |
| $t_{\text{su}}$                 | Set-up time<br>$D_{\text{sa}}$ , $D_{\text{sb}}$ to CP | Figure 3 | 1.2        | –                       | 15               | –   | –                        | –   | ns   |
|                                 |  |          | 2.0        | 22                      | 5                | –   | 26                       | –   |      |
|                                 |  |          | 2.7        | 16                      | 4                | –   | 19                       | –   |      |
|                                 |  |          | 3.0 to 3.6 | 13                      | 3 <sup>2</sup>   | –   | 15                       | –   |      |
|                                 |  |          | 4.5 to 5.5 | 9                       | 2 <sup>2</sup>   | –   | 10                       | –   |      |
| $t_h$                           | Hold time<br>$D_{\text{sa}}$ , $D_{\text{sb}}$ to CP   | Figure 3 | 1.2        | –                       | –10              | –   | –                        | –   | ns   |
|                                 |  |          | 2.0        | 5                       | –3               | –   | 5                        | –   |      |
|                                 |  |          | 2.7        | 5                       | –2               | –   | 5                        | –   |      |
|                                 |  |          | 3.0 to 3.6 | 5                       | –2 <sup>2</sup>  | –   | 5                        | –   |      |
|                                 |  |          | 4.5 to 5.5 | 5                       | –1 <sup>2</sup>  | –   | 5                        | –   |      |
| $f_{\text{max}}$                | Maximum clock<br>pulse frequency                       | Figure 1 | 2.0        | 14                      | 40               | –   | 12                       | –   | MHz  |
|                                 |  |          | 2.7        | 19                      | 58               | –   | 16                       | –   |      |
|                                 |  |          | 3.0 to 3.6 | 24                      | 70 <sup>2</sup>  | –   | 20                       | –   |      |
|                                 |  |          | 4.5 to 5.5 | 36                      | 100 <sup>2</sup> | –   | 30                       | –   |      |

## NOTE:

1. Unless otherwise stated, all typical values are at  $T_{\text{amb}} = 25^\circ\text{C}$ .
2. Typical value measured at  $V_{\text{CC}} = 3.3\text{V}$ .
3. Typical value measured at  $V_{\text{CC}} = 5.0\text{V}$ .

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## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V \leq 3.6V$   
 $V_M = 0.5V * V_{CC}$  at  $V_{CC} < 2.7V$  and  $\geq 4.5V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

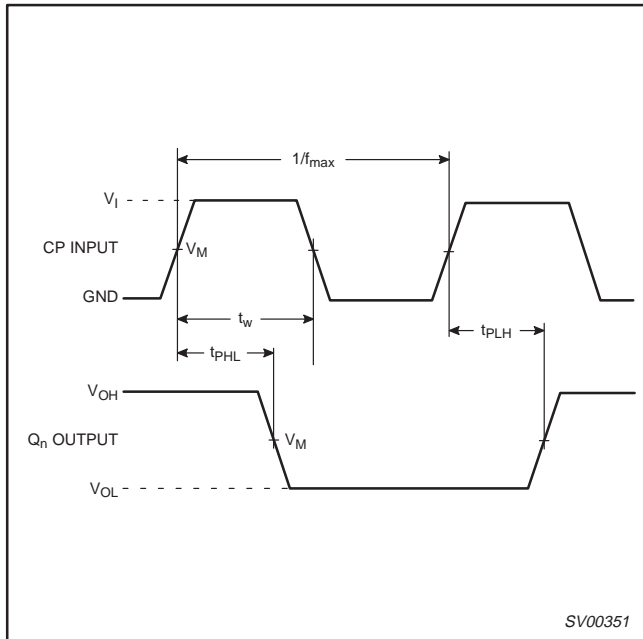


Figure 1. The clock (CP) to output (Q<sub>n</sub>) propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency

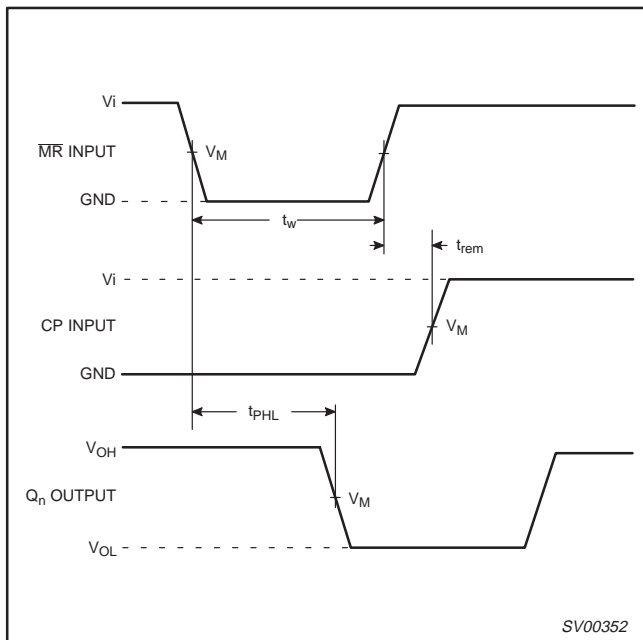


Figure 2. The master reset ( $\overline{MR}$ ) pulse width, the master reset to output (Q<sub>n</sub>) propagation delay and the master reset to clock (CP) removal time

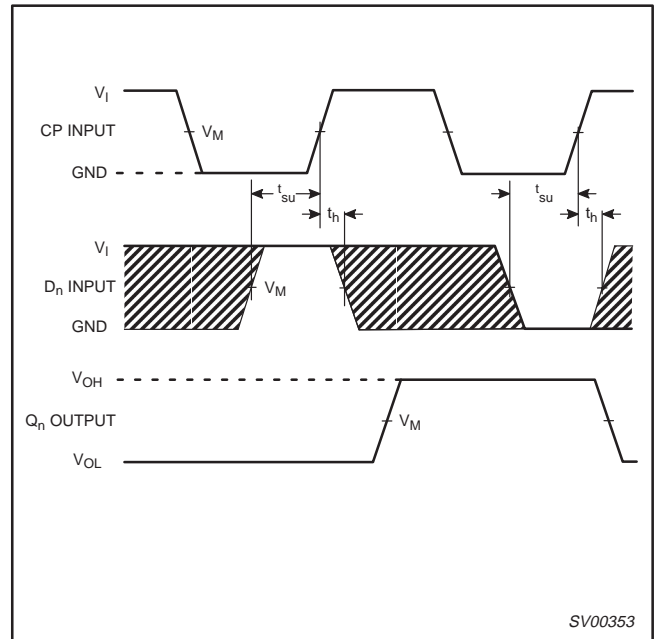


Figure 3. Data set-up and hold times for the D<sub>n</sub> inputs

**NOTE:**

The shaded areas indicate when the input is permitted to change for predictable output performance.

## TEST CIRCUIT

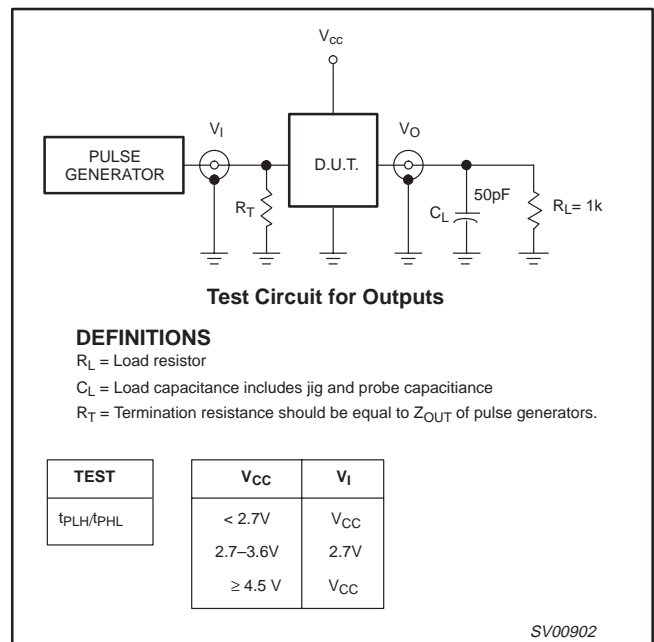


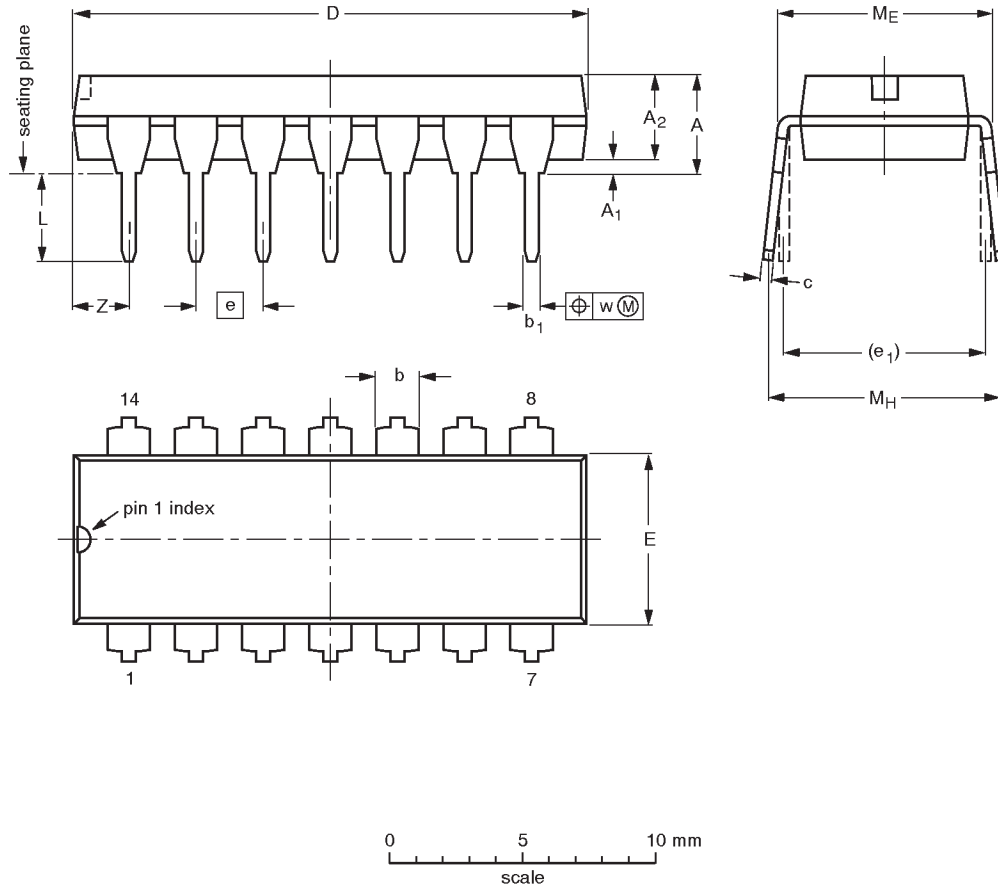
Figure 4. Load circuitry for switching times

# 8-bit serial-in/parallel-out shift register

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w     | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|-----------------------|
| mm     | 4.2    | 0.51                | 3.2                 | 1.73<br>1.13   | 0.53<br>0.38   | 0.36<br>0.23   | 19.50<br>18.55   | 6.48<br>6.20     | 2.54 | 7.62           | 3.60<br>3.05 | 8.25<br>7.80   | 10.0<br>8.3    | 0.254 | 2.2                   |
| inches | 0.17   | 0.020               | 0.13                | 0.068<br>0.044 | 0.021<br>0.015 | 0.014<br>0.009 | 0.77<br>0.73     | 0.26<br>0.24     | 0.10 | 0.30           | 0.14<br>0.12 | 0.32<br>0.31   | 0.39<br>0.33   | 0.01  | 0.087                 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |                     |                      |
| SOT27-1         | 050G04     | MO-001AA |      |                     | 92-11-17<br>95-03-11 |

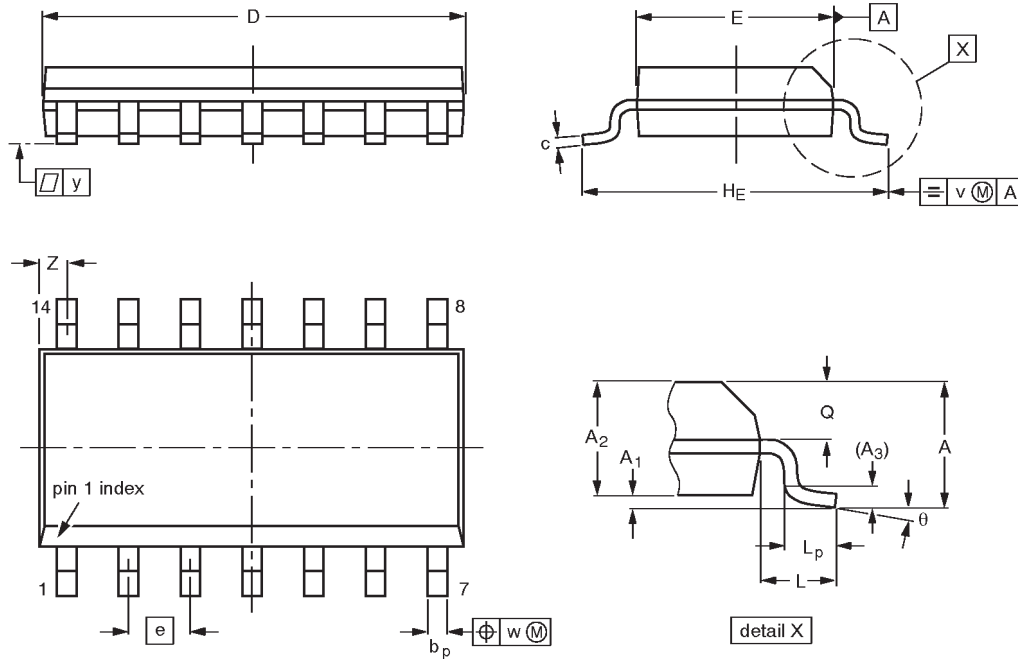


# 8-bit serial-in/parallel-out shift register

## 74LV164

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub>   | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c                | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | $\theta$ |
|--------|--------|------------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 1.75   | 0.25<br>0.10     | 1.45<br>1.25   | 0.25           | 0.49<br>0.36   | 0.25<br>0.19     | 8.75<br>8.55     | 4.0<br>3.8       | 1.27  | 6.2<br>5.8     | 1.05  | 1.0<br>0.4     | 0.7<br>0.6     | 0.25 | 0.25 | 0.1   | 0.7<br>0.3       | 8°<br>0° |
| inches | 0.069  | 0.0098<br>0.0039 | 0.057<br>0.049 | 0.01           | 0.019<br>0.014 | 0.0098<br>0.0075 | 0.35<br>0.34     | 0.16<br>0.15     | 0.050 | 0.24<br>0.23   | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

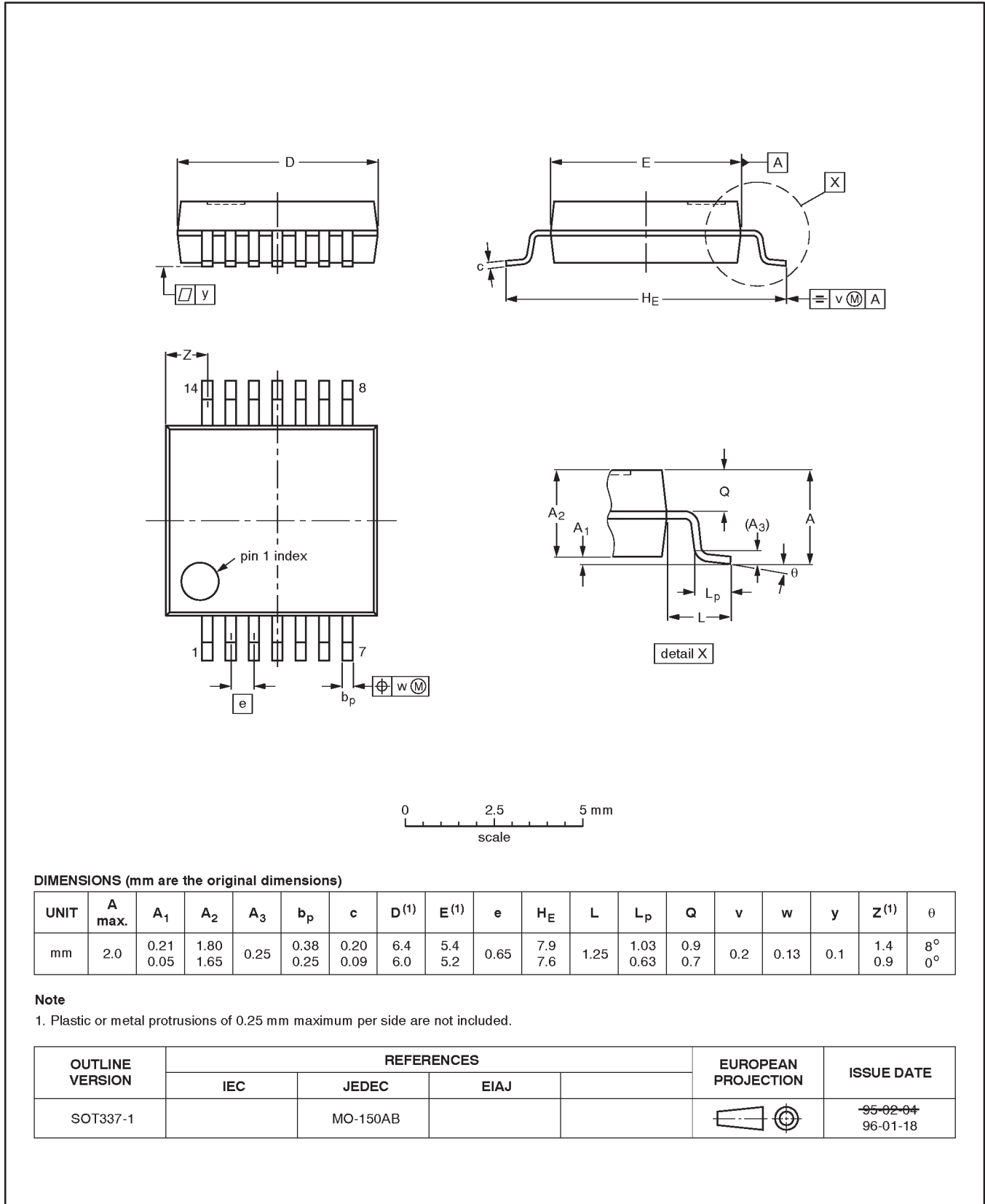
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT108-1        | 076E06S    | MS-012AB |      |  |                     | 91-08-13<br>95-01-23 |

# 8-bit serial-in/parallel-out shift register

## 74LV164

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm**

**SOT337-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c            | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L    | L <sub>p</sub> | Q          | v   | w    | y   | Z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 2.0    | 0.21<br>0.05   | 1.80<br>1.65   | 0.25           | 0.38<br>0.25   | 0.20<br>0.09 | 6.4<br>6.0       | 5.4<br>5.2       | 0.65 | 7.9<br>7.6     | 1.25 | 1.03<br>0.63   | 0.9<br>0.7 | 0.2 | 0.13 | 0.1 | 1.4<br>0.9       | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

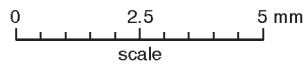
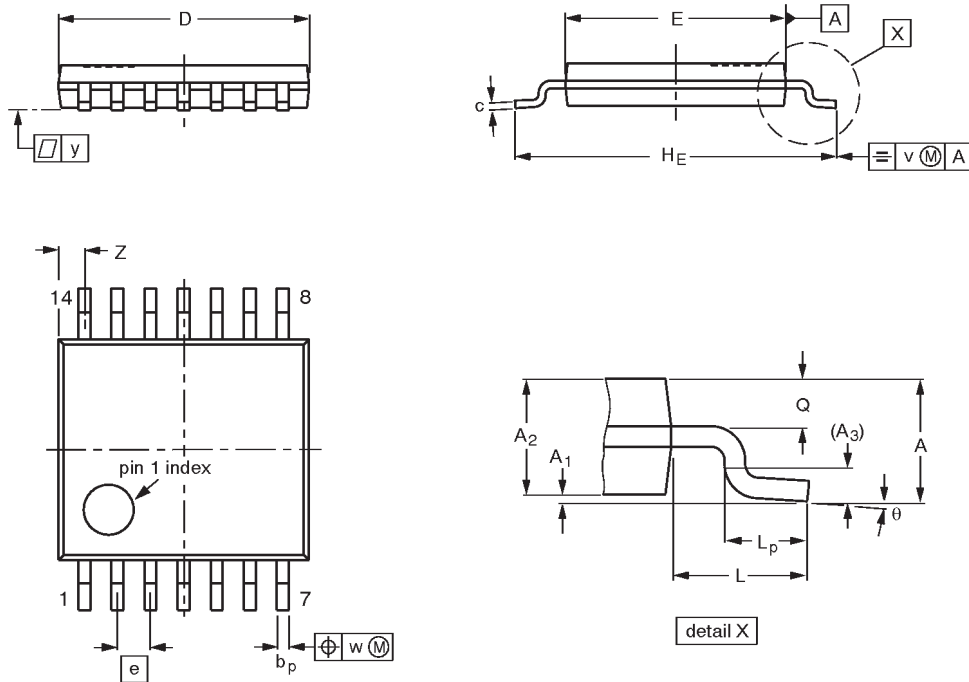
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE                      |
|-----------------|------------|----------|------|--|---------------------|---------------------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                                 |
| SOT337-1        |            | MO-150AB |      |  |                     | <del>95-02-04</del><br>96-01-18 |

# 8-bit serial-in/parallel-out shift register

## 74LV164

**TSSOP14:** plastic thin shrink small outline package; 14 leads; body width 4.4 mm

**SOT402-1**



**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c          | D <sup>(1)</sup> | E <sup>(2)</sup> | e    | H <sub>E</sub> | L   | L <sub>p</sub> | Q          | v   | w    | y   | z <sup>(1)</sup> | θ        |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm   | 1.10   | 0.15<br>0.05   | 0.95<br>0.80   | 0.25           | 0.30<br>0.19   | 0.2<br>0.1 | 5.1<br>4.9       | 4.5<br>4.3       | 0.65 | 6.6<br>6.2     | 1.0 | 0.75<br>0.50   | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.72<br>0.38     | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |      |  | EUROPEAN PROJECTION | ISSUE DATE             |
|-----------------|------------|--------|------|--|---------------------|------------------------|
|                 | IEC        | JEDEC  | EIAJ |  |                     |                        |
| SOT402-1        |            | MO-153 |      |  |                     | -94-07-12-<br>95-04-04 |

## 8-bit serial-in/parallel-out shift register

74LV164

## DEFINITIONS

| Data Sheet Identification        | Product Status                | Definition   |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i>   | <b>Formative or in Design</b> | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.   |
| <i>Preliminary Specification</i> | <b>Preproduction Product</b>  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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