

DATA SHEET

74LV10

Triple 3-input NAND gate

Product data

Supersedes data of 1998 Apr 20

2003 Mar 04

Triple 3-input NAND gate

74LV10

FEATURES

- Optimized for Low Voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C.
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25$ °C.
- Output capability: standard
- I_{CC} category: SSI

DESCRIPTION

The 74LV10 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT10.

The 74LV10 provides the 3-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nA, nB, nC to nY	$C_L = 15$ pF; $V_{CC} = 3.3$ V	9	ns
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	See Notes 1 and 2	12	pF

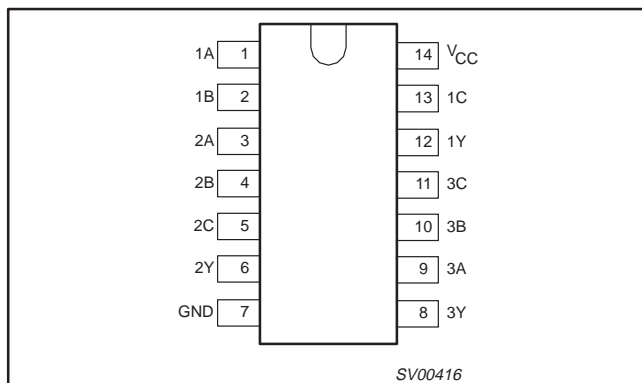
NOTES:

- C_{PD} is used to determine the dynamic power dissipation (P_D in μ W)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 N = number of outputs switching;
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
- The condition is $V_I = \text{GND to } V_{CC}$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	PKG. DWG. #
14-Pin Plastic SO	-40 °C to +125 °C	74LV10D	SOT108-1

PIN CONFIGURATION



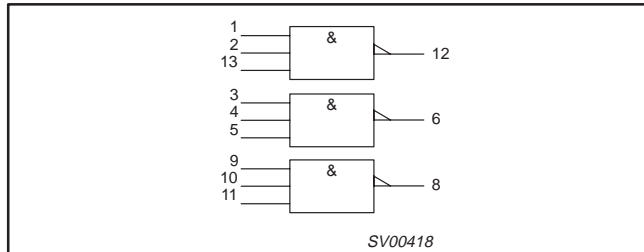
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 3, 9	1A – 3A	Data inputs
2, 4, 10	1B – 3B	Data inputs
7	GND	Ground (0 V)
12, 6, 8	1Y – 3Y	Data outputs
13, 5, 11	1C – 3C	Data inputs
14	V_{CC}	Positive supply voltage

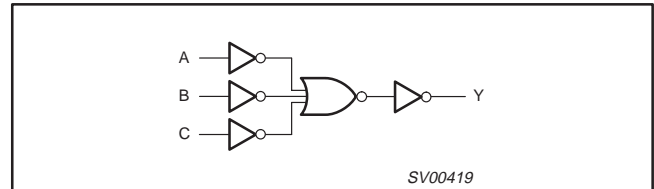
Triple 3-input NAND gate

74LV10

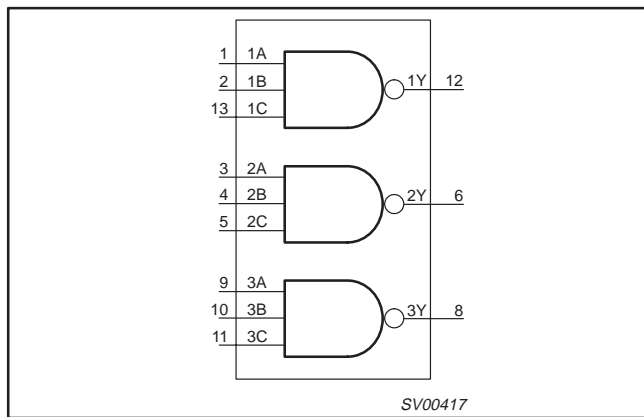
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM (ONE GATE)



LOGIC SYMBOL



FUNCTION TABLE

INPUTS			OUTPUTS
nA	nB	nC	nY
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

NOTES:
 H = HIGH voltage level
 L = LOW voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V_{CC}	DC supply voltage	See Note1	1.0	3.3	3.6	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 1.0\text{ V to }2.0\text{ V}$	–	–	500	ns/V
		$V_{CC} = 2.0\text{ V to }2.7\text{ V}$	–	–	200	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	–	–	100	ns/V

NOTE:
 1. The LV is guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.6\text{ V}$.

Triple 3-input NAND gate

74LV10

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5 \text{ V}$ or $V_O > V_{CC} + 0.5 \text{ V}$	50	mA
$\pm I_O$	DC output source or sink current (standard outputs)	$-0.5 \text{ V} < V_O < V_{CC} + 0.5 \text{ V}$	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with standard outputs		50	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO)	for temperature range: -40 °C to +125 °C above +70 °C derate linearly with 8 mW/K	500	mW

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40 °C to +85 °C			-40 °C to +125 °C		
			MIN	TYP ¹	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	$V_{CC} = 1.2 \text{ V}$	0.9			0.9		V
		$V_{CC} = 2.0 \text{ V}$	1.4			1.4		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0			2.0		
V_{IL}	LOW level Input voltage	$V_{CC} = 1.2 \text{ V}$			0.3		0.3	V
		$V_{CC} = 2.0 \text{ V}$			0.6		0.6	
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$			0.8		0.8	
V_{OH}	HIGH level output voltage; all outputs	$V_{CC} = 1.2 \text{ V}; V_I = V_{IH}$ or $V_{IL}; -I_O = 100 \mu\text{A}$		1.2				V
		$V_{CC} = 2.0 \text{ V}; V_I = V_{IH}$ or $V_{IL}; -I_O = 100 \mu\text{A}$	1.8	2.0		1.8		
		$V_{CC} = 2.7 \text{ V}; V_I = V_{IH}$ or $V_{IL}; -I_O = 100 \mu\text{A}$	2.5	2.7		2.5		
		$V_{CC} = 3.0 \text{ V}; V_I = V_{IH}$ or $V_{IL}; -I_O = 100 \mu\text{A}$	2.8	3.0		2.8		
V_{OH}	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0 \text{ V}; V_I = V_{IH}$ or $V_{IL}; -I_O = 6 \text{ mA}$	2.40	2.82		2.20		V
V_{OL}	LOW level output voltage; all outputs	$V_{CC} = 1.2 \text{ V}; V_I = V_{IH}$ or $V_{IL}; I_O = 100 \mu\text{A}$		0				V
		$V_{CC} = 2.0 \text{ V}; V_I = V_{IH}$ or $V_{IL}; I_O = 100 \mu\text{A}$		0	0.2		0.2	
		$V_{CC} = 2.7 \text{ V}; V_I = V_{IH}$ or $V_{IL}; I_O = 100 \mu\text{A}$		0	0.2		0.2	
		$V_{CC} = 3.0 \text{ V}; V_I = V_{IH}$ or $V_{IL}; I_O = 100 \mu\text{A}$		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0 \text{ V}; V_I = V_{IH}$ or $V_{IL}; I_O = 6 \text{ mA}$		0.25	0.40		0.50	V
I_I	Input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC}$ or GND			1.0		1.0	μA
I_{CC}	Quiescent supply current; SSI	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		40	μA
ΔI_{CC}	Additional quiescent supply current per input	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}; V_I = V_{CC} - 0.6 \text{ V}$			500		850	μA

NOTE:

- All typical values are measured at $T_{amb} = 25 \text{ °C}$.

Triple 3-input NAND gate

74LV10

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 1$ k Ω

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 °C to +85 °C			-40 °C to +125 °C		
				V _{CC} (V)	MIN	TYP ¹	MAX	MIN	
t _{PHL/PLH}	Propagation delay nA, nB, nC to nY	Figure 1, 2	1.2		55				ns
			2.0		19	36		44	
			2.7		14	26		33	
			3.0 to 3.6		10 ²	21		26	

NOTES:

1. Unless otherwise stated, all typical values are measured at T_{amb} = 25 °C.
2. Typical values are measured at V_{CC} = 3.3 V.

AC WAVEFORMS

V_M = 1.5 V at V_{CC} ≥ 2.7 V;

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V;

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

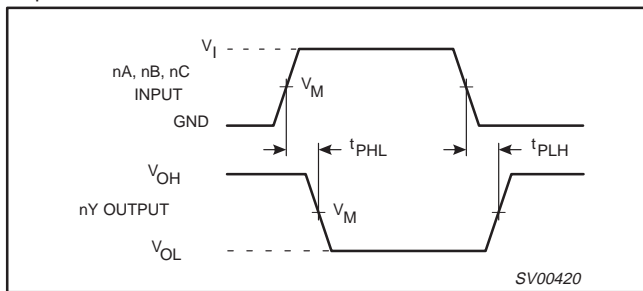


Figure 1. Input (nA, nB, nC) to output (nY) propagation delays.

TEST CIRCUIT

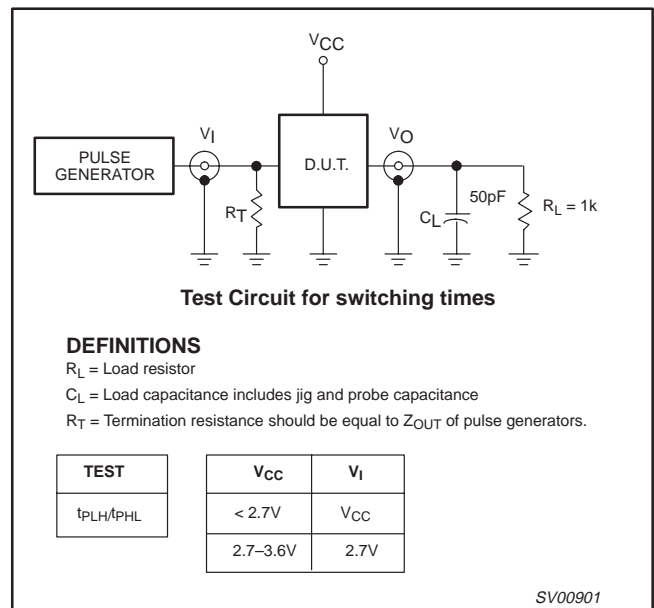


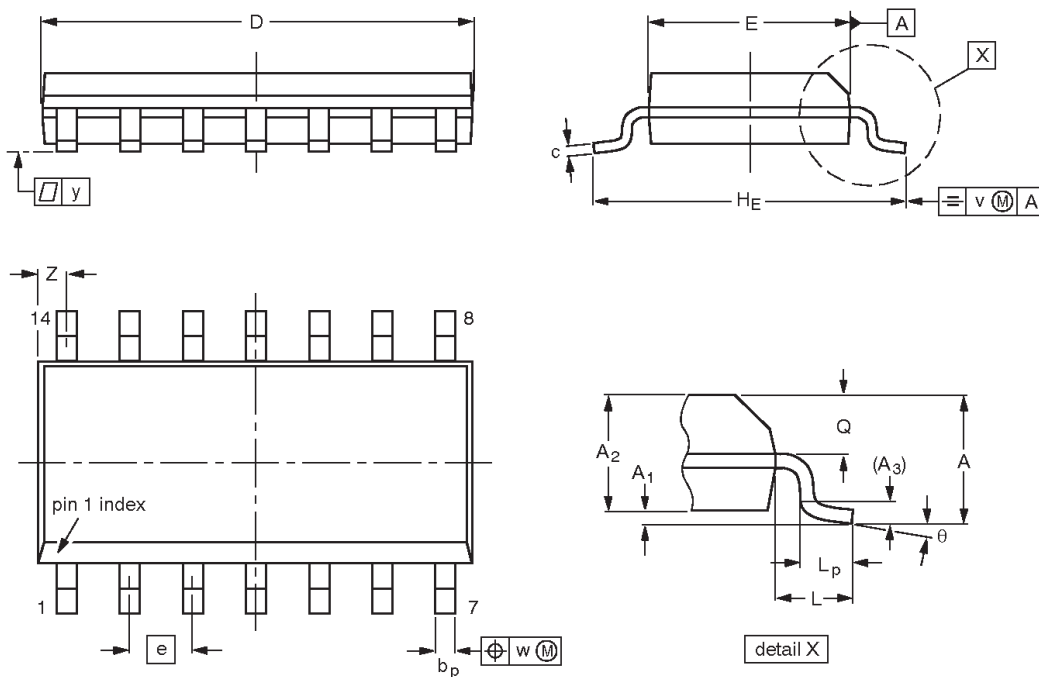
Figure 2. Load circuitry for switching times.

Triple 3-input NAND gate

74LV10

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

Triple 3-input NAND gate

74LV10

REVISION HISTORY

Rev	Date	Description
_3	20030304	Product data (9397 750 11193). ECN 853-1919 29491 of 07 February 2003. Supersedes data of 1998 Apr 20 (9397 750 04407). Modifications: <ul style="list-style-type: none"> • Delete DIL, SSOP and TSSOP package ordering and package outlines (discontinued options). • Correct power dissipation formula.
_2	19980420	Product specification (9397 750 04407). ECN 853-1919 19256 of 20 April 1998. Supersedes data of 1997 Feb 12.

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products—including circuits, standard cells, and/or software—described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

© Koninklijke Philips Electronics N.V. 2003
 All rights reserved. Printed in U.S.A.

For sales offices addresses send e-mail to:
sales.addresses@www.semiconductors.philips.com

Date of release: 03-03
 Document order number: 9397 750 11193

Let's make things better.