INTEGRATED CIRCUITS

DATA SHEET

74F299

8-bit universal shift/storage register (3-State)

Product data
Supersedes data of 1990 Mar 01

2003 Feb 05

Philips
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FEATURES

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: Shift left, shift right, load and store
- 3-State outputs for bus-oriented applications

DESCRIPTION

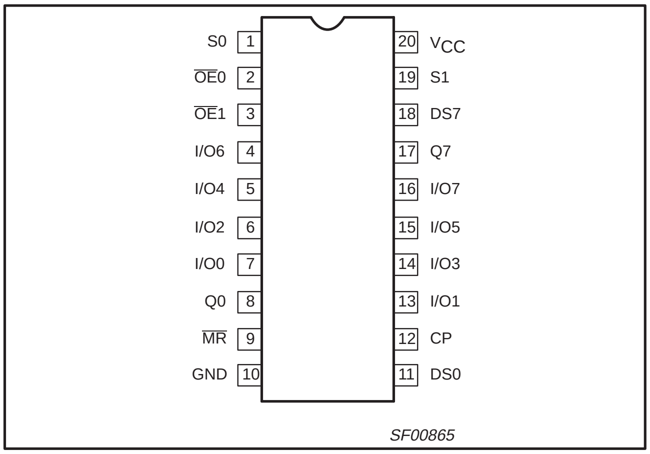
The 74F299 is an 8-bit universal shift/storage register with 3-State outputs. Four modes of operation are possible: Hold (store), shift left, shift right and parallel load. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0 and Q7 to allow easy serial cascading. A separate active-LOW Master Reset is used to reset the register.

The 74F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1, as shown in the Function Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{\text{MR}}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of clock are observed.

A HIGH signal on either $\overline{\text{OE}}$0 or $\overline{\text{OE}}$1 disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S0 and S1 in preparation for a parallel load operation.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F299	115 MHz	58 mA

ORDERING INFORMATION

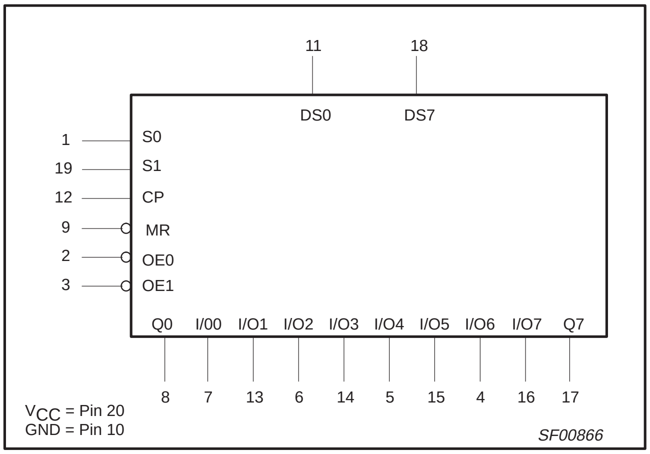
DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5 V ±10%, T_{amb} = 0 °C to +70 °C	
20-pin plastic DIP	N74F299N	SOT146-1
20-pin plastic SOL	N74F299D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

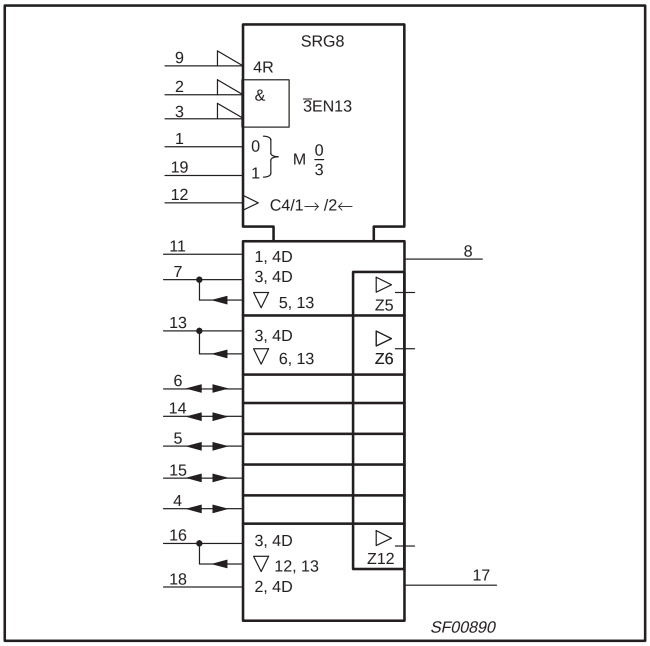
PINS	DESCRIPTION	74F(U.L.) HIGH / LOW	LOAD VALUE HIGH / LOW
DS0	Serial data input for right shift	1.0 / 1.0	20 µA / 0.6 mA
DS7	Serial data input for left shift	1.0 / 1.0	20 µA / 0.6 mA
S0, S1	Mode select inputs	1.0 / 2.0	20 µA / 1.2 mA
CP	Clock pulse input (Active rising edge)	1.0 / 1.0	20 µA / 0.6 mA
$\overline{\text{MR}}$	Asynchronous Master Reset input (Active LOW)	1.0 / 1.0	20 µA / 0.6 mA
$\overline{\text{OE}}$0, $\overline{\text{OE}}$1	Output Enable input (Active LOW)	1.0 / 1.0	20 µA / 0.6 mA
Q0, Q7	Serial outputs	50 / 33	1.0 mA / 20 mA
I/On	Multiplexed parallel data inputs	3.5 / 1.0	70 µA / 0.6 mA
	3-State parallel outputs	150 / 40	3.0 mA / 24 mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 µA in the HIGH State and 0.6 mA in the LOW state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

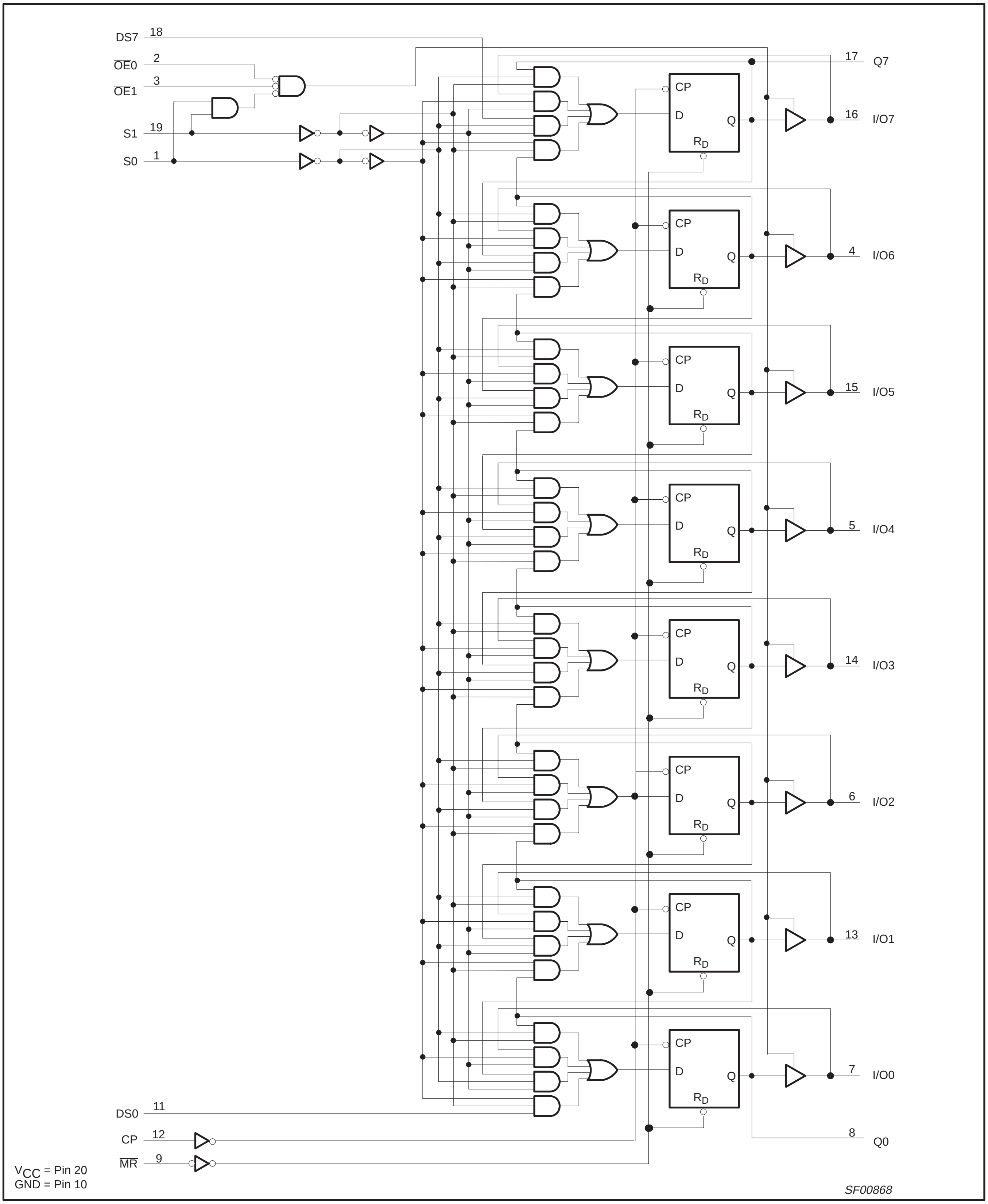


FUNCTION TABLE

INPUTS	INPUTS				OPERATING MODE
$\overline{\text{OE}}$n	$\overline{\text{MR}}$	S1	S0	CP	
L	L	X	X	X	Asynchronous Reset; Q0 – Q7 = LOW
L	H	H	H	↑	Parallel load; I/On → Qn (I/On outputs disabled)
L	H	L	H	↑	Shift right; DS0 → Q0, Q0 → Q1, etc.
L	H	H	L	↑	Shift left; DS7 → Q7, Q7 → Q6, etc.
L	H	L	L	X	Hold
H	X	X	X	X	Outputs in High-Z

H = HIGH voltage level
L = LOW voltage level
X = Don’t care
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IN}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state		–0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in LOW output state	Q0, Q7	40	mA
		I/On	48	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	HIGH-level output current	Q0, Q7			–1	mA
		I/On			–3	mA
I_{OL}	LOW-level output current	Q0, Q7			20	mA
		I/On			24	mA
T_{amb}	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	HIGH-level output voltage	Q0, Q7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –1 mA	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
		I/On		I_{OH} = –3 mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.3		V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, $I_I = I_{IK}$				–0.73	–1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = MAX, V_I = 7.0 V					100	µA
		I/On	V_{CC} = 5.5V, V_I = 5.5 V					1	mA
I_{IH}	HIGH-level input current	except I/On	V_{CC} = MAX, V_I = 2.7 V					20	µA
I_{IL}	LOW-level input current	S0, S1	V_{CC} = MAX, V_I = 0.5 V					–1.2	mA
		others						–0.6	mA
$I_{IH} + I_{OZH}$	Off-state output current, HIGH-level voltage applied	I/On only	V_{CC} = MAX, V_O = 2.7 V					70	µA
$I_{IL} + I_{OZL}$	Off-state output current LOW-level voltage applied		V_{CC} = MAX, V_O = 0.5 V					–0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX			–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX				55	60	mA
		I_{CCL}					70	90	mA
		I_{CCZ}					65	95	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

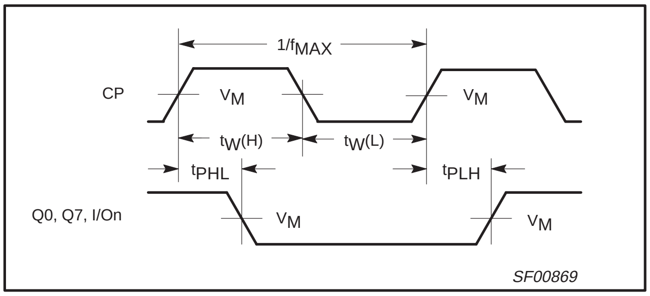
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	I/O	Waveform 1	70	100		70		MHz
		Qn		85	115		85		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q0 or Q7		Waveform 1	4.0 4.5	5.0 6.0	7.5 8.0	3.5 4.5	8.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to I/On		Waveform 1	4.0 4.0	6.0 6.5	9.0 9.0	4.0 4.0	10.0 10.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q0 or Q7		Waveform 2	5.5	7.5	9.5	5.5	10.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/On		Waveform 2	5.5	7.5	10.0	5.5	10.5	ns
t_{PZH} t_{PZL}	Output Enable time Sn, $\overline{OE}$ to I/On		Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	9.0 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time Sn, $\overline{OE}$ to I/On		Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	8.0 6.5	ns ns

AC SET-UP REQUIREMENTS

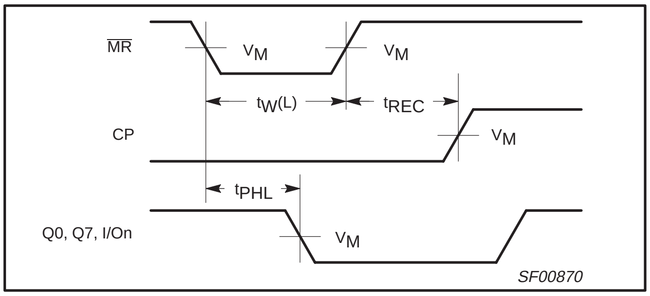
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW S0 or S1 to CP	Waveform 3	6.5 6.5			7.5 7.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW S0 or S1 to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, HIGH or LOW I/On, DS_L or DS_R to CP	Waveform 3	3.5 3.5			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, HIGH or LOW I/On, DS_L or DS_R to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, HIGH or LOW	Waveform 1	5.0 4.5			5.0 4.5		ns
$t_w(L)$	$\overline{MR}$ Pulse width, LOW	Waveform 2	4.5			4.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

AC WAVEFORMS

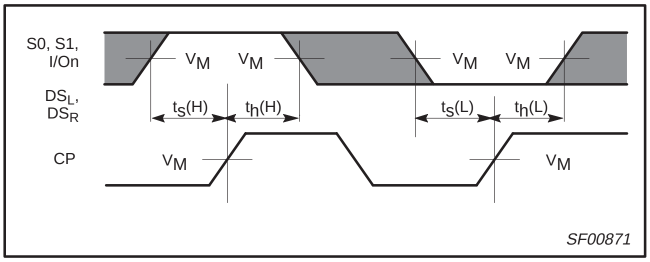
For all waveforms, V_M = 1.5 V
The shaded areas indicate when the input is permitted to change for predictable output performance.



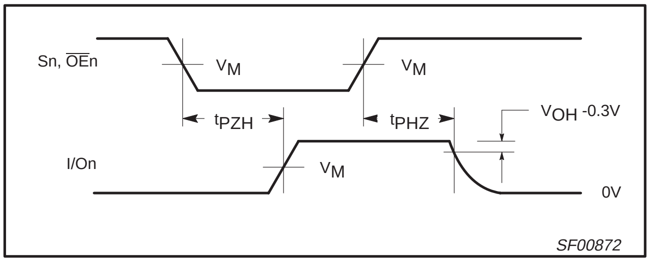
Waveform 1. Propagation delay, clock input to output, clock width, and maximum clock frequency



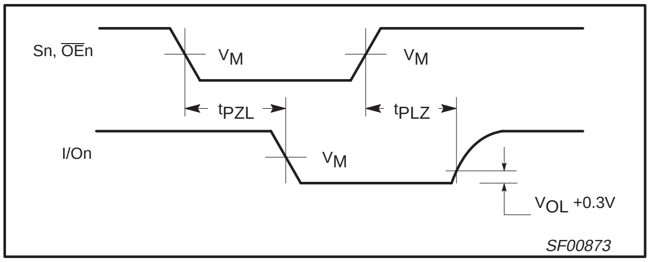
Waveform 2. Master Reset pulse width, Master Reset to output delay, and Master Reset to clock recovery time



Waveform 3. Set-up and hold times

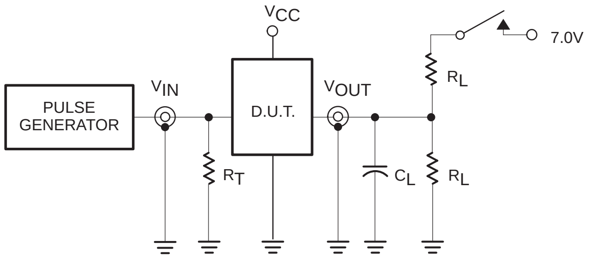


Waveform 4. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level

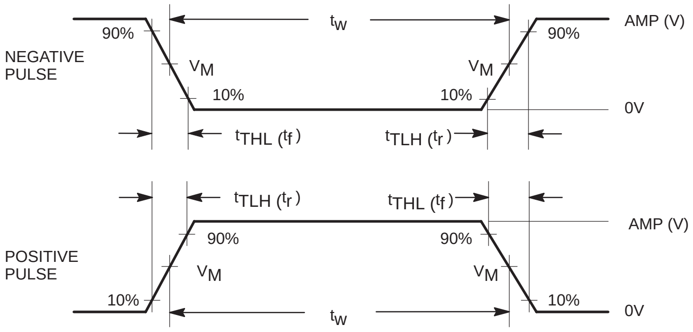


Waveform 5. 3-State Output Enable time to LOW level and Output Disable time from LOW level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

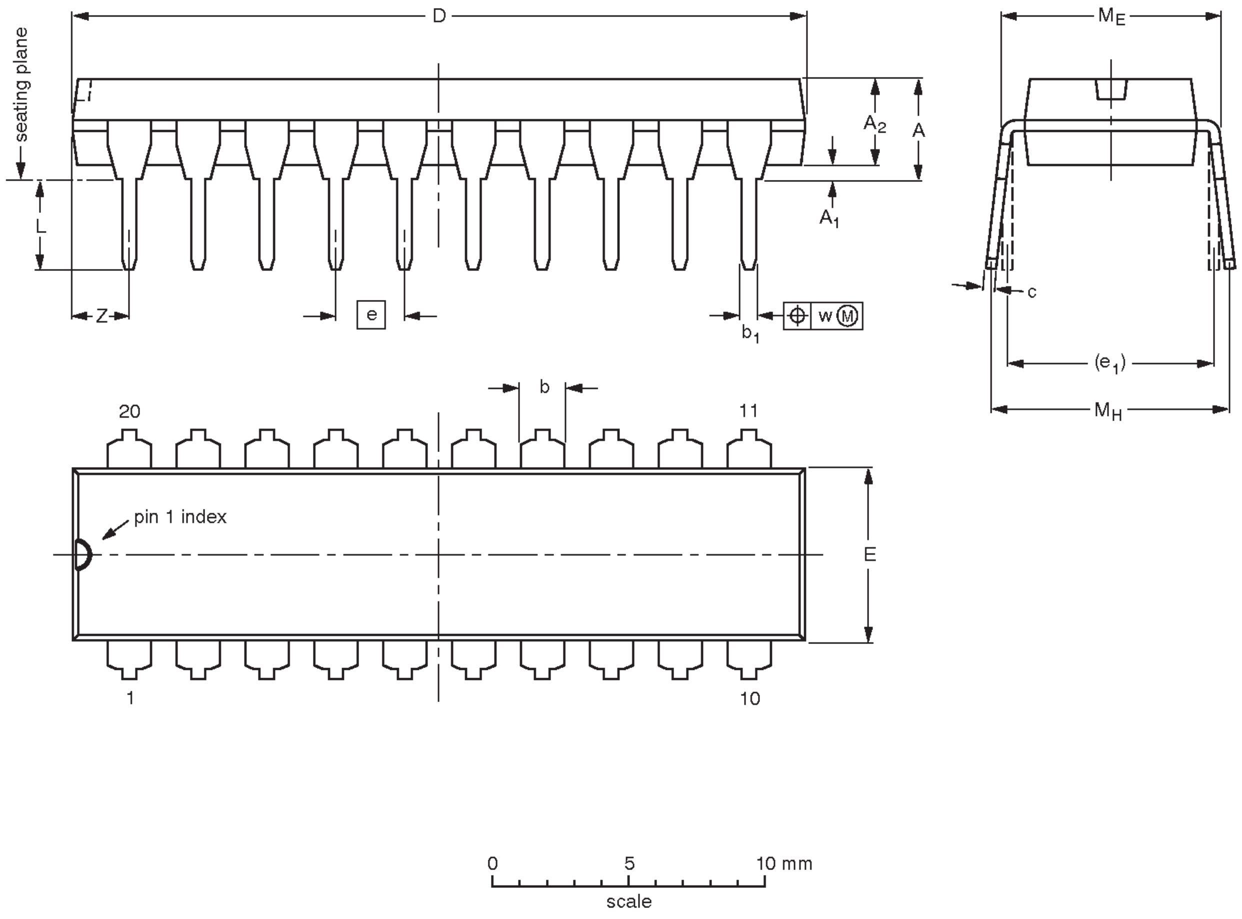
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	**V_M**	**rep. rate**	**t_w**	**t_{TLH}**	**t_{THL}**
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

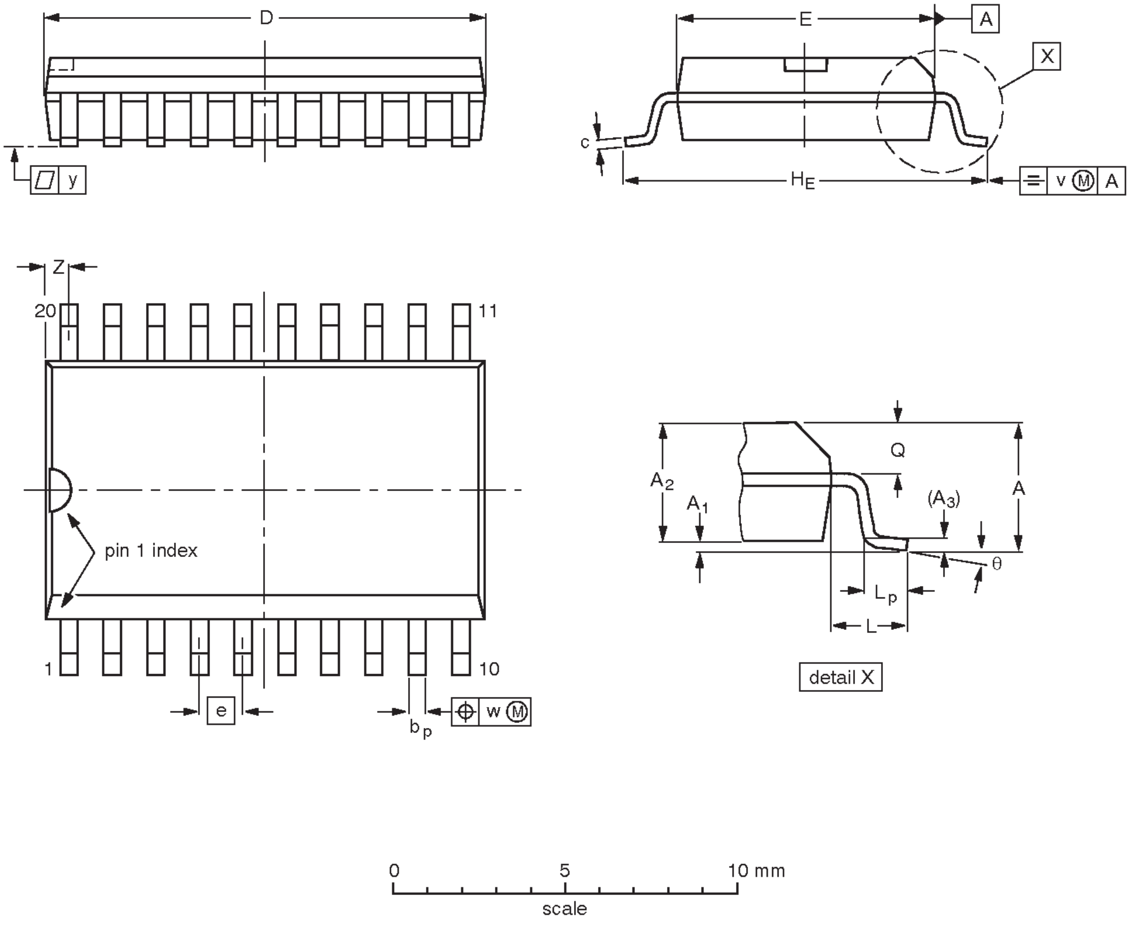
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1		MS-001	SC-603			~~95-05-24~~ 99-12-27

SO20: plastic small outline package; 20 leads; body width 7.5 mm SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_3	20030205	**Product data (9397 750 11037); ECN 853-0365 29307 of 17 December 2002.** **Supersedes Product specification (9397 750 05117) of 01 March 1990.** Modifications: • Delete all references to DB package. Package option was discontinued.
_2	19900301	**Product specification (9397 750 05117); ECN 853-0365 29307 of 01 March 1990.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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