

# DATA SHEET

## **74F219A**

64-bit TTL bipolar RAM, non-inverting  
(3-State)

Product specification

1996 Jan 05

IC15 Data Handbook

## 64-bit TTL bipolar RAM, non-inverting (3-State)

74F219A

## FEATURES

- High speed performance
- Replaces 74F219
- Address access time: 8ns max vs 28ns for 74F219
- Power dissipation: 4.3mW/bit typ
- Schottky clamp TTL
- One chip enable
- Non-Inverting outputs (for inverting outputs see 74F189A)
- 3-state outputs
- 74F219A in 150 mil wide SO is preferred options for new designs
- C3F219A in 300 mil wide SOL replaces 74F219 in existing designs

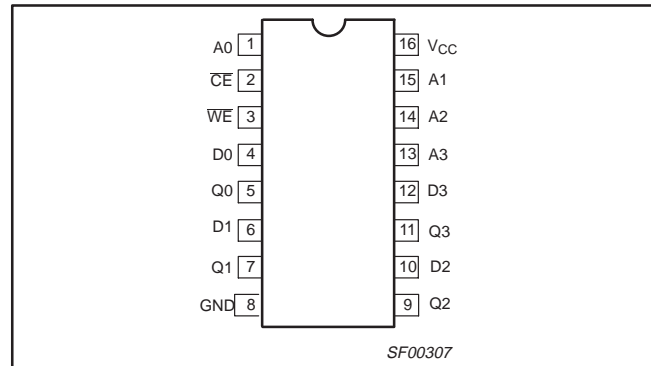
## DESCRIPTION

The 74F219A is a high speed, 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs are in high impedance state whenever the chip enable ( $\overline{CE}$ ) is high. The outputs are active only in the READ mode ( $\overline{WE}$  = high) and the output data is the complement of the stored data.

## APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

## PIN CONFIGURATION



TYPE	TYPICAL ACCESS TIME	TYPICAL SUPPLY CURRENT(TOTAL)
74F219A	5.0ns	55mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
16-pin plastic Dual In-line Package	N74F219AN	SOT38-4
16-pin plastic Small Outline (150mil)	N74F219AD	SOT109-1
16-pin plastic Small Outline Large (300mil)	C3F219AD	SOT162-1

## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

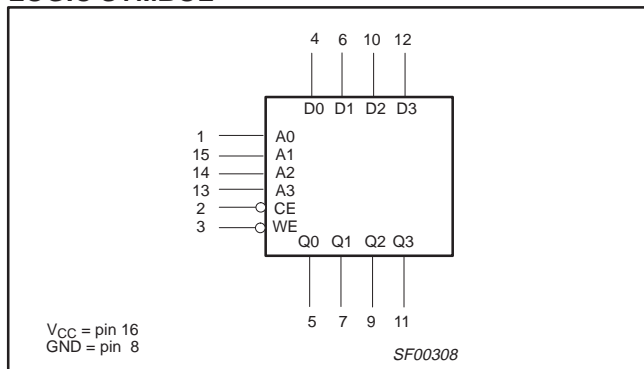
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
A0 – A3	Address inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\overline{CE}$	Chip enable input (active low)	1.0/2.0	20 $\mu$ A/1.2mA
$\overline{WE}$	Write enable input (active low)	1.0/2.0	20 $\mu$ A/1.2mA
Q0 – Q3	Data outputs	150/40	3mA/24mA

**NOTE:** One (1.0) FAST unit load is defined as: 20 $\mu$ A in the high state and 0.6mA in the low state.

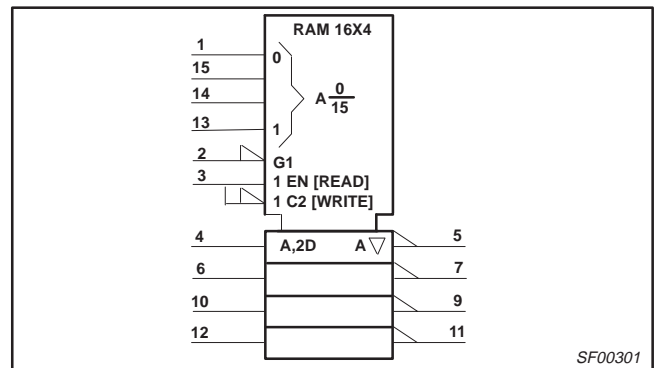
# 64-bit TTL bipolar RAM, non-inverting (3-State)

## 74F219A

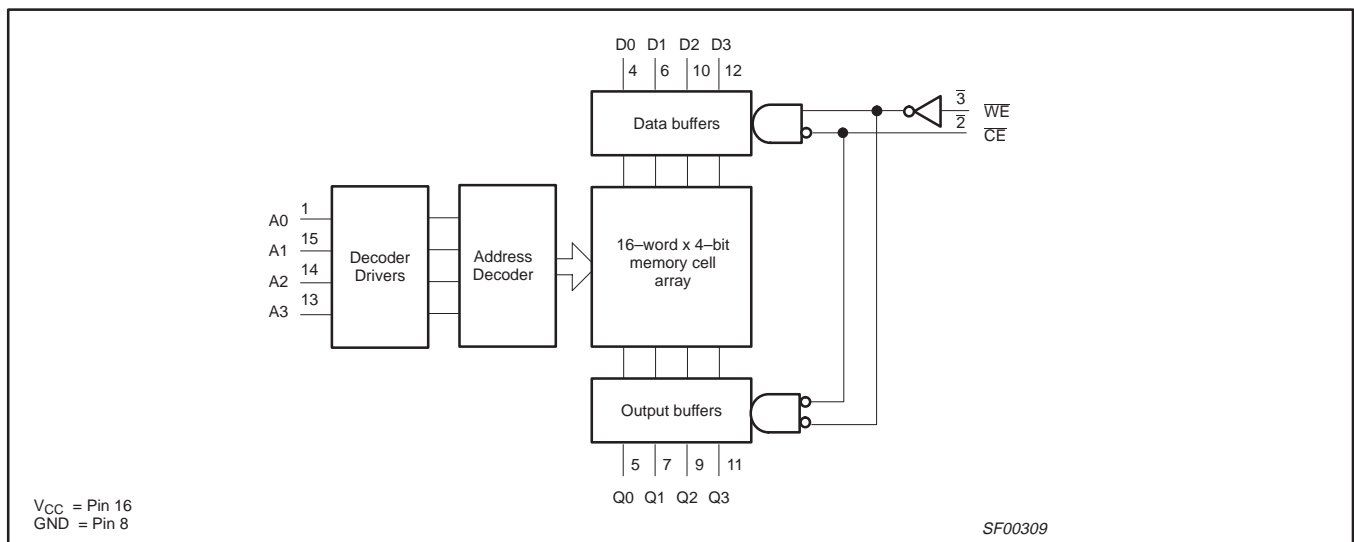
### LOGIC SYMBOL



### IEC/IEEE SYMBOL



### LOGIC DIAGRAM



### FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
CE	WE	D <sub>n</sub>	Q <sub>n</sub>	
L	H	X	Stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

#### NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care

## 64-bit TTL bipolar RAM, non-inverting (3-State)

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in high output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in low output state	48	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-3	mA
I <sub>OL</sub>	Low-level output current			24	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>	2.4		V	
		V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±5%V <sub>CC</sub>	2.7	3.4	V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>		0.35	0.50	V
		V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±5%V <sub>CC</sub>		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA
I <sub>IL</sub>	Low-level input current	others CE, WE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA
							-1.2
I <sub>OZH</sub>	Offset output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				50	μA
I <sub>OZL</sub>	Offset output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				-50	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60		-150	mA
I <sub>CC</sub>	Supply current (total)	V <sub>CC</sub> = MAX, CE = WE = GND			55	80	mA
C <sub>IN</sub>	Input capacitance	V <sub>CC</sub> = 5V, V <sub>IN</sub> = 2.0V			4		pF
C <sub>OUT</sub>	Output capacitance	V <sub>CC</sub> = 5V, V <sub>OUT</sub> = 2.0V			7		pF

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## 64-bit TTL bipolar RAM, non-inverting (3-State)

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Access time	Propagation delay An to Qn	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	8.0 8.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>		Enable time CE to Qn	Waveform 2	1.5 2.5	3.0 4.0	6.0 7.0	1.5 2.0	7.0 7.5	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Disable time CE to Qn		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.0	8.0 6.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Write recovery time	Enable time WE to Qn	Waveform 4	2.0 3.0	3.5 4.5	6.5 7.5	1.5 2.5	7.0 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>		Disable time WE to Qn	Waveform 4	3.0 1.5	5.0 3.5	8.0 6.0	2.5 1.5	9.0 7.0	

## AC SETUP REQUIREMENT

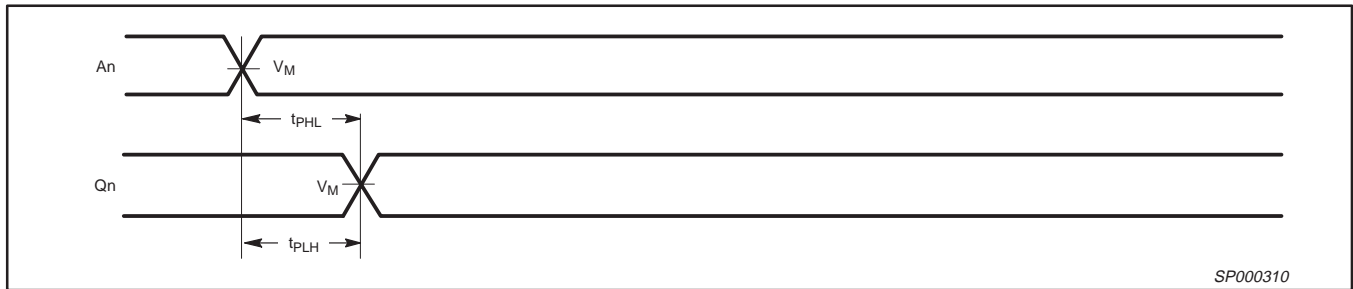
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t <sub>su(H)</sub> t <sub>su(L)</sub>	Setup time, high or low An to $\overline{WE}$		Waveform 4	4.5 4.5			5.0 5.0		ns
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold time, high or low An to $\overline{WE}$		Waveform 4	0 0			0 0		
t <sub>su(H)</sub> t <sub>su(L)</sub>	Setup time, high or low Dn to $\overline{WE}$		Waveform 4	8.0 7.5			9.0 8.5		ns
t <sub>h(H)</sub> t <sub>h(L)</sub>	Hold time, high or low Dn to $\overline{WE}$		Waveform 4	0 0			0 0		
t <sub>su(L)</sub>	Setup time, low CE (falling edge) to $\overline{WE}$ (falling edge)		Waveform 4	0			0		ns
t <sub>h(L)</sub>	Hold time, low WE (falling edge) to $\overline{WE}$ (rising edge)		Waveform 4	6.5			7.5		ns
t <sub>w(L)</sub>	Pulse width, low WE		Waveform 4	7.0			8.0		ns

# 64-bit TTL bipolar RAM, non-inverting (3-State)

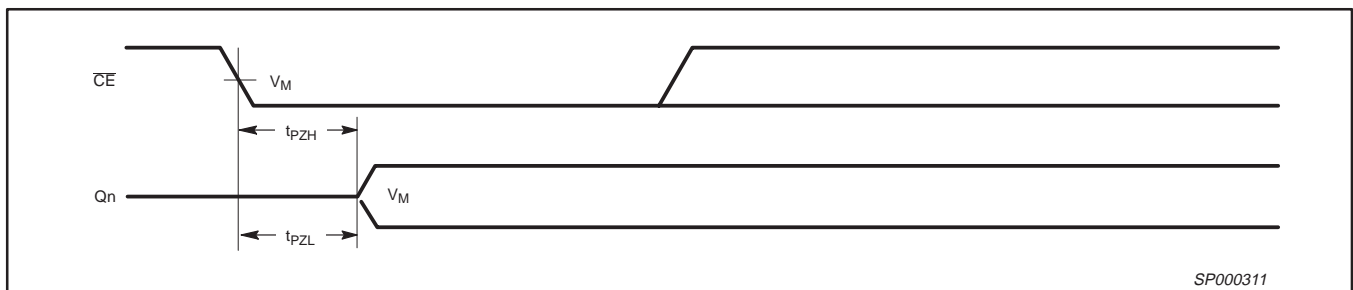
# 74F219A

## AC WAVEFORMS FOR READ CYCLES

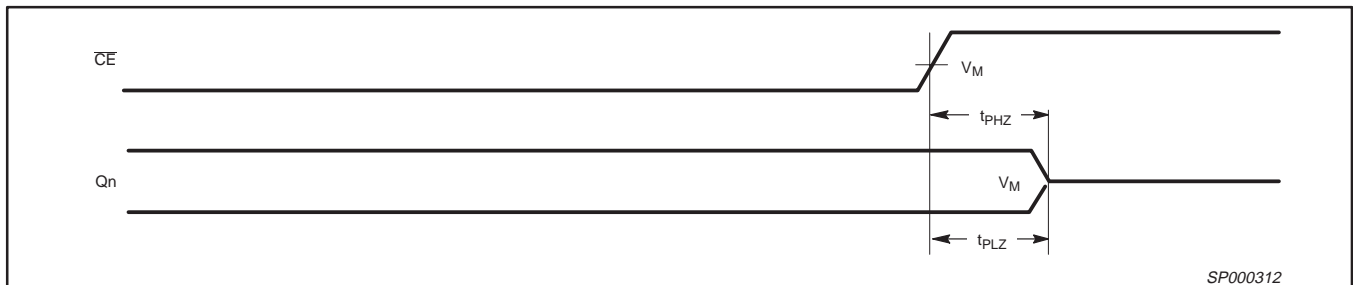
For all waveforms,  $V_M = 1.5V$ .



Waveform 1. Read cycle, address access time



Waveform 2. Read cycle, chip enable access time

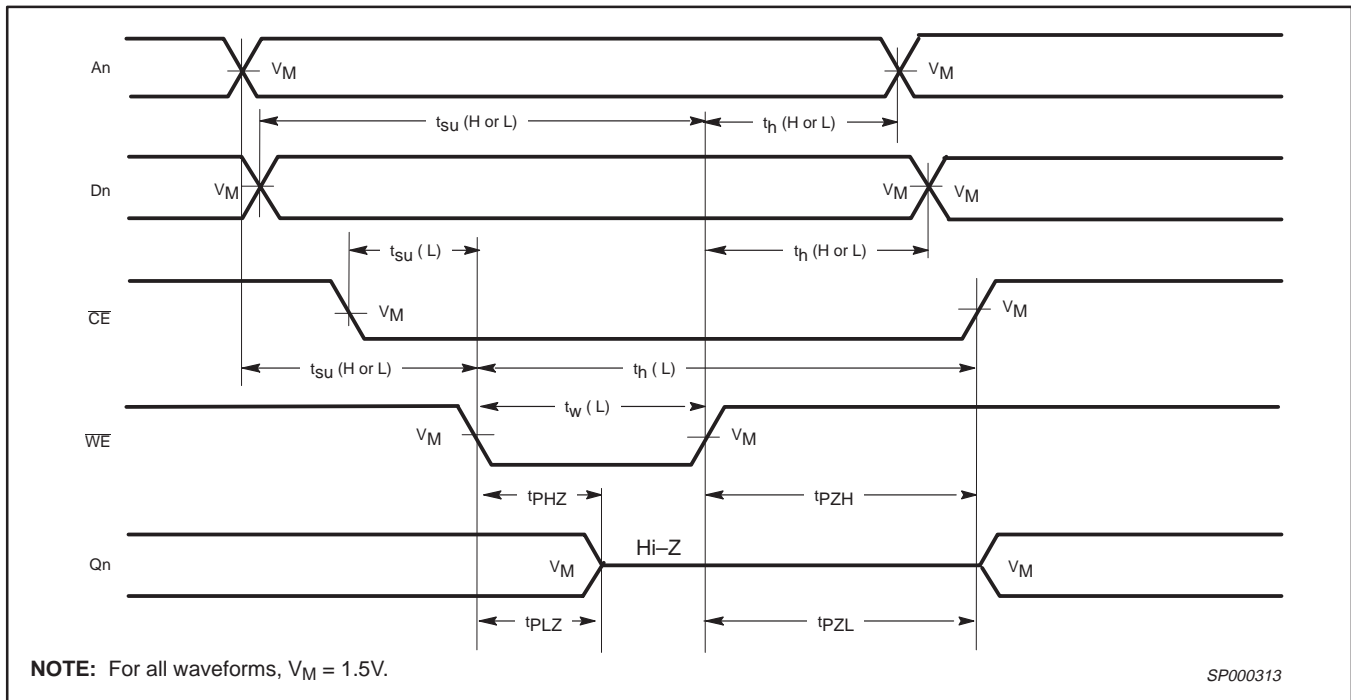


Waveform 3. Read cycle, chip disable time

# 64-bit TTL bipolar RAM, non-inverting (3-State)

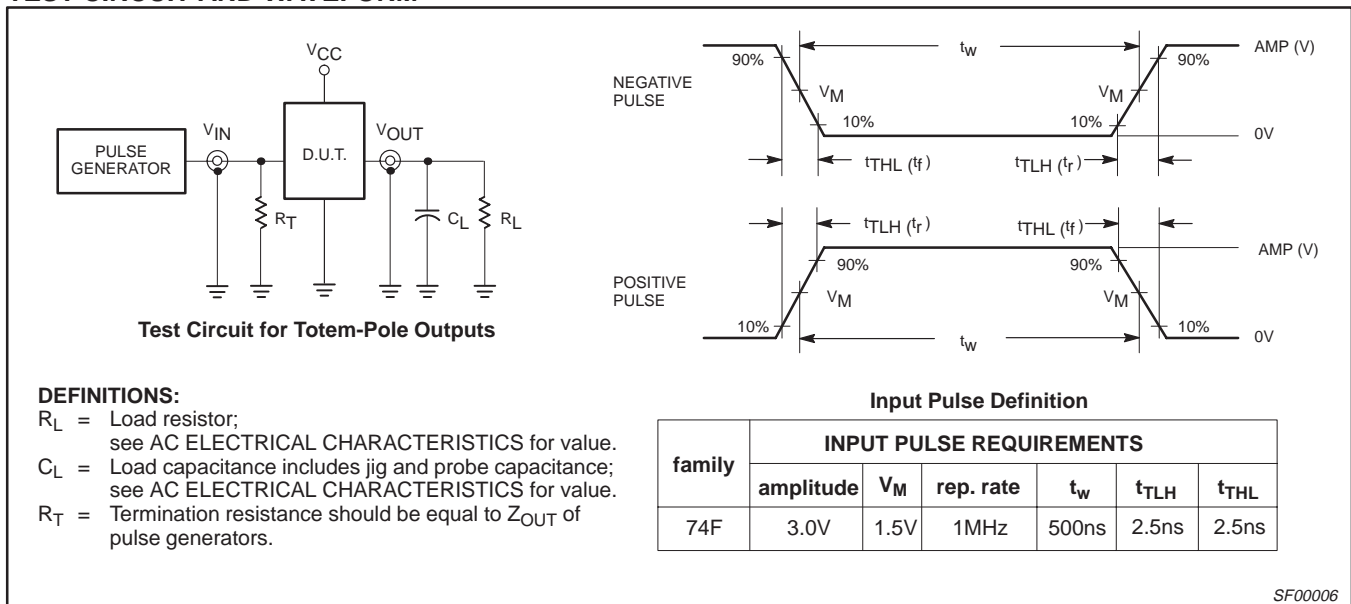
# 74F219A

## AC WAVEFORMS FOR WRITE CYCLE



Waveform 4. Write cycle

## TEST CIRCUIT AND WAVEFORM

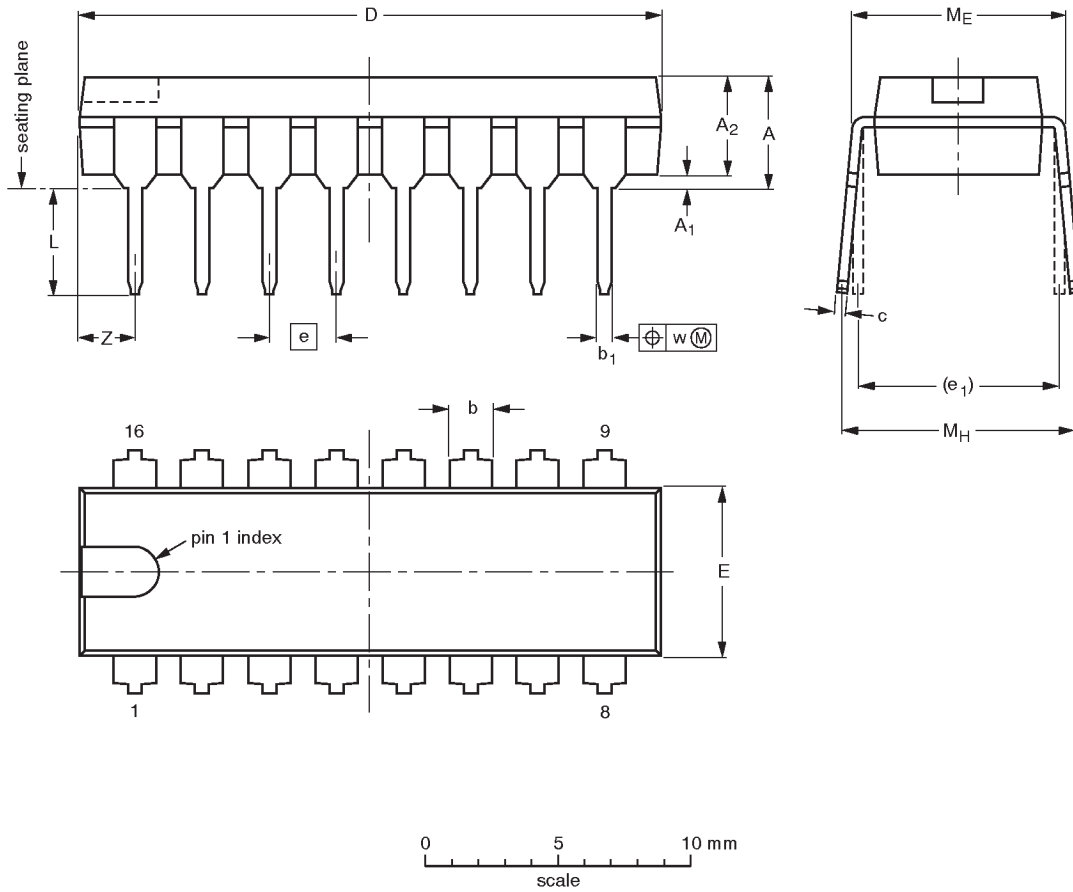


64-Bit TTL bipolar RAM, non-inverting (3-State)

74F219A

DIP16: plastic dual in-line package; 16 leads (300 mil); long body

SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				92-10-02 95-01-19

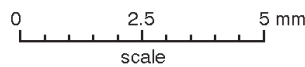
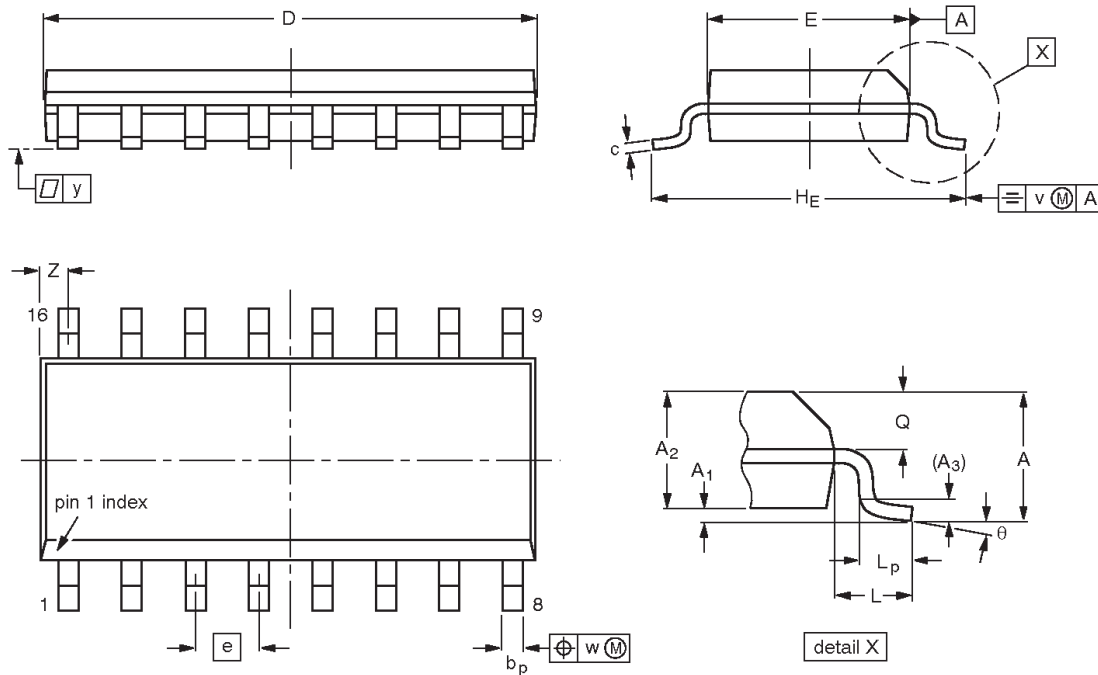


64-Bit TTL bipolar RAM, non-inverting (3-State)

74F219A

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45 0.049	0.25 0.36	0.49 0.19	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01 0.014	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

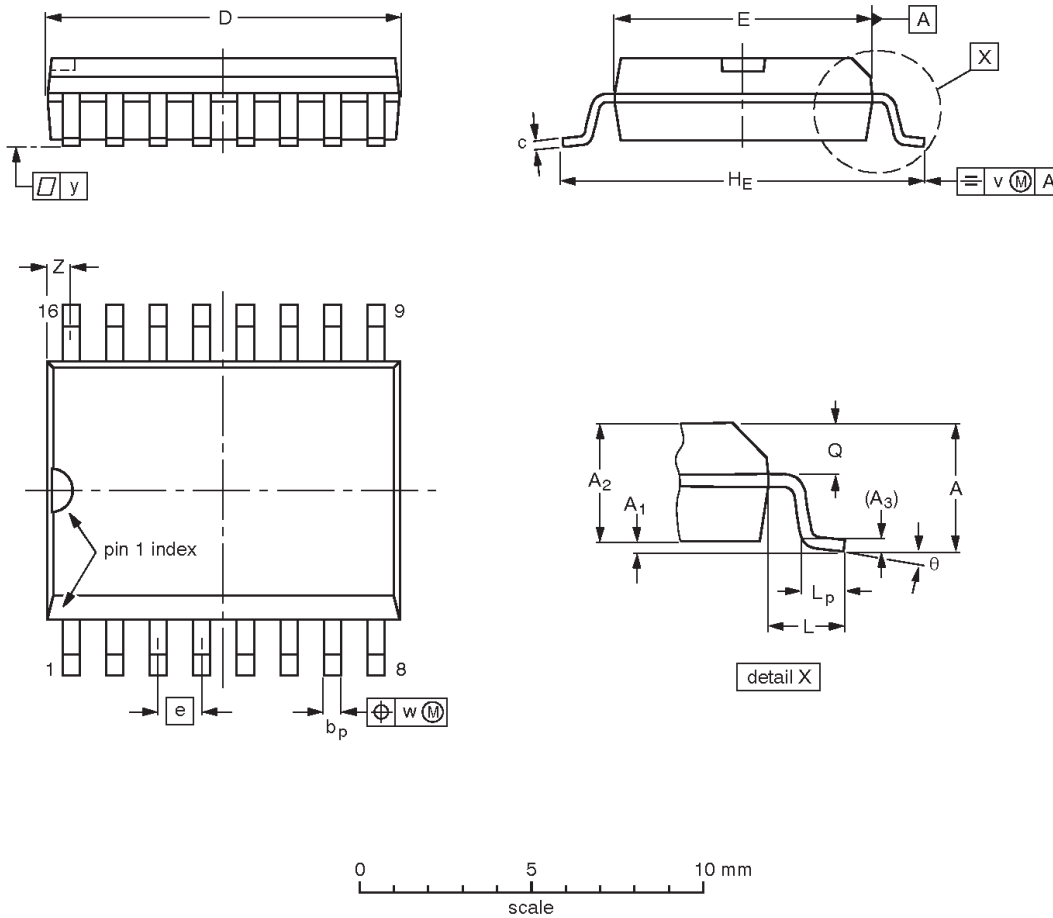
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

64-Bit TTL bipolar RAM, non-inverting (3-State)

74F219A

SO16: plastic small outline package; 16 leads; body width 7.5 mm

SOT162-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				95-01-24 97-05-22

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64-Bit TTL bipolar RAM, non-inverting (3-State)

74F219A

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**NOTES**

## 64-bit TTL bipolar RAM, non-inverting (3-State)

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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