DATA SHEET

74ALVCH16825 18-bit buffer/driver (3-State)

Product specification

1998 Jul 27

IC24 Data Handbook





18-bit buffer/driver (3-State)

74ALVCH16825

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTETM flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16825 is an 18-bit non-inverting buffer/driver with 3-State outputs for bus-oriented applications.

The 74ALVCH16825 consists of two 9-bit sections with separate output enable signals. For either 9-bit buffer section, the two output enable (1OE1 and 1OE2 or 2OE1 and 2OE2) inputs must both be LOW for corresponding D outputs to be active. If either output enable input is HIGH, the outputs of that 9-buffer section are in the high impedance state.

The 74ALVCH16825 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

PIN CONFIGURATION

	_		1	
1 0E 1	1	_	56	1 OE 2
1Y ₁	2		55	1A ₀
1Y ₁	3		54	1A ₁
GND	4		53	GND
1Y ₂	5		52	1A ₂
1Y ₃	6		51	1A ₃
V _{CC}	7		50	V _{CC}
1Y ₄	8		49	1A ₄
1Y ₅	9		48	1A ₅
1Y ₆	10		47	1A ₆
GND	11		46	GND
1Y ₇	12		45	1A ₇
1Y ₈	13		44	1A ₈
GND	14		43	GND
GND	15		42	GND
2Y ₀	16		41	2A ₀
2Y ₁	17		40	2A ₁
GND	18		39	GND
2Y ₂	19		38	2A ₂
2Y ₃	20		37	2A ₃
2Y ₄	21		36	2A ₄
V_{CC}	22		35	V _{CC}
2Y ₅	23		34	2A ₅
2Y ₆	24		33	2A ₆
GND	25		32	GND
2Y ₇	26		31	2A ₇
2Y ₈	27		30	2A ₈
2 0E 1	28		29	2 OE 2
	L		J	
			S	:H00139

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \le 2.5$ ns

OND - OV, Tame) - 20 0, 4 - 4 = 2:010				
SYMBOL	PARAMETER	CONDITION	NS	TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay CP to Qn	V _{CC} = 2.5V, C _L = 30pF V _{CC} = 3.3V, C _L = 50pF	2.0 2.0	ns	
C _I	Input capacitance			4.0	pF
C _{PD}	Power dissipation capacitance per latch	$V_1 = GND \text{ to } V_{CC}^1$	Output enabled	19	pF
CPD	ower dissipation capacitance per laten	VI = GIAD to AGG	Output disabled	3	1 PF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $\begin{aligned} &P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \Sigma \; (C_L \times V_{CC}{}^2 \times f_o) \; \text{where:} \; f_i = \text{input frequency in MHz;} \; C_L = \text{output load capacitance in pF;} \\ &f_o = \text{output frequency in MHz;} \; V_{CC} = \text{supply voltage in V;} \; \Sigma \; (C_L \times V_{CC}{}^2 \times f_o) = \text{sum of outputs.} \end{aligned}$

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DRAWING NUMBER
56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II	–40°C to +85°C	74ALVCH16825 DGG	ACH16825 DGG	SOT364-1

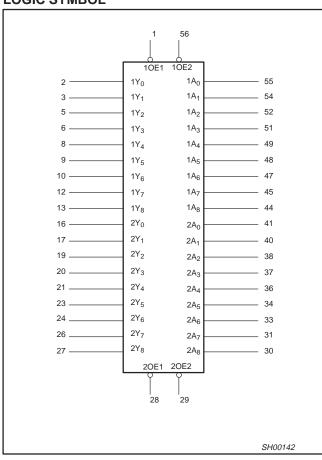
18-bit buffer/driver (3-State)

74ALVCH16825

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1 OE 1	Output enable input
56	1 OE 2	(active LOW)
55, 54, 52, 51, 49, 48, 47, 45, 44	1A0 to 1A8	Data inputs
2, 3, 5, 6, 8, 9, 10, 12, 13	1Y0 to 1Y8	Data outputs
4, 11, 14, 15, 18, 25, 32, 39, 42, 43, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V _{CC}	Positive supply voltage
28	2 0E 1	Output enable input
29	2 OE 2	(active LOW)
43, 42, 41, 40, 38, 37, 36, 34, 33, 31	2A0 to 2A8	Data inputs
16, 17, 19, 20, 21, 23, 24, 26, 27	2Y0 to 2Y8	Data outputs

LOGIC SYMBOL



FUNCTION TABLE

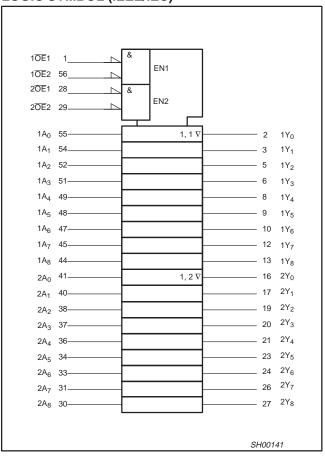
	INPUTS						
nOE1	nOE2	nOE2 A					
L	L	L	L				
L	L	Н	Н				
Н	Х	Х	Z				
Х	Н	Х	Z				

H = HIGH voltage level L = LOW voltage level

X = Don't care

Z = High impedance "off" state

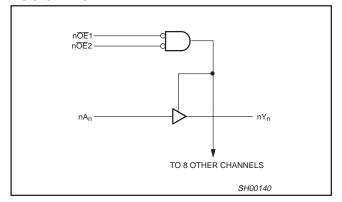
LOGIC SYMBOL (IEEE/IEC)



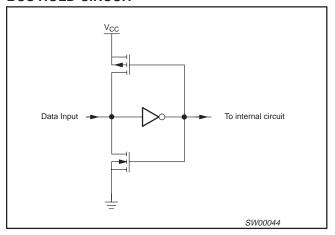
18-bit buffer/driver (3-State)

74ALVCH16825

LOGIC DIAGRAM



BUS HOLD CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
Vcc	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	V
VI	DC Input voltage range		0	V _{CC}	V
Vo	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _r , t _f	Input rise and fall times	$V_{CC} = 2.3 \text{ to } 3.0 \text{V}$ $V_{CC} = 3.0 \text{ to } 3.6 \text{V}$	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT		
V _{CC}	DC supply voltage		-0.5 to +4.6	V		
I _{IK}	DC input diode current	V _I < 0	- 50	mA		
\/	DC input voltage	For control pins ²	-0.5 to +4.6			
VI	DC input voltage	For data inputs ²	–0.5 to V _{CC} +0.5	V		
I _{OK}	DC output diode current	$V_{O} > V_{CC}$ or $V_{O} < 0$	±50	mA		
V _O	DC output voltage	Note 2	–0.5 to V _{CC} +0.5	V		
IO	DC output source or sink current	$V_O = 0$ to V_{CC}	±50	mA		
I _{GND} , I _{CC}	DC V _{CC} or GND current		± 100	mA		
T _{stg}	Storage temperature range		-65 to +150	°C		
P _{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850 600	mW		

NOTE:

^{1.} Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

18-bit buffer/driver (3-State)

74ALVCH16825

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

				LIMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	Temp :	= -40°C to +8	5°C	UNIT
			MIN	1.2 1.5 1.2 0.15 0.7 V _{CC} V _{CC} - 0.08 V _{CC} - 0.26 V _{CC} - 0.14 V _{CC} - 0.28 GND 0.07 0.15 0.14 0.27 0.1 8	MAX	1
.,		V _{CC} = 2.3 to 2.7V	1.7	1.2		,,
V_{IH}	HIGH level Input voltage	V _{CC} = 2.7 to 3.6V	2.0	1.5		V
.,	1000		1.2	0.7	,,	
V_{IL}	V _{IL} LOW level Input voltage	V _{CC} = 2.7 to 3.6V		1.5	0.8	· V
		$V_{CC} = 2.3 \text{ to } 3.6 \text{V}; V_{I} = V_{IH} \text{ or } V_{IL}; I_{O} = -100 \mu\text{A}$	V _{CC} -0.2	V _{CC}		
		$V_{CC} = 2.3V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -6$ mA	V _{CC} - 0.3	V _{CC} - 0.08		1
	V _{OH} HIGH level output voltage	$V_{CC} = 2.3V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} - 0.6	V _{CC} - 0.26		1 ,
VOH		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} - 0.5	V _{CC} - 0.14		٧
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -12mA$	V _{CC} - 0.6	V _{CC} - 0.09		1
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = -24$ mA	V _{CC} -1.0	V _{CC} - 0.28		1
		V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL} ; I_O = 100 μ A		GND	0.20	٧
		$V_{CC} = 2.3V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 6mA$		0.07	0.40	V
V_{OL}	LOW level output voltage	$V_{CC} = 2.3V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 12mA$		0.15	0.70	
		$V_{CC} = 2.7V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 12mA$		0.14	0.40	V
		$V_{CC} = 3.0V$; $V_I = V_{IH}$ or V_{IL} ; $I_O = 24$ mA		0.27	0.55	1
II	Input leakage current	V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND		0.1	5	μА
I _{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6V; V_I = V_{IH} or V_{IL} ; V_O = V_{CC} or GND		0.1	10	μА
I _{CC}	Quiescent supply current	$V_{CC} = 2.3 \text{ to } 3.6 \text{V}; V_{I} = V_{CC} \text{ or GND}; I_{O} = 0$		0.2	40	μΑ
Δl _{CC}	Additional quiescent supply current	$V_{CC} = 2.3V \text{ to } 3.6V; V_I = V_{CC} - 0.6V; I_O = 0$		150	750	μΑ
I _{BHL} ²	Bus hold LOW sustaining current	$V_{CC} = 2.3V; V_I = 0.7V$	45	-		μА
IBHL	Bus floid ESVV subtaining current	$V_{CC} = 3.0V; V_I = 0.8V$	75	150		μι
I _{BHH} ²	Bus hold HIGH sustaining current	$V_{CC} = 2.3V; V_I = 1.7V$	-45 -75	475		μΑ
	Puo hold I OW overdrive average	$V_{CC} = 3.0V; V_{I} = 2.0V$	-75 500	-175		
I _{BHLO} ²	Bus hold LICL everdrive current	$V_{CC} = 3.6V$	500			μΑ
I _{BHHO} ²	Bus hold HIGH overdrive current	V _{CC} = 3.6V	-500			μΑ

NOTES:

All typical values are at T_{amb} = 25°C.
 Valid for data inputs of bus hold parts.

18-bit buffer/driver (3-State)

74ALVCH16825

AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO 2.7V RANGE

 $GND = 0V; \ t_r = t_f \leq 2.0ns; \ C_L = 30pF$

				LIMITS		
SYMBOL	PARAMETER	WAVEFORM	V _{CC} = 2.3 to 2.7V		UNIT	
			MIN	TYP ¹	MAX	
t _{PHL} /t _{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.0	4.1	ns
t _{PZH} /t _{PZL}	3-State output enable time nOEn to nYn	2, 3	1.0	2.9	6.0	ns
t _{PHZ} /t _{PLZ}	3-State output disable time nOEn to nYn	2,3	1.2	2.2	5.6	ns

NOTE:

AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO 3.6V RANGE AND $V_{CC} = 2.7V$

GND = 0V; $t_r = t_f \le 2.5 \text{ns}$; $C_L = 50 \text{pF}$

				LIMITS			LIMITS		UNIT	
SYMBOL PARAMETER		WAVEFORM	V _C	$_{C}$ = 3.3 \pm 0.	3V		$V_{CC} = 2.7V$			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX		
t _{PHL} /t _{PLH}	Propagation delay nAn to nYn	1, 3	1.0	2.0	3.4	1.0	2.1	3.9	ns	
t _{PZH} /t _{PZL}	3-State output enable time nOEn to nYn	2, 3	1.0	2.8	4.7	1.0	2.9	5.7	ns	
t _{PHZ} /t _{PLZ}	3-State output disable time nOEn to nYn	2, 3	1.3	2.9	4.5	1.3	3.0	4.9	ns	

NOTES:

- 1. All typical values are measured $T_{amb} = 25$ °C.
- 2. Typical value is measured at $V_{CC} = 3.3V$

AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO 2.7V AND V_{CC} < 2.3V RANGE

 $V_{M} = 0.5 V_{CC}$ $V_{X} = V_{OL} + 0.15 V$

 $V_Y = V_{OH} - 0.15V$ V_{OL} and V_{OH} are the typical output voltage drop that occur with the

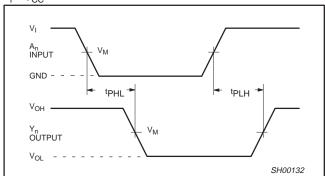
AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO 3.6V AND $V_{CC} = 2.7V RANGE$

 $V_{M} = 1.5 \text{ V}$ $V_{X} = V_{OL} + 0.3 \text{V}$

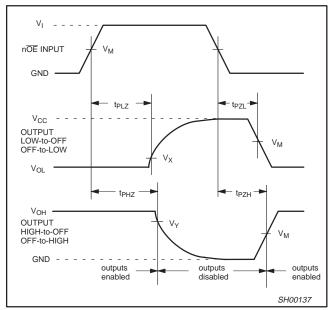
 $V_{Y} = V_{OH} - 0.3V$

 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

 $\frac{V_{I}}{V_{I}} = 2.7V$ $\frac{V_{I}}{V_{I}} = V_{CC}$



Waveform 1. Input (Dn) to output (Yn) propagation delay



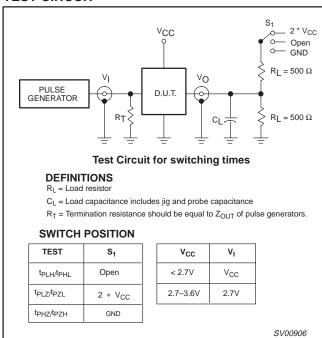
Waveform 2. 3-State enable and disable times

^{1.} All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

18-bit buffer/driver (3-State)

74ALVCH16825

TEST CIRCUIT



Waveform 3. Load circuitry for switching times

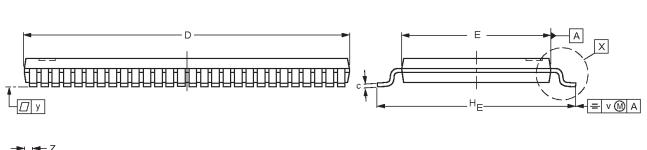
1998 Jul 27 7

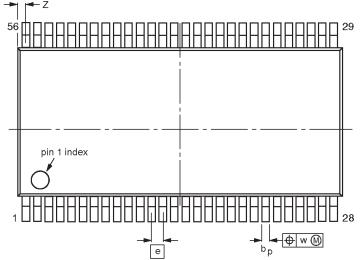
18-bit buffer/driver (3-State)

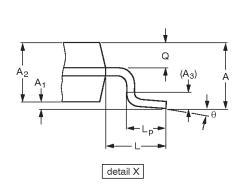
74ALVCH16825

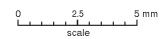
TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1









DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE REFERENCES				EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT364-1		MO-153EE				-93-02-03- 95-02-10

18-bit buffer/driver (3-State)

74ALVCH16825

NOTES

18-bit buffer/driver (3-State)

74ALVCH16825

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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^[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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