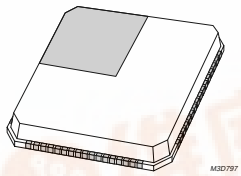


PIP250M

Integrated buck converter

Rev. 02 — 21 February 2003 Product data

1. Description

The PIP250M is a fully integrated synchronous buck converter intended for use as a point-of-load regulator. It contains two N-channel power MOSFETs, a Schottky diode and a voltage mode, pulse width modulated (PWM) controller. The controller features include overcurrent and overvoltage protection and undervoltage lockout functions. By combining the power components and the controller into a single component, stray inductances are virtually eliminated, resulting in lower switching losses and a compact, efficient design with minimal external component count.

2. Features

- Output current up to 15 A
- Single supply 5 V operation
- Fixed 300 kHz operating frequency
- Voltage mode control
- Minimum regulated output voltage 0.8 V
- Internal soft start
- Overcurrent protection
- Overvoltage protection
- Remote sensing.

3. Applications

- High-current point-of-load regulation
- Distributed power architectures
- Multiple output telecom power supplies
- Microprocessor and Digital Signal Processing (DSP) supplies
- Computer peripheral supplies
- Cable modems
- Set-top boxes.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PIP250M	HVQFN68	plastic, thermal enhanced very thin quad flat package; no leads; 68 terminals; body 10 × 10 × 0.85 mm	SOT687-1

PHILIPS

5. Block diagram

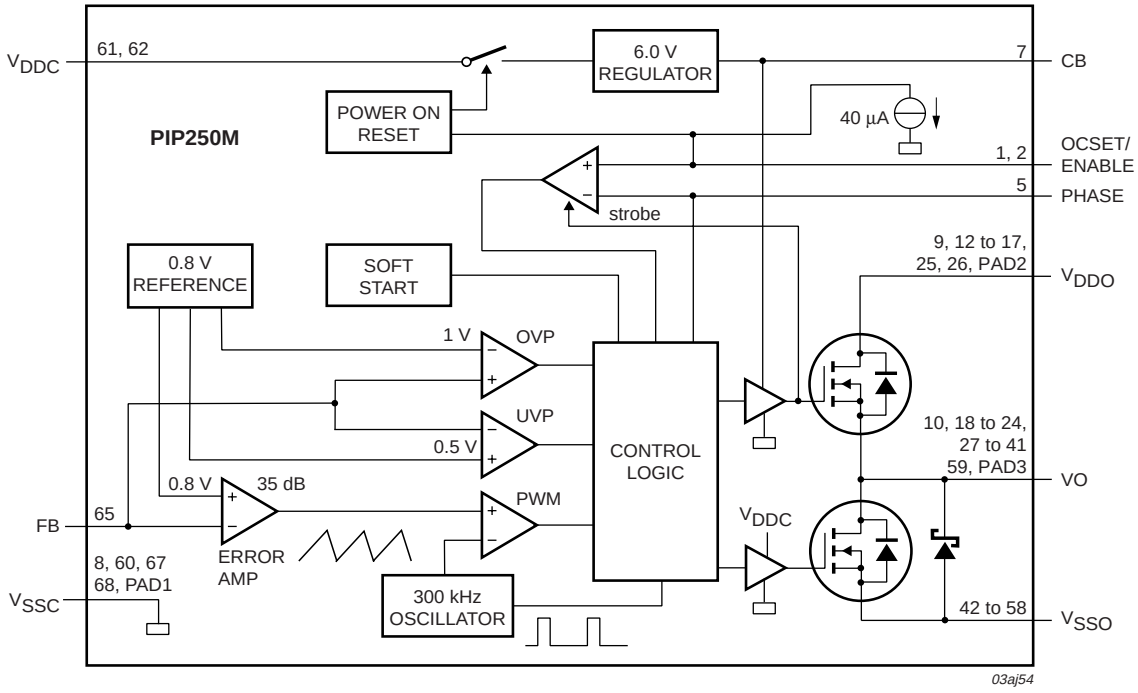
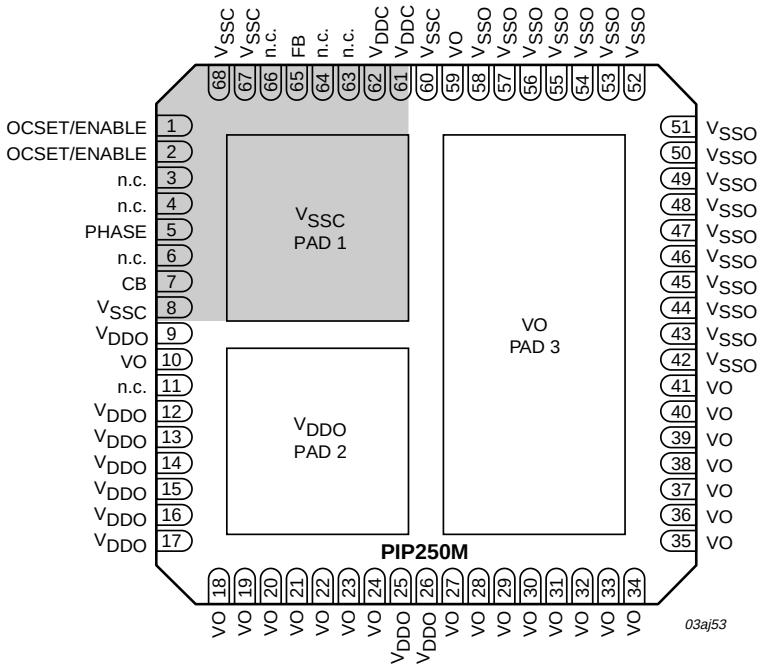


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



Grey area denotes terminal 1 index area.

Fig 2. Pin configuration (footprint view).

6.2 Pin description

Table 2: Pin description

Symbol	Pin		I/O	Description
V_{DDO}	9, 12 to 17, 25, 26, PAD2	[1]	-	output stage supply voltage
V_{SSO}	42 to 58		-	output stage ground
V_{DDC}	61, 62		-	control circuit supply voltage
V_{SSC}	8, 60, 67, 68, PAD1	[1]	-	control circuit ground
VO	10, 18 to 24, 27 to 41, 59, PAD3	[1]	O	output
CB	7		I/O	bootstrap capacitor connection
PHASE	5		I	sense connection for current limit
OCSET/ ENABLE	1, 2		I	current limit set and enable input
FB	65		I	feedback input
n.c.	3, 4, 6, 11, 63, 64, 66	[2]	-	no internal connection

[1] PAD1, PAD2 and PAD3 are electrical connections and must be soldered to the printed circuit board

[2] All n.c. pins should be connected to V_{SSC}.

7. Functional description

7.1 Pin functions

7.1.1 Output stage supply (V_{DDO}, V_{SSO})

The power output stage of the PIP250M consists of two N-channel, power MOSFETs and a Schottky diode configured as a synchronous buck converter. The drain of the upper MOSFET is connected to the positive conversion supply (V_{DDO}), and the source of the lower MOSFET is connected to power ground (V_{SSO}). The Schottky diode is connected between the source and drain of the lower MOSFET.

7.1.2 Output voltage (VO)

VO is the switched node of the power MOSFET output stage. This node is connected internally to the source of the upper MOSFET and the drain of the lower MOSFET.

7.1.3 Control circuit supply (V_{DDC}, V_{SSC})

V_{DDC} is the positive supply to the control circuit. V_{SSC} is the control circuit ground. All control voltages are measured with respect to V_{SSC}.

7.1.4 Bootstrap capacitor connection (CB)

The upper MOSFET driver stage is powered from the CB pin.

7.1.5 Voltage feedback pin (FB)

The FB pin is connected to the inverting input of the error amplifier, and to the inputs of the overvoltage and undervoltage comparators.

7.1.6 Current limit set and enable input (OCSET/ENABLE)

The overcurrent threshold is set by an external resistor between V_{DDO} and OCSET/ENABLE. The PIP250M can be shut down by pulling this pin LOW.

7.1.7 Sense connection for current limit (PHASE)

The PHASE input is normally connected externally to the power output stage switched node (VO). The voltage on the PHASE input is compared with the voltage on the OCSET/ENABLE input during the interval when the upper MOSFET is on. The overcurrent trip operates if the voltage on the PHASE input is lower than the voltage on the OCSET/ENABLE input.

7.2 Operation

7.2.1 Single supply operation

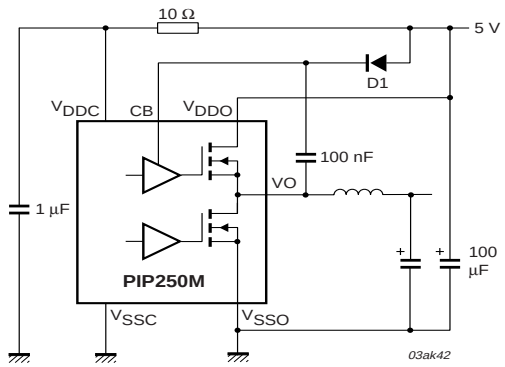


Fig 3. Single supply operation.

Operation of the PIP250M from a single 5 V conversion supply is shown in Figure 3. The upper MOSFET gate driver stage is supplied from the CB pin. An external bootstrap circuit, comprising D1 and the 100 nF capacitor generates a voltage on CB of twice V_{DDO}.

The control circuit supply, V_{DDC} is protected from transients by a low pass filter comprising a 10 Ω resistor and a 1 µF capacitor. These components should be placed close to the device pins.

7.2.2 Regulated output voltage

The reference voltage of the PIP250M is 0.8 V. The regulated output voltage is set using a resistive divider as shown in Figure 9. The resistors should be placed as close as possible to the FB pin. Both resistors should be less than 1 kΩ in order to avoid noise coupling. The 68 nF capacitor across the upper resistor improves the control loop stability by adding a small amount of phase margin.

7.2.3 Power on reset

The PIP250M control circuit powers up when the voltage on V_{DDC} rises above the start-up threshold voltage (typically 4.1 V). The control circuit stops operating when the voltage on V_{DDC} falls below the power-down threshold voltage (typically 3.6 V).

Once the voltage on V_{DDC} is above the start-up threshold voltage, the PIP250M does not produce pulses until the voltage on OCSET/ENABLE rises above the OCSET/ENABLE start-up threshold voltage (typically 1.25 V).

7.2.4 Soft start

The soft start sequence prevents surge currents being drawn from the conversion supply when the PIP250M is powered up into a high current load. The soft start sequence is controlled by an internal digital counter. During the soft start sequence, the reference voltage on the non inverting input of the error amplifier is increased from zero up to the normal operating level of 0.8 V. The duration of the soft start sequence is typically 2 ms.

7.2.5 Overcurrent protection

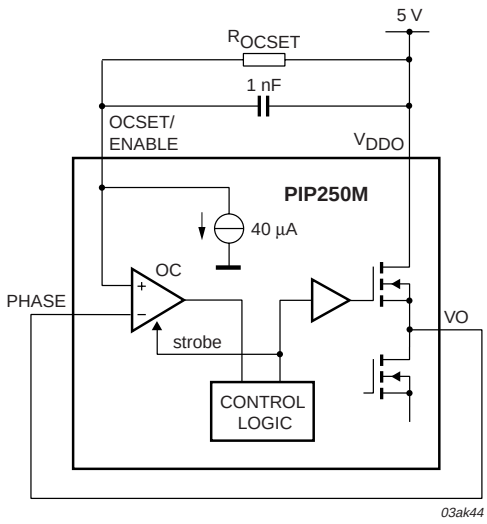


Fig 4. Overcurrent protection.

The overcurrent protection function is shown in Figure 4. The overcurrent trip function is enabled when the upper MOSFET gate drive signal is HIGH.

During this interval, the voltage on the PHASE input is compared with the voltage on the OCSET/ENABLE input. If the voltage on the PHASE input is lower than the voltage on the OCSET/ENABLE input, then the PIP250M detects an overcurrent trip condition and turns off the gate drive to the upper MOSFET. There is an internal filter with a time constant of 30 µs in series with the PHASE input. Since the switching frequency is 300 kHz, this means that the overcurrent trip operates if the overcurrent condition persists for10 switching cycles.

If three overcurrent pulses are detected, the PIP250M latches off and produces no more pulses until it has been reset. To reset the PIP250M, the supply voltage (V_{DDC}) must be reduced below the power down reset threshold and then increased back up to 5 V.

An external resistor (R_{OCSET}) sets the overcurrent trip level. Figure 5 shows the overcurrent trip level (I_{TRIP}) as a function of R_{OCSET}.

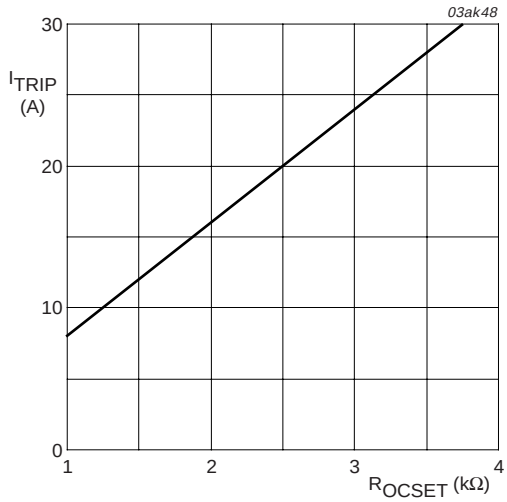


Fig 5. Overcurrent trip level as a function of R_{OCSET}.

7.2.6 Undervoltage and overvoltage protection

With reference to Figure 1, the FB pin is connected internally to the overvoltage and undervoltage comparators, labelled OVP and UVP respectively. In normal operation, the voltage on FB is regulated at 0.8 V.

If the voltage on FB exceeds the overvoltage protection (OVP) threshold (1 V) for longer than 30 μs, an overvoltage condition is detected, the gate drive signals to the MOSFETs are disabled, and the PIP250M latches off. To reset the latch, the PIP250M must be powered down by reducing V_{DDC} below the power down reset threshold and then increasing V_{DDC} back up to 5 V.

If the voltage on FB drops below the undervoltage protection (UVP) threshold (0.5 V) for longer than 30 μs, then an undervoltage condition is detected and the gate drive signals to the MOSFET drivers are turned off. If three undervoltage pulses are detected then the PIP250M latches off. To reset the PIP250M, the supply voltage (V_{DDC}) must be reduced below the power down reset threshold and then increased back up to 5 V.

8. Limiting values

Table 3: Limiting values

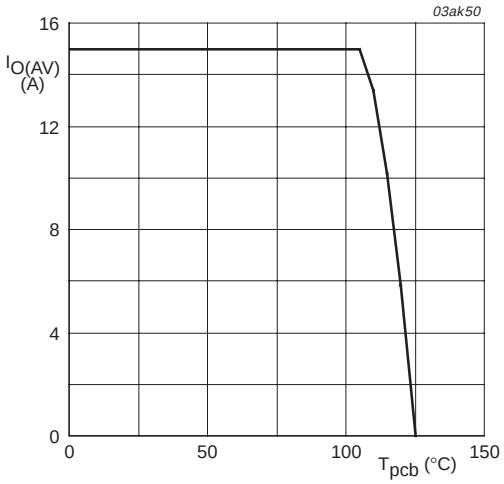
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDC}	control circuit supply voltage			–0.3	+7	V
V_{DDO}	output stage supply voltage			–0.3	+7	V
V_{PHASE}	input voltage on PHASE			–0.3	+7	V
V_{OCSET}	input voltage on OCSET			–0.3	+7	V
V_{FB}	input voltage on FB			–0.3	+7	V
V_O	output voltage			–0.3	$+V_{DDO}$ + 0.3	V
V_{CB}	bootstrap voltage			–0.3	+15	V
$I_{O(AV)}$	average output current	$T_{pcb} \leq 110$ °C; Figure 6		-	15	A
I_{ORM}	repetitive peak output current	$t_p \leq 10$ µs; duty cycle ≤ 0.075	[1]	-	200	A
P_{tot}	total power dissipation	T_{pcb} = 25 °C	[2]	-	20	W
		T_{pcb} = 90 °C	[2]	-	7	W
T_j	junction temperature			–40	+125	°C
T_{stg}	storage temperature			–55	+150	°C
V_{esd}	electrostatic discharge voltage	human body model; C = 100 pF; R = 1500 Ω		-	2	kV
		machine model; C = 200 pF; R = 10 Ω; L = 0.75 µH	[3]	-	200	V

[1] Pulse width and repetition rate limited by maximum value of T_j.

[2] Assumes a thermal resistance from junction to printed-circuit board of 5 K/W

[3] The PIP250M meets class 2 for Human Body Model and class M3 for Machine Model.



Circuit of Figure 9; V_{DDC} = 5 V; V_{DDO} = 5 V; V_O = 2.5 V.

Fig 6. Average output current as a function of printed-circuit board temperature.

9. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}pcb)}$	thermal resistance from junction to printed-circuit board		-	4	5	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	device mounted on FR4 printed-circuit board; copper area around device 25 × 25 mm				
		no thermal vias	-	25	-	K/W
		with thermal vias	-	20	-	K/W
		with thermal vias and forced air cooling; airflow = 0.8 ms^{-1} (150 LFM)	-	15	-	K/W
$R_{th(j\text{-}c)}$	thermal resistance from junction to case	measured on upper surface of package.	-	11	-	K/W

10. Characteristics

Table 5: Characteristics

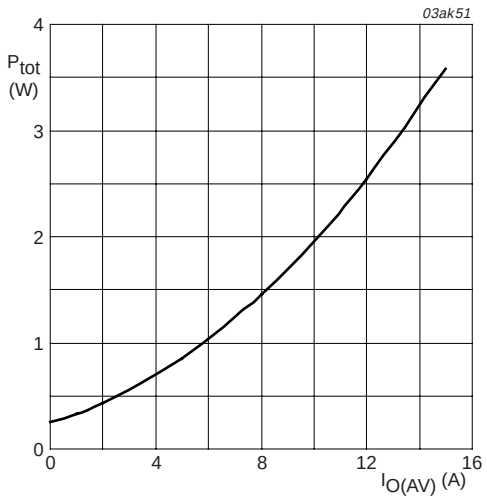
V_{DDC} = 5 V; T_{amb} = 25 °C; circuit of Figure 9 unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Control circuit supply						
V_{DDC}	control circuit supply voltage	–40 °C ≤ T_j ≤ +125 °C	-	5	-	V
I_{DDC}	control circuit supply current		-	24	-	mA
Power dissipation						
P_{tot}	power dissipation	V_{DDC} = 5 V; V_{DDO} = 5 V; V_O = 2.5 V; $I_{O(AV)}$ = 15 A; Figure 7	-	3.6	-	W
η	efficiency	V_{DDC} = 5 V; V_{DDO} = 5 V; V_O = 2.5 V; $I_{O(AV)}$ = 15 A; Figure 8	-	88	-	%
Power-on Reset						
$V_{DDC(th)su}$	start-up threshold control circuit supply voltage	V_{DDC} increasing; V_{OCSET} = 4.5 V	3.85	4.1	4.35	V
$V_{DDC(th)sd}$	shut-down threshold control circuit supply voltage	V_{DDC} decreasing; V_{OCSET} = 4.5 V	3.25	3.7	3.98	V
V_{hys}	hysteresis	V_{OCSET} = 4.5 V	0.3	0.5	0.7	V
$V_{OCSET(th)su}$	start-up threshold voltage OCSET	V_{OCSET} increasing	0.8	1.25	2.0	V
Reference						
$V_{i(ref)FB}$	reference voltage	measured at FB pin	0.78	0.8	0.82	V
Oscillator						
f_{osc}	oscillator frequency		250	300	350	kHz
$V_{osc(p\text{-}p)}$	oscillator ramp amplitude (peak-to-peak value)		-	1.75	-	V

Table 5: Characteristics *...continued*

V_{DDC} = 5 V; T_{amb} = 25 °C; circuit of Figure 9 unless otherwise specified.

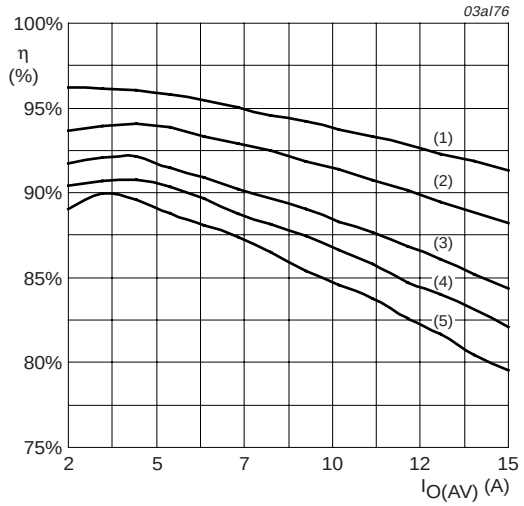
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Error amplifier						
G_{ol}	open loop gain		-	35	-	dB
GB	Gain bandwidth product		-	17	-	MHz
Overvoltage, overcurrent and undervoltage protection						
$V_{FB(th)OV}$	overvoltage threshold feedback voltage	voltage on FB increasing	1.0	1.1	-	V
$V_{FB(th)UV}$	undervoltage threshold feedback voltage	voltage on FB decreasing	-	0.5	0.6	V
I_{OCSET}	OCSET sink current	V_{OCSET} = 4.5 V	35	40	45	µA
$t_{D(OC)}$	overcurrent trip delay		-	30	-	µs
$t_{D(UV)}$	undervoltage trip delay		-	30	-	µs
t_{SS}	soft start interval		-	2	-	ms



See circuit of Figure 9.

V_{DDC} = 5 V; V_{DDO} = 5 V; V_O = 2.5 V

Fig 7. Total power dissipation as a function of average output current; typical values.



See circuit of Figure 9.

(1) V_O = 3.3 V

(2) V_O = 2.5 V

(3) V_O = 1.8 V

(4) V_O = 1.5 V

(5) V_O = 1.2 V

Fig 8. Total solution efficiency as a function of average output current; typical values.

11. Application information

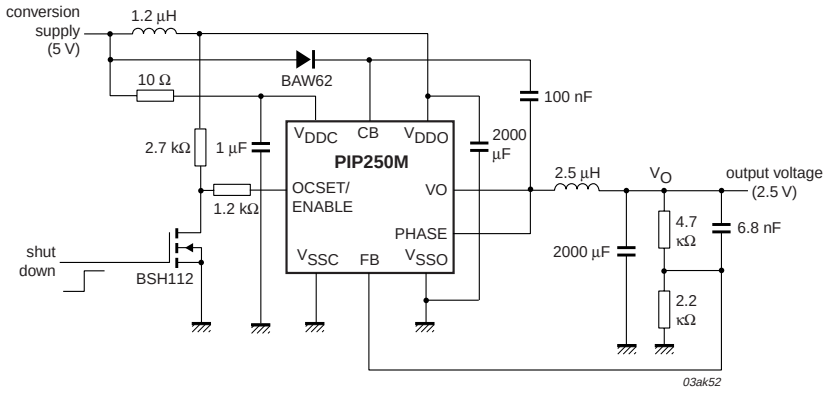
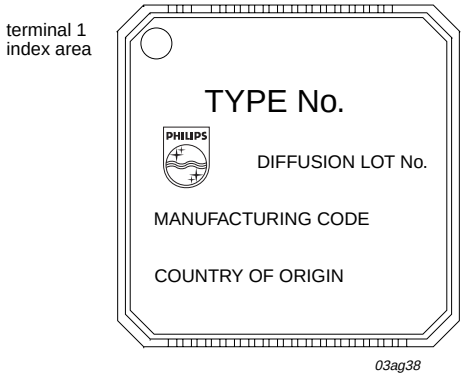


Fig 9. Typical application circuit.

12. Marking



TYPE No: PIP250M-NN (NN is version number)

DIFFUSION LOT No: 7 characters

MANUFACTURING CODE: see Figure 11

COUNTRY OF ORIGIN: Korea

Fig 10. SOT687-1 marking.

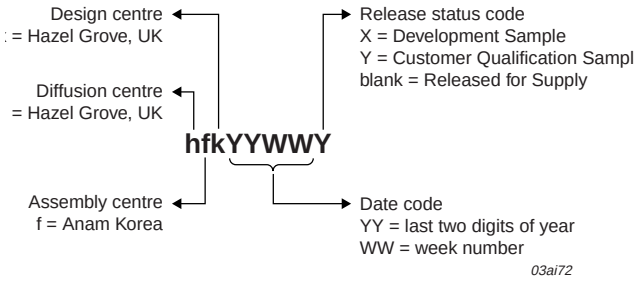
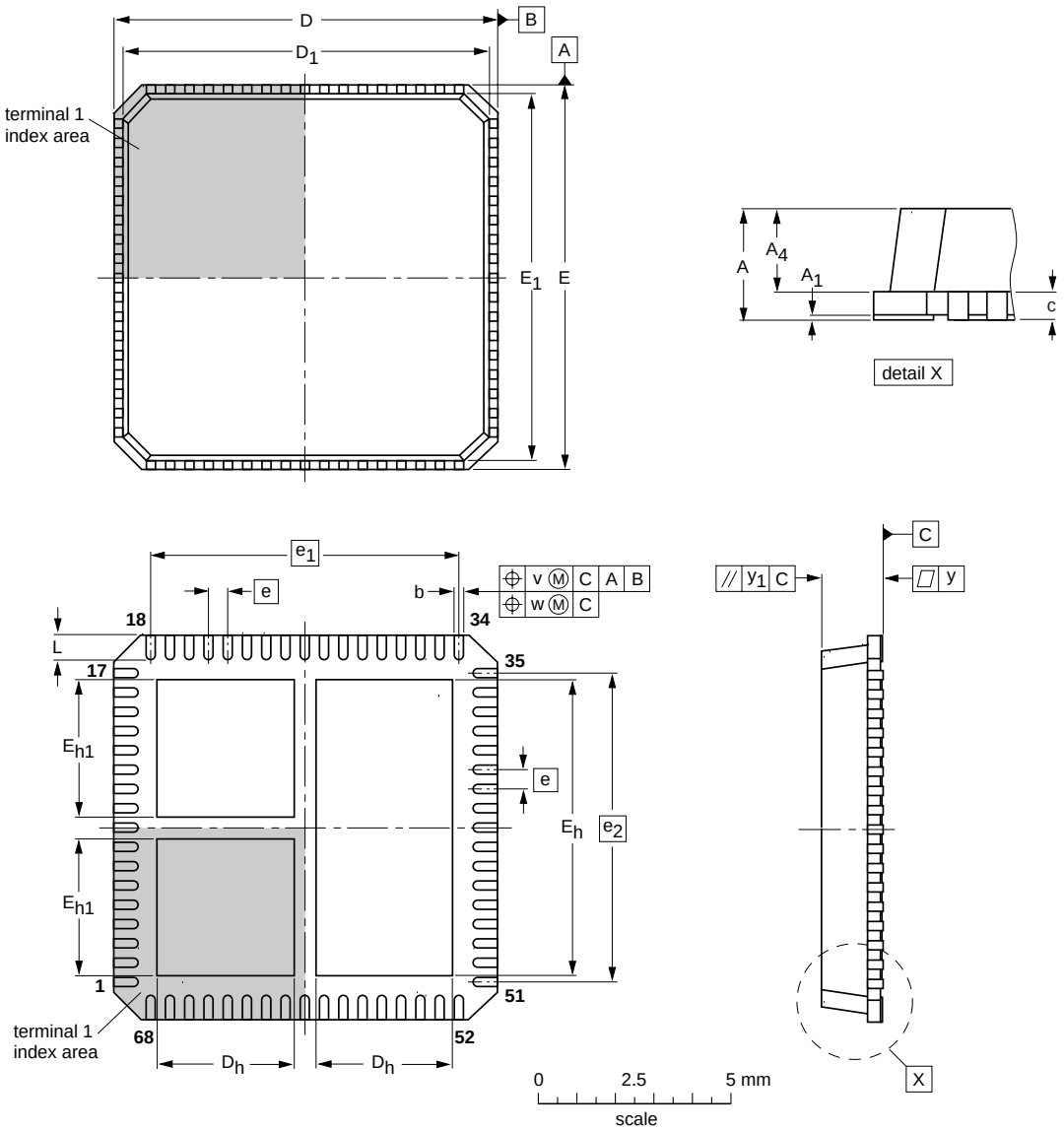


Fig 11. Interpretation of manufacturing code.

13. Package outline

HVQFN68: plastic thermal enhanced very thin quad flat package; no leads; 68 terminals; body 10 x 10 x 0.85 mm **SOT687-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_4	b	c	D	D_1	D_h	E	E_1	E_h	E_{h1}	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.80 0.65	0.30 0.18	0.2	10.15 9.85	9.95 9.55	3.8 3.5	10.15 9.85	9.95 9.55	7.85 7.55	3.8 3.5	0.5	8	8	0.75 0.50	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT687-1	- - -	MO-220	- - -			~~02-04-24~~ 02-10-18

Fig 12. SOT687-1.

14. Soldering

14.1 Introduction to soldering HVQFN packages

The HVQFN package is a near Chip Scale Package (CSP) with a copper lead frame. It is a leadless package, where electrical contact to the printed circuit board is made through metal pads on the underside of the package. In addition to the small pads around the periphery of the package, there are large pads on the underside that provide low thermal resistance, low electrical resistance, low inductance connections between the power components inside the package and the PCB. It is this feature of the HVQFN package that makes it ideally suited for low voltage, high current DC to DC converter applications.

Electrical connection between the package and the printed circuit board is made by printing solder paste on the printed circuit board, placing the component and reflowing the solder in a convection or infra-red oven. The solder reflow process is shown in Figure 13 and the typical temperature profile is shown in Figure 14. To ensure good solder joints, the peak temperature T_p should not exceed 220° C, and the time above liquidus temperature should be less than 1.25 minutes. The ramp rate during preheat should not exceed 3 K/s. Nitrogen purge is recommended during reflow.

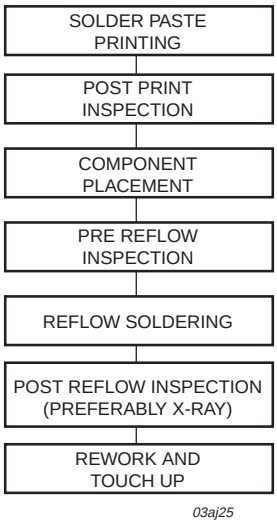


Fig 13. Typical reflow soldering process flow.

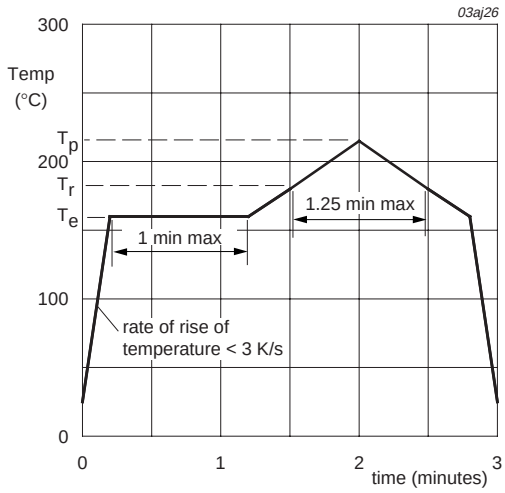


Fig 14. Typical reflow soldering temperature profile.

14.2 Rework guidelines

Since the solder joints are largely inaccessible, only the side fillets can be touched up. If there are defects underneath the package, then the whole package has to be removed.

The first step in component removal is to reflow the solder joints. It is recommended that the board is heated from the underside using a convective heater whilst hot air or gas is directed at the upper surface of the component. Nozzles should be used to direct the hot air or gas to minimize heating of adjacent components. Excessive airflow should be avoided since this may cause the package to skew. An airflow of 15 to 20 liters per minute is usually adequate.

Once the solder joints have reflowed, the component should be lifted off the board using a vacuum pen.

The next step is to clean the solder pads using solder braid and a blade shaped soldering tool. Finally, the pads should be cleaned with a solvent. The solvent is usually specific to the type of solder paste used in the original assembly and the paste manufacturers recommendations should be followed.

15. Mounting

15.1 PCB design guidelines

The terminals on the underside of the package are rectangular in shape with a rounded edge on the inside. Electrical connection between the package and the printed-circuit board is made by printing solder paste onto the PCB footprint followed by component placement and reflow soldering. The PCB footprint shown in Figure 15 is designed to form reliable solder joints.

The use of solder resist between each solder land is recommended. PCB tracks should not be routed through the corner areas shown in Figure 15. This is because there is a small, exposed remnant of the lead frame in each corner of the package, left over from the cropping process.

Good surface flatness of the PCB lands is desirable to ensure accuracy of placement after soldering. Printed-circuit boards that are finished with a roller tin process tend to leave small lumps of tin in the corners of each land. Levelling with a hot air knife improves flatness. Alternatively, an electro-less silver or silver immersion process produces completely flat PCB lands.

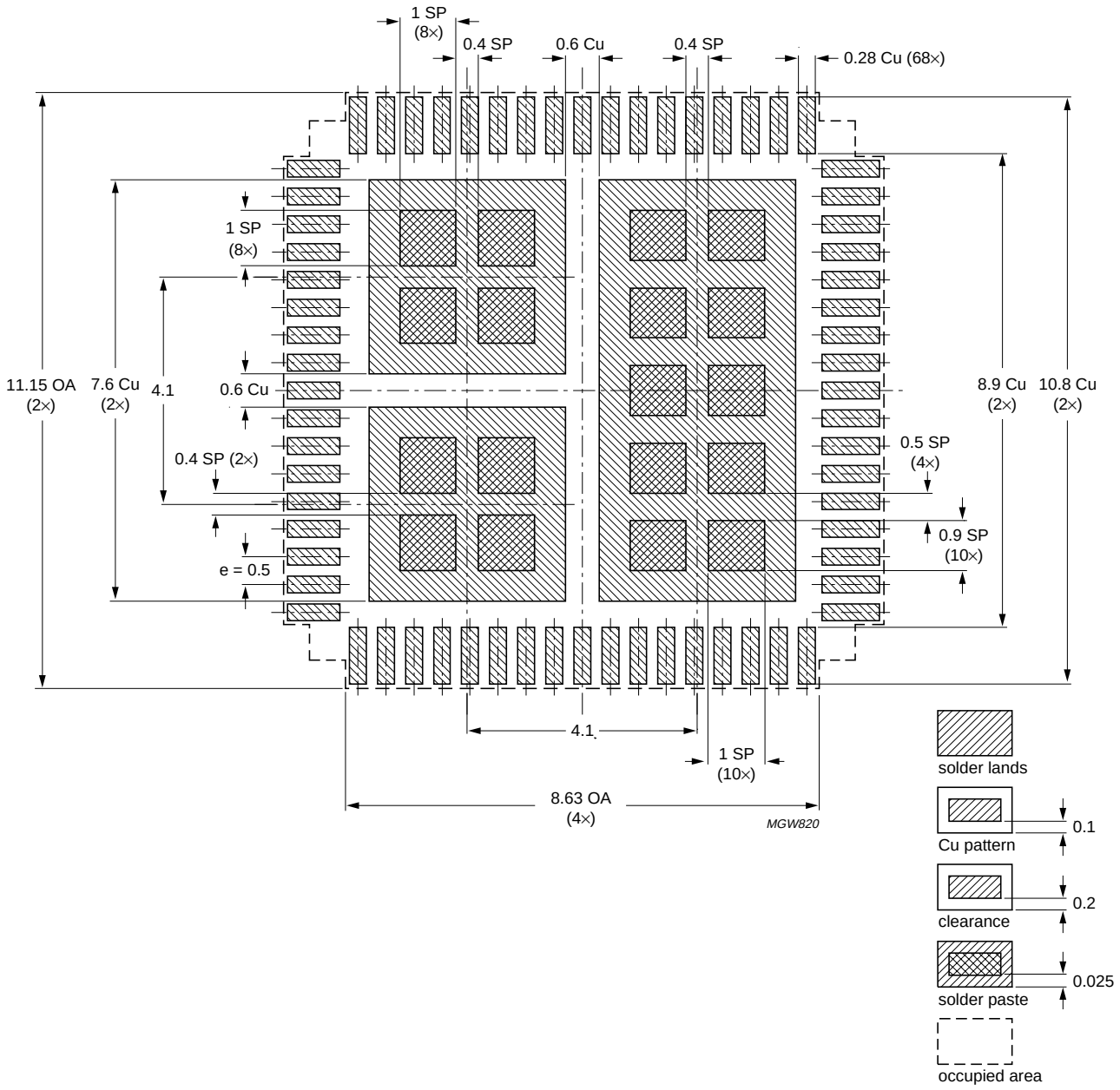


Fig 15. PCB footprint for SOT687-1 package (reflow soldering).

15.2 Solder paste printing

The process of printing the solder paste requires care because of the fine pitch and small size of the solder lands. A stencil thickness of 0.125 mm is recommended. The stencil apertures can be made the same size as the PCB lands in Figure 15.

The type of solder paste recommended for HVQFN packages is “No clean”, Type 3, due to the difficulty of cleaning flux residues from beneath the package.

16. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	**20030221**	**-**	**Product data (9397 750 10904)** Modifications: • Table 2: Pin description OCSET changed to OCSET/ENABLE • Section 7: – Dual supply operation deleted – Regulated output voltage section added – Overcurrent protection description clarified – Figure 5 revised • Table 5: – Typical value of I_{DDC} changed from 20 mA to 24 mA – Efficiency added • Figure 8 added.
01	**20021018**	**-**	**Objective data (9397 750 10579)**

17. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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9397 750 10904

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Date of release: 21 February 2003 **Document order number: 9397 750 10904**