DATA SHEET

TDA8926
Power stage 2 × 50 W class-D audio amplifier

Preliminary specification
Supersedes data of 2002 Feb 07

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Philips Semiconductors

PHILIPS

CONTENTS

Power stage 2 × 50 W class-D audio amplifier

TDA8926

1 FEATURES

- High efficiency (>94%)
- Operating voltage from ±15 to ±30 V
- Very low quiescent current
- High output power
- Short-circuit proof across the load, only in combination with controller TDA8929T
- Diagnostic output
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Electrostatic discharge protection (pin to pin)
- Thermally protected, only in combination with controller TDA8929T.

2 APPLICATIONS

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters).

3 GENERAL DESCRIPTION

The TDA8926 is the switching power stage of a two-chip set for a high efficiency class-D audio power amplifier system. The system is split into two chips:

- TDA8926J: a digital power stage in a DBS17P power package
- TDA8929T: the analog controller chip in a SO24 package.

With this chip set a compact 2 × 50 W audio amplifier system can be built, operating with high efficiency and very low dissipation. No heatsink is required, or depending on supply voltage and load, a very small one. The system operates over a wide supply voltage range from ±15 up to ±30 V and consumes a very low quiescent current.

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
General; V_P = ±25 V						
V_P	supply voltage		±15	±25	±30	V
$I_{q(tot)}$	total quiescent current	no load connected	–	35	45	mA
η	efficiency	P_o = 30 W	–	94	–	%
Stereo single-ended configuration						
P_o	output power	R_L = 8 Ω; THD = 10%; V_P = ±25 V	30	37	–	W
		R_L = 4 Ω; THD = 10%; V_P = ±21 V	40	50	–	W
Mono bridge-tied load configuration						
P_o	output power	R_L = 8 Ω; THD = 10%; V_P = ±21 V	80	100	–	W

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8926J	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6 BLOCK DIAGRAM

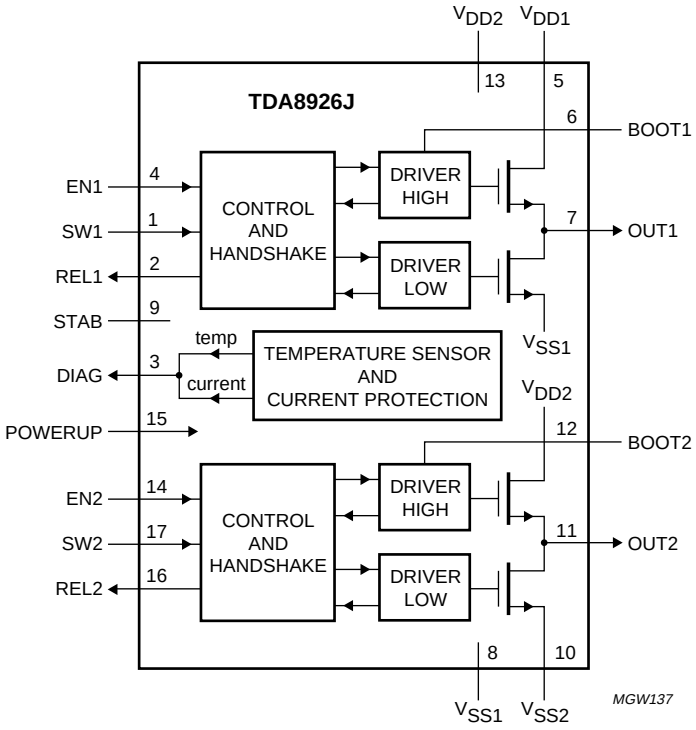


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
SW1	1	digital switch input; channel 1
REL1	2	digital control output; channel 1
DIAG	3	digital open-drain output for overtemperature and overcurrent report
EN1	4	digital enable input; channel 1
V_{DD1}	5	positive power supply; channel 1
BOOT1	6	bootstrap capacitor; channel 1
OUT1	7	PWM output; channel 1
V_{SS1}	8	negative power supply; channel 1
STAB	9	decoupling internal stabilizer for logic supply
V_{SS2}	10	negative power supply; channel 2
OUT2	11	PWM output; channel 2
BOOT2	12	bootstrap capacitor; channel 2
V_{DD2}	13	positive power supply; channel 2
EN2	14	digital enable input; channel 2
POWERUP	15	enable input for switching on internal reference sources
REL2	16	digital control output; channel 2
SW2	17	digital switch input; channel 2

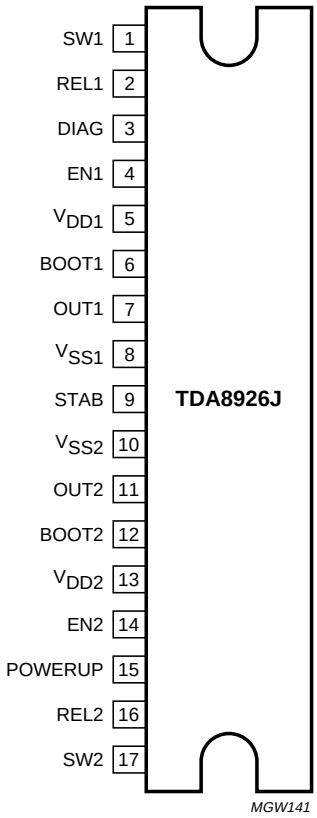


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

The combination of the TDA8926J and the TDA8929T controller produces a two-channel audio power amplifier system using the class-D technology (see Fig.3). In the TDA8929T controller the analog audio input signal is converted into a digital Pulse Width Modulation (PWM) signal.

The power stage TDA8926 is used for driving the low-pass filter and the loudspeaker load. It performs a level shift from the low-power digital PWM signal, at logic levels, to a high-power PWM signal that switches between the main supply lines. A 2nd-order low-pass filter converts the PWM signal into an analog audio signal across the loudspeaker.

For a description of the controller, see data sheet *"TDA8929T, Controller class-D audio amplifier"*.

8.1 Power stage

The power stage contains the high-power DMOS switches, the drivers, timing and handshaking between the power switches and some control logic. For protection, a temperature sensor and a maximum current detector are built-in on the chip.

For interfacing with the controller chip the following connections are used:

- Switch (pins SW1 and SW2): digital inputs; switching from V_{SS} to V_{SS} + 12 V and driving the power DMOS switches
- Release (pins REL1 and REL2): digital outputs; switching from V_{SS} to V_{SS} + 12 V; follow SW1 and SW2 with a small delay
- Enable (pins EN1 and EN2): digital inputs; at a level of V_{SS} the power DMOS switches are open and the PWM outputs are floating; at a level of V_{SS} + 12 V the power stage is operational and controlled by the switch pin if pin POWERUP is at V_{SS} + 12 V
- Power-up (pin POWERUP): must be connected to a continuous supply voltage of at least V_{SS} + 5 V with respect to V_{SS}
- Diagnostics (pin DIAG): digital open-drain output; pulled to V_{SS} if the temperature or maximum current is exceeded.

8.2 Protection

Temperature and short-circuit protection sensors are included in the TDA8926. The protection circuits are operational only in combination with the controller TDA8929T. In the event that the maximum current or maximum temperature is exceeded the diagnostic output is activated. The controller has to take appropriate measures by shutting down the system.

8.2.1 OVERTEMPERATURE

If the junction temperature (T_j) exceeds 150 °C, then pin DIAG becomes LOW. The diagnostic pin is released if the temperature is dropped to approximately 130 °C, so there is a hysteresis of approximately 20 °C.

8.2.2 SHORT-CIRCUIT ACROSS THE LOUDSPEAKER TERMINALS

When the loudspeaker terminals are short-circuited this will be detected by the current protection. If the output current exceeds the maximum output current of 5 A, then pin DIAG becomes LOW. The controller should shut down the system to prevent damage. Using the controller TDA8929T the system is shut down within 1 μs, and after 220 ms it will attempt to restart the system again. During this time the dissipation is very low, therefore the average dissipation during a short circuit is practically zero.

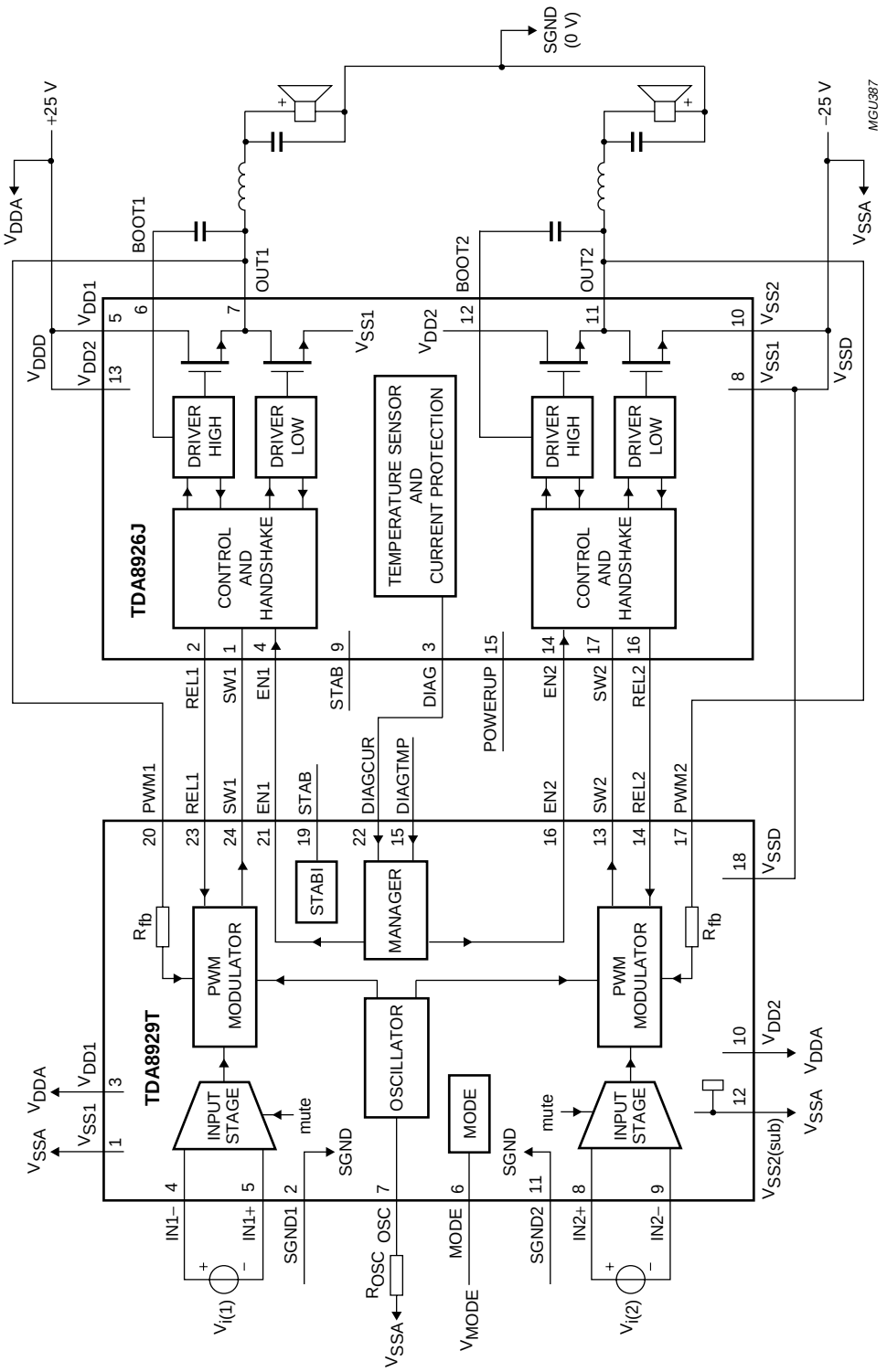


Fig.3 Typical application schematic of the class-D system using controller TDA8929T and the TDA8926J.

8.3 BTL operation

BTL operation can be achieved by driving the audio input channels of the controller in the opposite phase and by connecting the loudspeaker with a BTL output filter between the two outputs (pins OUT1 and OUT2) of the power stage (see Fig.4).

In this way the system operates as a mono BTL amplifier and with the same loudspeaker impedance a four times higher output power can be obtained.

For more information see Chapter 15.

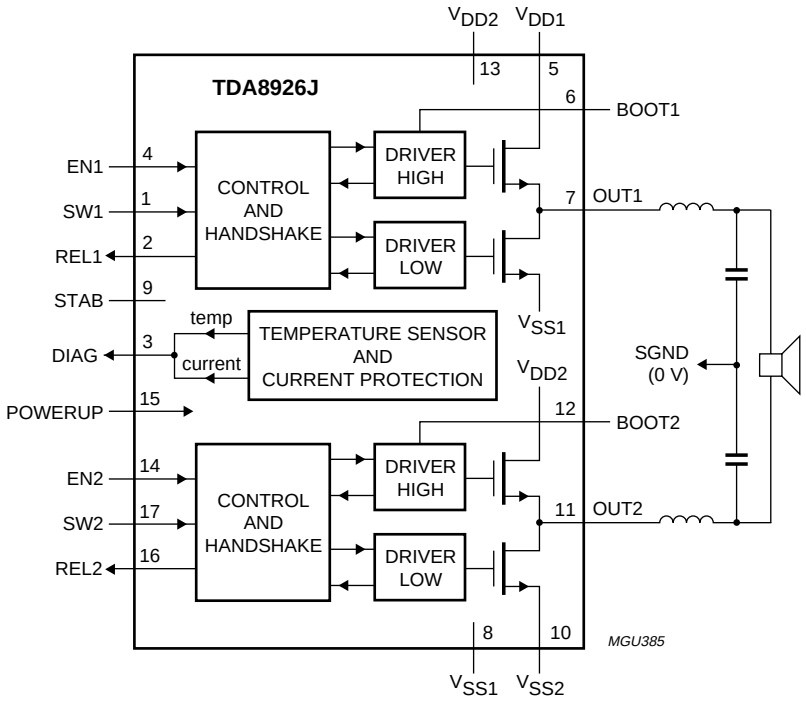


Fig.4 Mono BTL application.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rate System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	±30	V
$V_{P(sc)}$	supply voltage for short-circuits across the load		–	±30	V
I_{ORM}	repetitive peak current in output pins		–	5	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
$V_{es(HBM)}$	electrostatic discharge voltage (HBM)	note 1			
		all pins with respect to V_{DD} (class 1a)	–500	+500	V
		all pins with respect to V_{SS} (class 1a)	–1500	+1500	V
		all pins with respect to each other (class 1a)	–1500	+1500	V
$V_{es(MM)}$	electrostatic discharge voltage (MM)	note 2			
		all pins with respect to V_{DD} (class B)	–250	+250	V
		all pins with respect to V_{SS} (class B)	–250	+250	V
		all pins with respect to each other (class B)	–250	+250	V

Notes

1. Human Body Model (HBM); R_S = 1500 Ω; C = 100 pF.
2. Machine Model (MM); R_S = 10 Ω; C = 200 pF; L = 0.75 μH.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air	1.0	K/W

11 QUALITY SPECIFICATION

In accordance with *"SNW-FQ611-part D"* if this device is used as an audio amplifier (except for ESD, see also Chapter 9).

12 DC CHARACTERISTICS

V_P = ±25 V; T_{amb} = 25 °C; measured in test diagram of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	±15	±25	±30	V
$I_{q(tot)}$	total quiescent current	no load connected	–	35	45	mA
		outputs floating	–	5	10	mA
Internal stabilizer logic supply (pin STAB)						
$V_{O(STAB)}$	stabilizer output voltage		11	13	15	V
Switch inputs (pins SW1 and SW2)						
V_{IH}	HIGH-level input voltage	referenced to V_{SS}	10	–	V_{STAB}	V
V_{IL}	LOW-level input voltage	referenced to V_{SS}	0	–	2	V
Control outputs (pins REL1 and REL2)						
V_{OH}	HIGH-level output voltage	referenced to V_{SS}	10	–	V_{STAB}	V
V_{OL}	LOW-level output voltage	referenced to V_{SS}	0	–	2	V
Diagnostic output (pin DIAG, open-drain)						
V_{OL}	LOW-level output voltage	I_{DIAG} = 1 mA; note 2	0	–	1.0	V
I_{LO}	output leakage current	no error condition	–	–	50	µA
Enable inputs (pins EN1 and EN2)						
V_{IH}	HIGH-level input voltage	referenced to V_{SS}	–	9	V_{STAB}	V
V_{IL}	LOW-level input voltage	referenced to V_{SS}	0	5	–	V
$V_{EN(hys)}$	hysteresis voltage		–	4	–	V
$I_{I(EN)}$	input current		–	–	300	µA
Switching-on input (pin POWERUP)						
$V_{POWERUP}$	operating voltage	referenced to V_{SS}	5	–	12	V
$I_{I(POWERUP)}$	input current	$V_{POWERUP}$ = 12 V	–	100	170	µA
Temperature protection						
T_{diag}	temperature activating diagnostic	$V_{DIAG} = V_{DIAG(LOW)}$	150	–	–	°C
T_{hys}	hysteresis on temperature diagnostic	$V_{DIAG} = V_{DIAG(LOW)}$	–	20	–	°C

Notes

1. The circuit is DC adjusted at V_P = ±15 to ±30 V.
2. Temperature sensor or maximum current sensor activated.

13 AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Single-ended application; note 1						
P_o	output power	R_L = 8 Ω; V_P = ±25 V				
		THD = 0.5%	25[2]	30	–	W
		THD = 10%	30[2]	37	–	W
		R_L = 8 Ω; V_P = ±30 V				
		THD = 0.5%	–	40	–	W
		THD = 10%	–	52	–	W
		R_L = 4 Ω; V_P = ±21 V				
		THD = 0.5%	30[2]	40	–	W
		THD = 10%	40[2]	50	–	W
THD	total harmonic distortion	P_o = 1 W; note 3				
		f_i = 1 kHz	–	0.01	0.05	%
		f_i = 10 kHz	–	0.1	–	%
$G_{v(cl)}$	closed-loop voltage gain		29	30	31	dB
η	efficiency	P_o = 30 W; f_i = 1 kHz; note 4	–	94	–	%
Mono BTL application; note 5						
P_o	output power	R_L = 8 Ω; THD = 0.5%	70[2]	80	–	W
		R_L = 8 Ω; THD = 10%	80[2]	100	–	W
THD	total harmonic distortion	P_o = 1 W; note 3				
		f_i = 1 kHz	–	0.01	0.05	%
		f_i = 10 kHz	–	0.1	–	%
$G_{v(cl)}$	closed loop voltage gain		35	36	37	dB
η	efficiency	P_o = 30 W; f_i = 1 kHz; note 4	–	94	–	%

Notes

1. V_P = ±25 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 310 kHz; R_s = 0.1 Ω (series resistance of filter coil); T_{amb} = 25 °C; measured in reference design (SE application) shown in Fig.7; unless otherwise specified.
2. Indirectly measured; based on $R_{ds(on)}$ measurement.
3. Total Harmonic Distortion (THD) is measured in a bandwidth of 22 Hz to 22 kHz. When distortion is measured using a low-order low-pass filter a significantly higher value will be found, due to the switching frequency outside the audio band.
4. Efficiency for power stage; output power measured across the loudspeaker load.
5. V_P = ±21 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 310 kHz; R_s = 0.1 Ω (series resistance of filter coil); T_{amb} = 25 °C; measured in reference design (BTL application) shown in Fig.7; unless otherwise specified.

14 SWITCHING CHARACTERISTICS

V_P = ±25 V; T_{amb} = 25 °C; measured in Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PWM outputs (pins OUT1 and OUT2); see Fig.5						
t_r	rise time		–	30	–	ns
t_f	fall time		–	30	–	ns
t_{blank}	blanking time		–	70	–	ns
t_{PD}	propagation delay	from pin SW1 (SW2) to pin OUT1 (OUT2)	–	20	–	ns
$t_{W(min)}$	minimum pulse width	note 1	–	220	270	ns
$R_{ds(on)}$	on-resistance of the output transistors		–	0.2	0.3	Ω

Note

1. When used in combination with controller TDA8929T, the effective minimum pulse width during clipping is $0.5t_{W(min)}$.

14.1 Duty factor

For the practical useable minimum and maximum duty factor (δ) which determines the maximum output power:

$$\frac{t_{W(min)} \times f_{osc}}{2} \times 100\% < \delta < \left(1 - \frac{t_{W(min)} \times f_{osc}}{2}\right) \times 100\%$$

Using the typical values: 3.5% < δ < 96.5%.

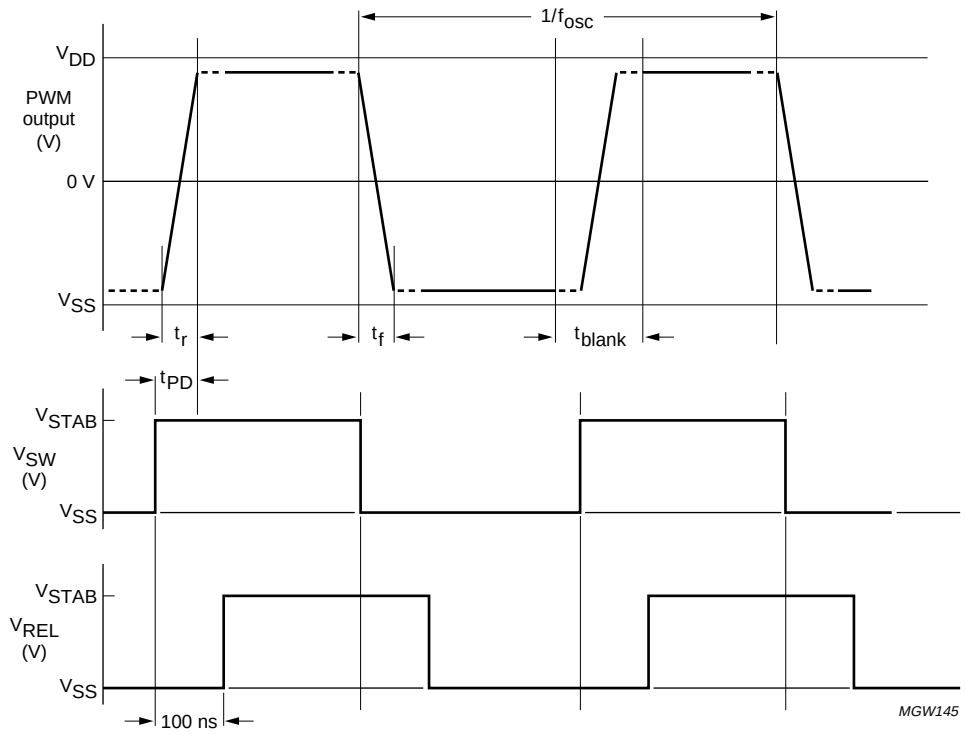


Fig.5 Timing diagram PWM output, switch and release signals.

15 TEST AND APPLICATION INFORMATION

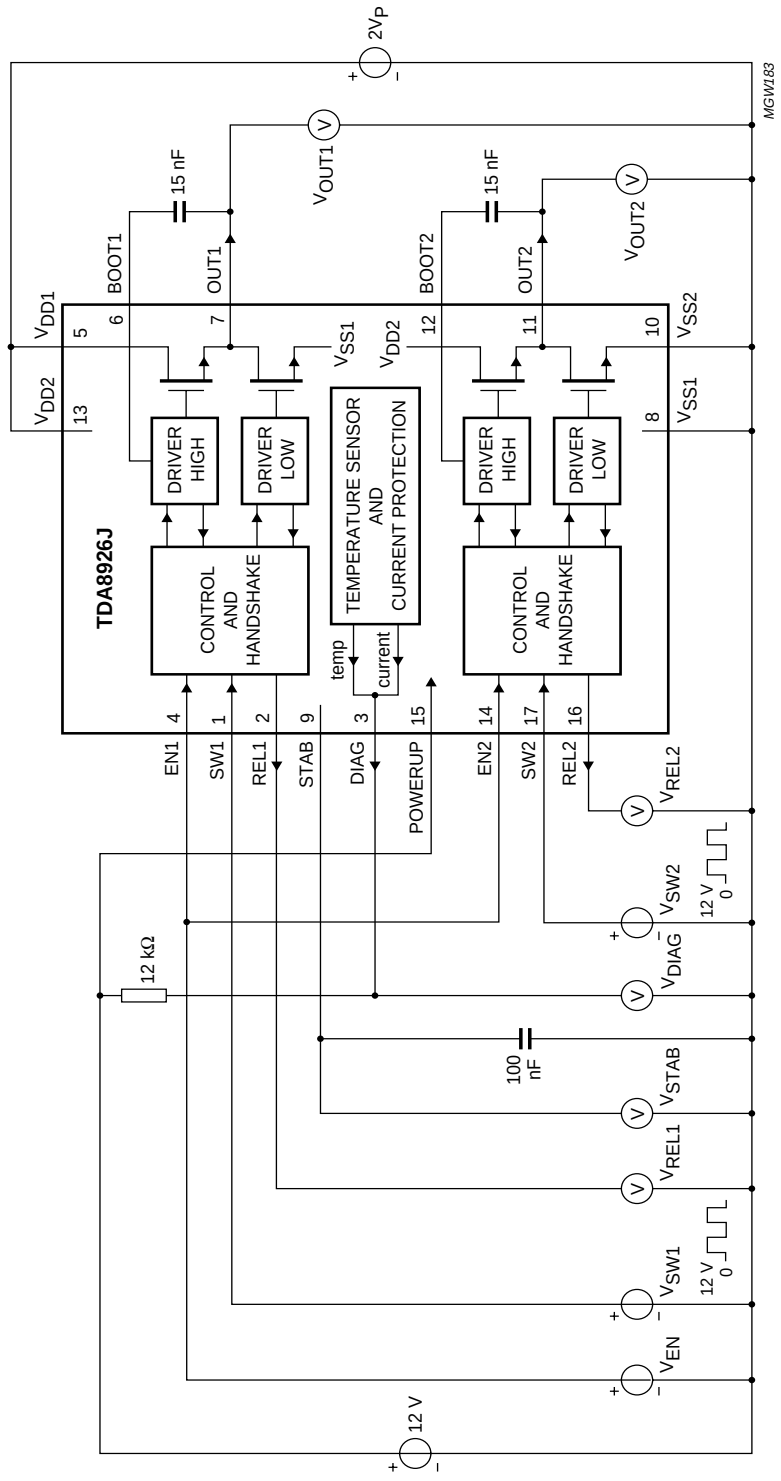


Fig.6 Test diagram.

15.1 BTL application

When using the system in a mono BTL application (for more output power), the inputs of both channels of the PWM modulator must be connected in parallel; the phase of one of the inputs must be inverted. In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

15.2 Package ground connection

The heatsink of the TDA8926J is connected internally to V_{SS}.

15.3 Output power

The output power in single-ended applications can be estimated using the formula

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{(R_L + R_{ds(on)} + R_s)} \times V_P \times (1 - t_{W(min)} \times f_{osc})\right]^2}{2 \times R_L}$$

The maximum current $I_{O(max)} = \frac{[V_P \times (1 - t_{W(min)} \times f_{osc})]}{R_L + R_{ds(on)} + R_s}$ should not exceed 5 A.

The output power in BTL applications can be estimated using the formula

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{R_L + 2 \times (R_{ds(on)} + R_s)} \times 2V_P \times (1 - t_{W(min)} \times f_{osc})\right]^2}{2 \times R_L}$$

The maximum current $I_{O(max)} = \frac{[2V_P \times (1 - t_{W(min)} \times f_{osc})]}{R_L + 2 \times (R_{ds(on)} + R_s)}$ should not exceed 5 A.

Where:

R_L = load impedance

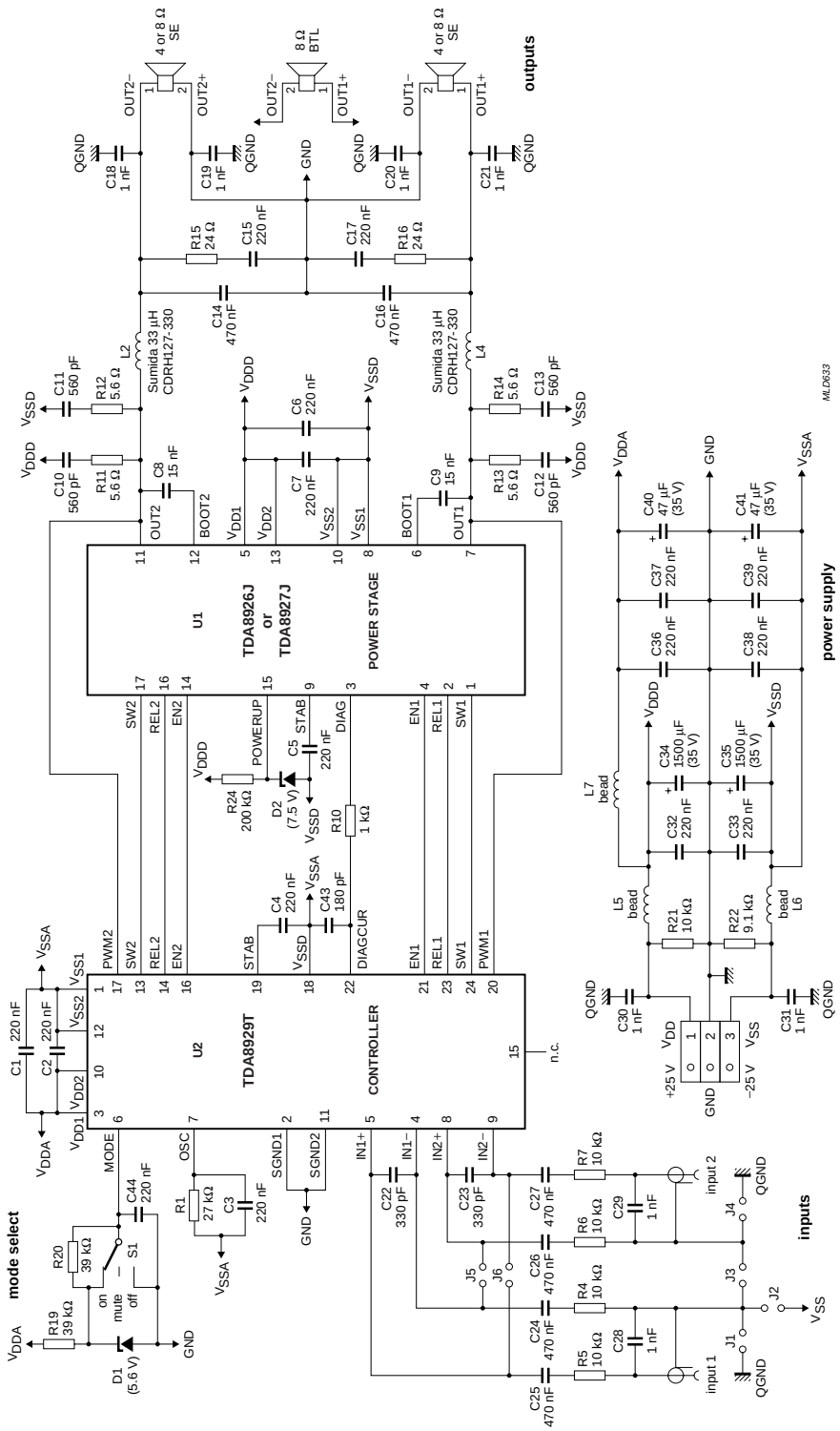
R_s = series resistance of filter coil

$P_{o(1\%)}$ = output power just at clipping

The output power at THD = 10%: $P_{o(10\%)} = 1.25 \times P_{o(1\%)}$.

15.4 Reference design

The reference design for a two-chip class-D audio amplifier for TDA8926J and controller TDA8929T is shown in Fig.7. The Printed-Circuit Board (PCB) layout is shown in Fig.8. The bill of materials is given in Table 1.



R21 and R22 are necessary only in BTL applications with asymmetrical supply.
BTL: remove R6, R7, C23, C26 and C27 and close J5 and J6.
C22 and C23 influence the low-pass frequency response and should be tuned with the real load (loudspeaker).
Inputs floating or inputs referenced to QGND (close J1 and J4) or referenced to V_{SS} (close J2 and J3) for an input signal ground reference.

Fig.7 Two-chip class-D audio amplifier application diagram for TDA8926J and controller TDA8929T.

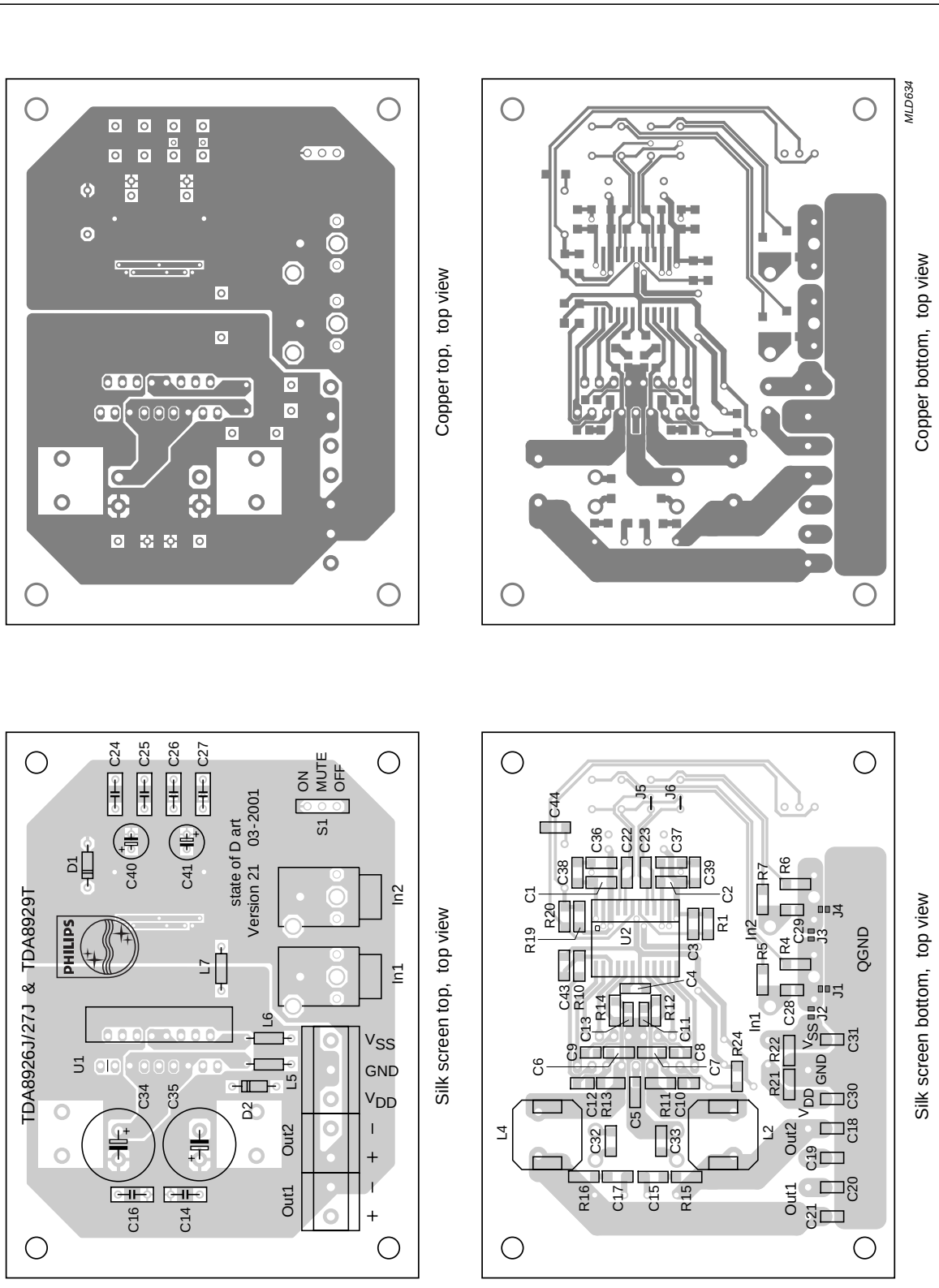


Fig.8 Printed-circuit board layout for TDA8926J and controller TDA8929T.

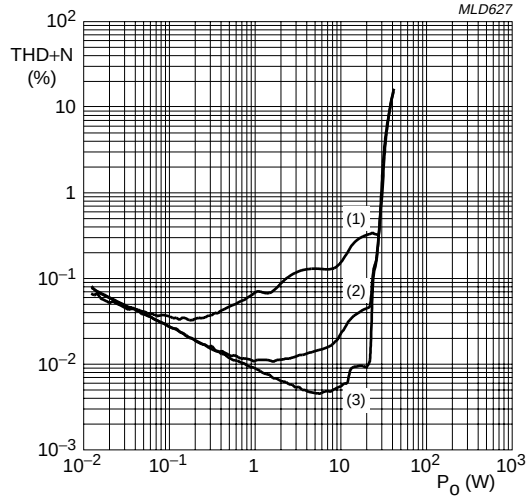
15.5 Reference design bill of material

Table 1 Two-chip class-D audio amplifier PCB (Version 2.1; 03-2001) for TDA8926J and TDA8929T (see Figs 7 and 8)

COMPONENT	DESCRIPTION	VALUE	COMMENTS
In1 and In2	Cinch input connectors		2 × Farnell: 152-396
Out1, Out2, V_{DD}, GND and V_{SS}	supply/output connectors		2 × Augat 5KEV-02; 1 × Augat 5KEV-03
S1	on/mute/off switch		PCB switch Knitter ATE 1 E M-O-M
U1	power stage IC	TDA8926J/27J	DBS17P package
U2	controller IC	TDA8929T	SO24 package
L2 and L4	demodulation filter coils	33 μH	2 × Sumida CDRH127-330
L5, L6 and L7	power supply ferrite beads		3 × Murata BL01RN1-A62
C1 and C2	supply decoupling capacitors for V_{DD} to V_{SS} of the controller	220 nF/63 V	2 × SMD1206
C3	clock decoupling capacitor	220 nF/63 V	SMD1206
C4	12 V decoupling capacitor of the controller	220 nF/63 V	SMD1206
C5	12 V decoupling capacitor of the power stage	220 nF/63 V	SMD1206
C6 and C7	supply decoupling capacitors for V_{DD} to V_{SS} of the power stage	220 nF/63 V	SMD1206
C8 and C9	bootstrap capacitors	15 nF/50 V	2 × SMD0805
C10, C11, C12 and C13	snubber capacitors	560 pF/100 V	4 × SMD0805
C14 and C16	demodulation filter capacitors	470 nF/63 V	2 × MKT
C15 and C17	resonance suppress capacitors	220 nF/63 V	2 × SMD1206
C18, C19, C20 and C21	common mode HF coupling capacitors	1 nF/50 V	4 × SMD0805
C22 and C23	input filter capacitors	330 pF/50 V	2 × SMD1206
C24, C25, C26 and C27	input capacitors	470 nF/63 V	4 × MKT
C28, C29, C30 and C31	common mode HF coupling capacitors	1 nF/50 V	2 × SMD0805
C32 and C33	power supply decoupling capacitors	220 nF/63 V	2 × SMD1206
C34 and C35	power supply electrolytic capacitors	1500 μF/35 V	2 × Rubycon ZL very low ESR (large switching currents)
C36, C37, C38 and C39	analog supply decoupling capacitors	220 nF/63 V	4 × SMD1206
C40 and C41	analog supply electrolytic capacitors	47 μF/35 V	2 × Rubycon ZA low ESR
C43	diagnostic capacitor	180 pF/50 V	SMD1206
C44	mode capacitor	220 nF/63 V	SMD1206
D1	5.6 V Zener diode	BZX79C5V6	DO-35
D2	7.5 V Zener diode	BZX79C7V5	DO-35
R1	clock adjustment resistor	27 kΩ	SMD1206

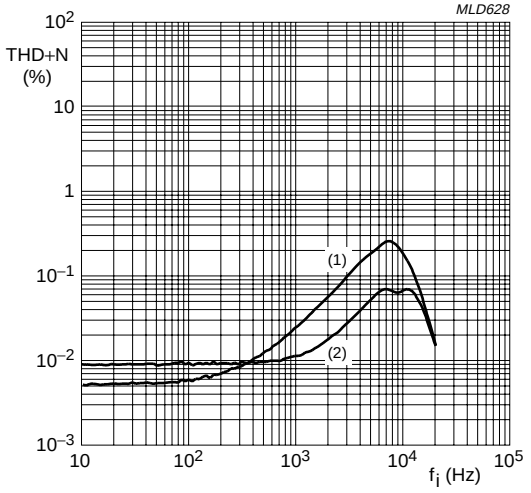
COMPONENT	DESCRIPTION	VALUE	COMMENTS
R4, R5, R6 and R7	input resistors	10 kΩ	4 × SMD1206
R10	diagnostic resistor	1 kΩ	SMD1206
R11, R12, R13 and R14	snubber resistors	5.6 Ω; >0.25 W	4 × SMD1206
R15 and R16	resonance suppression resistors	24 Ω	2 × SMD1206
R19	mode select resistor	39 kΩ	SMD1206
R20	mute select resistor	39 kΩ	SMD1206
R21	resistor needed when using an asymmetrical supply	10 kΩ	SMD1206
R22	resistor needed when using an asymmetrical supply	9.1 kΩ	SMD1206
R24	bias resistor for powering-up the power stage	200 kΩ	SMD1206

15.6 Curves measured in reference design



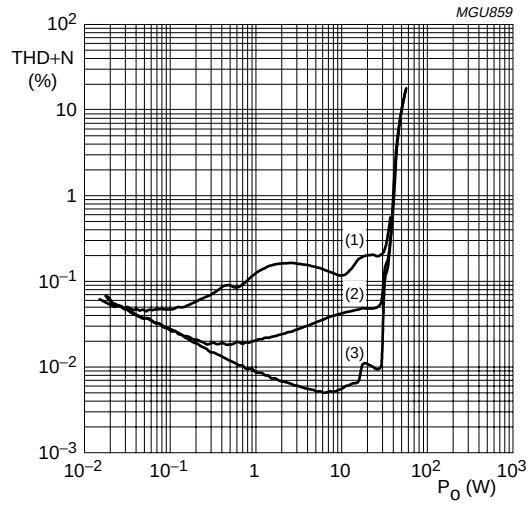
2 × 8 Ω SE; V_P = ±25 V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.9 Total harmonic distortion plus noise as a function of output power.



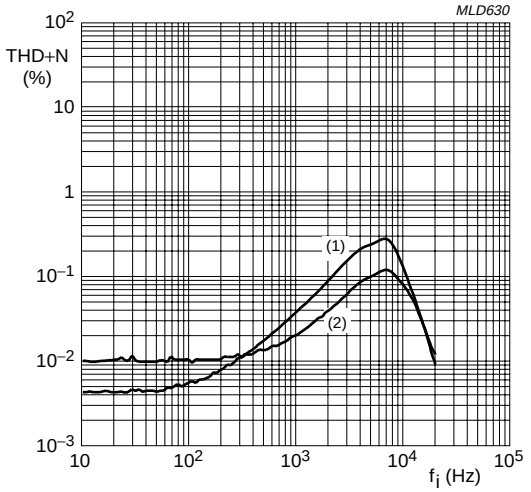
2 × 8 Ω SE; V_P = ±25 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.10 Total harmonic distortion plus noise as a function of input frequency.



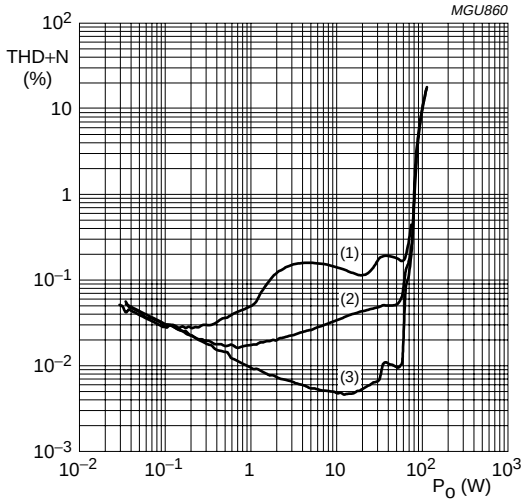
2 × 4 Ω SE; V_P = ±21 V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.11 Total harmonic distortion plus noise as a function of output power.



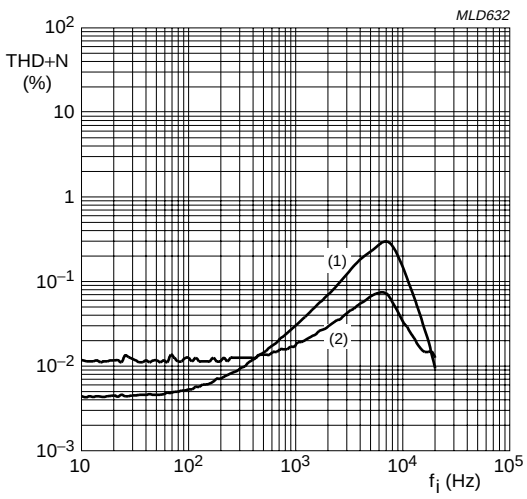
2 × 4 Ω SE; V_P = ±21 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.12 Total harmonic distortion plus as a function of input frequency.



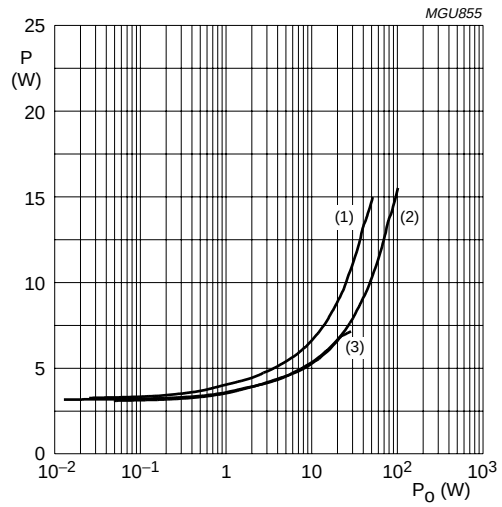
1 × 8 Ω BTL; V_P = ±21 V.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.13 Total harmonic distortion plus noise as a function of output power.



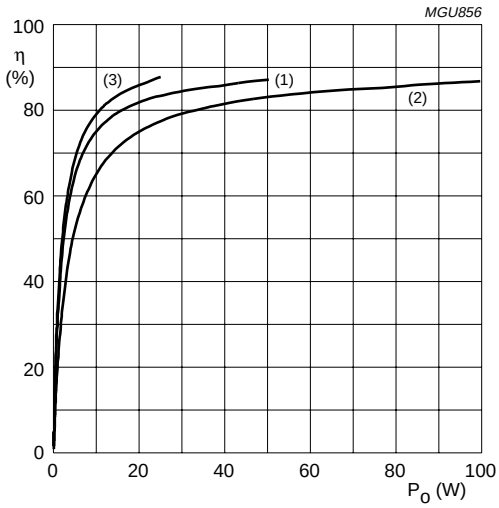
1 × 8 Ω BTL; V_P = ±21 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.14 Total harmonic distortion plus noise as a function of input frequency.



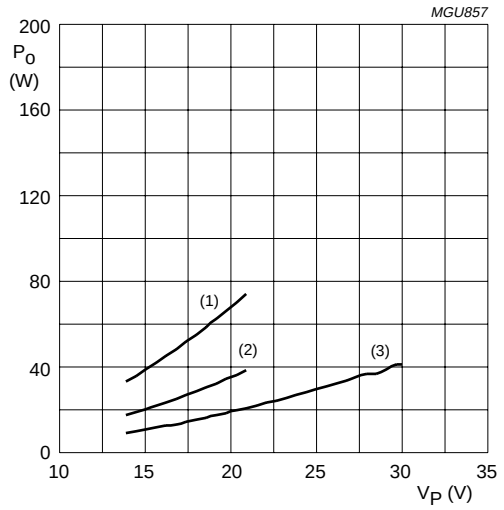
V_P = ±21 V; f_i = 1 kHz.
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.
(3) 2 × 8 Ω SE.

Fig.15 Power dissipation as a function of output power.



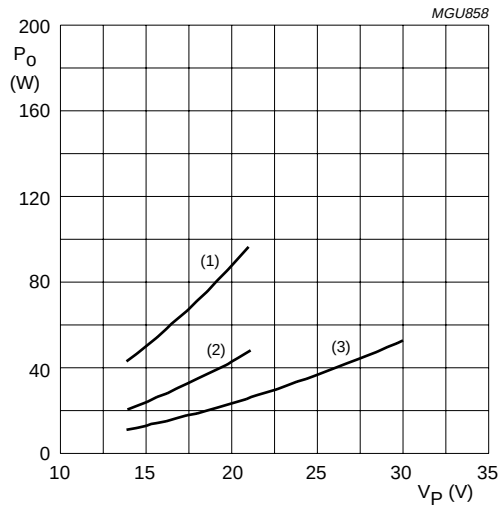
V_P = ±21 V; f_i = 1 kHz.
(1) 2 × 4 Ω SE.
(2) 1 × 8 Ω BTL.
(3) 2 × 8 Ω SE.

Fig.16 Efficiency as a function of output power.



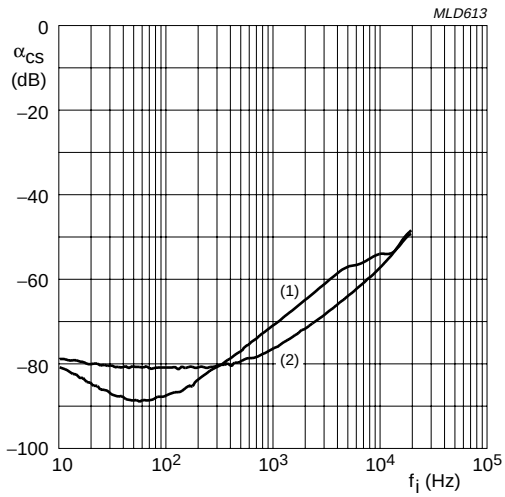
THD + N = 0.5%; f_i = 1 kHz.
(1) 1 × 8 Ω BTL.
(2) 2 × 4 Ω SE.
(3) 2 × 8 Ω SE.

Fig.17 Output power as a function of supply voltage.



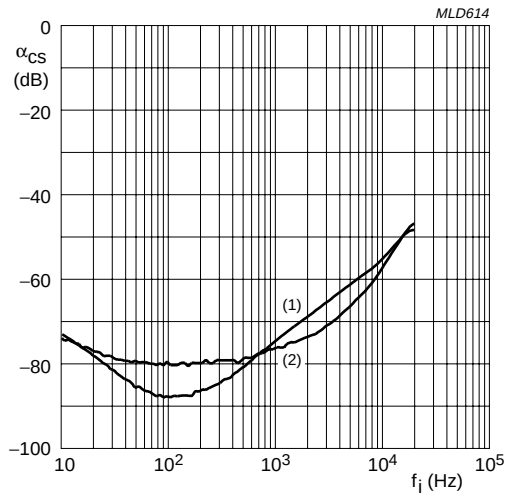
THD + N = 10%; f_i = 1 kHz.
(1) 1 × 8 Ω BTL.
(2) 2 × 4 Ω SE.
(3) 2 × 8 Ω SE.

Fig.18 Output power as a function of supply voltage.



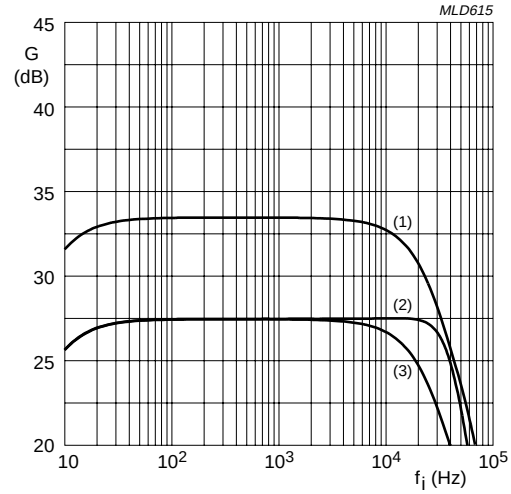
2 × 8 Ω SE; V_P = ±21 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.19 Channel separation as a function of input frequency.



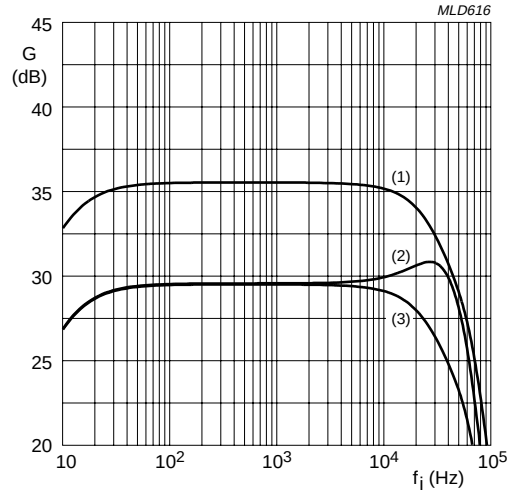
2 × 4 Ω SE; V_P = ±21 V.
(1) P_o = 10 W.
(2) P_o = 1 W.

Fig.20 Channel separation as a function of input frequency.



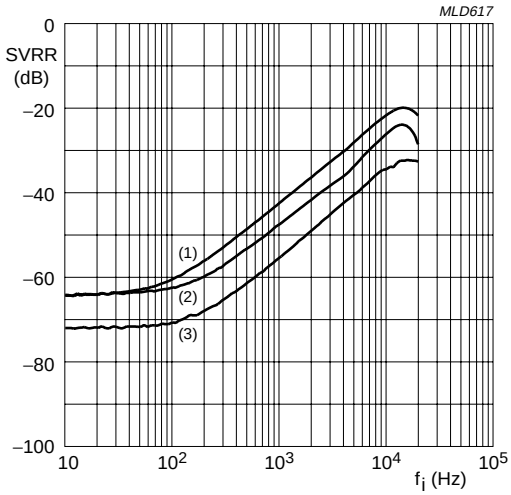
V_P = ±21 V; V_i = 100 mV; R_s = 10 kΩ/C_i = 330 pF.
(1) 1 × 8 Ω BTL.
(2) 2 × 8 Ω SE.
(3) 2 × 4 Ω SE.

Fig.21 Gain as a function of input frequency.



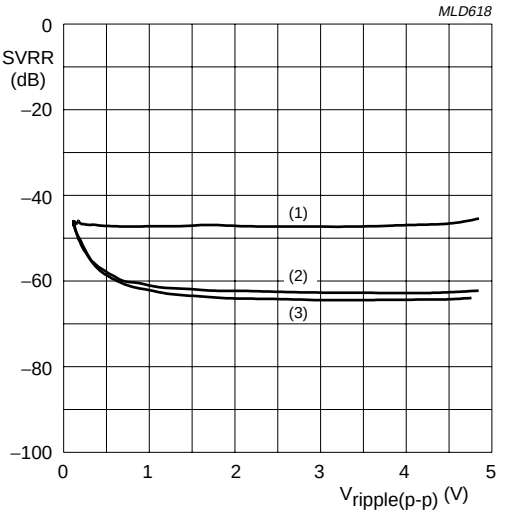
V_P = ±21 V; V_i = 100 mV; R_s = 0 Ω.
(1) 1 × 8 Ω BTL.
(2) 2 × 8 Ω SE.
(3) 2 × 4 Ω SE.

Fig.22 Gain as a function of input frequency.



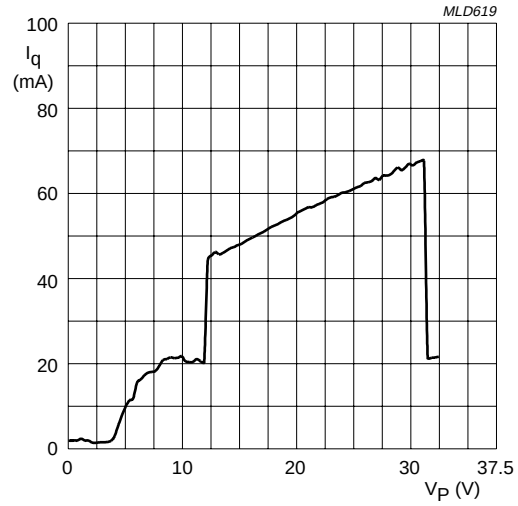
V_P = ±21 V; $V_{ripple(p-p)}$ = 2 V.
(1) Both supply lines in antiphase.
(2) Both supply lines in phase.
(3) One supply line rippled.

Fig.23 Supply voltage ripple rejection as a function of input frequency.



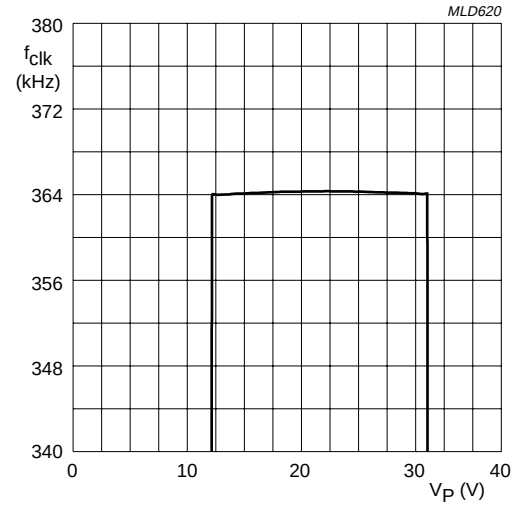
V_P = ±21 V.
(1) f_{ripple} = 1 kHz.
(2) f_{ripple} = 100 Hz.
(3) f_{ripple} = 10 Hz.

Fig.24 Supply voltage ripple rejection as a function of ripple voltage (peak-to-peak value).



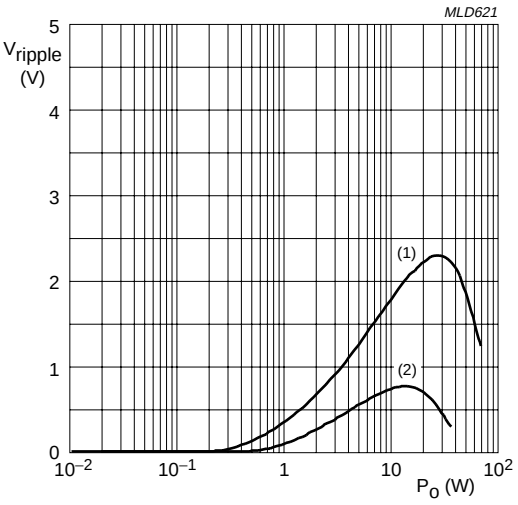
R_L = open-circuit.

Fig.25 Quiescent current as a function of supply voltage.



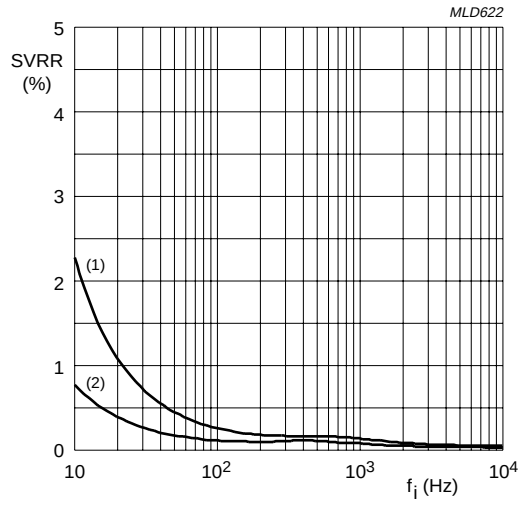
R_L = open-circuit.

Fig.26 Clock frequency as a function of supply voltage.



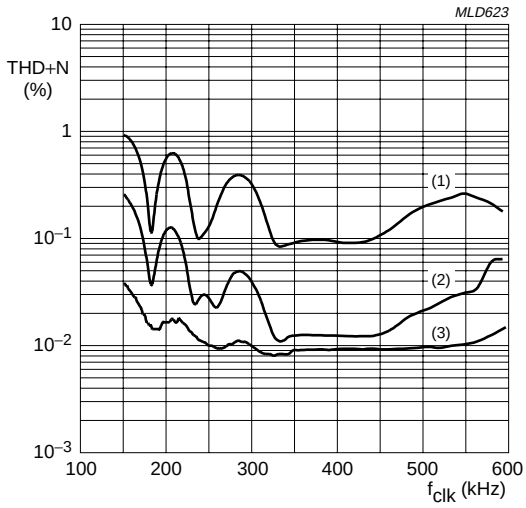
V_P = ±21 V; 1500 μF per supply line; f_i = 10 Hz.
(1) 1 × 4 Ω SE.
(2) 1 × 8 Ω SE.

Fig.27 Supply voltage ripple as a function of output power.



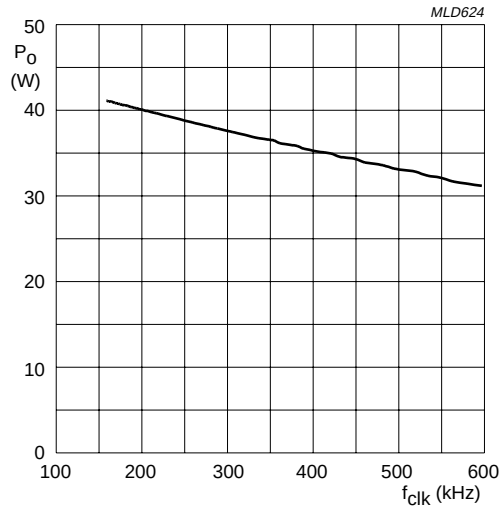
V_P = ±21 V; 1500 μF per supply line.
(1) P_o = 30 W into 1 × 4 Ω SE.
(2) P_o = 15 W into 1 × 8 Ω SE.

Fig.28 Supply voltage ripple rejection as a function of input frequency.



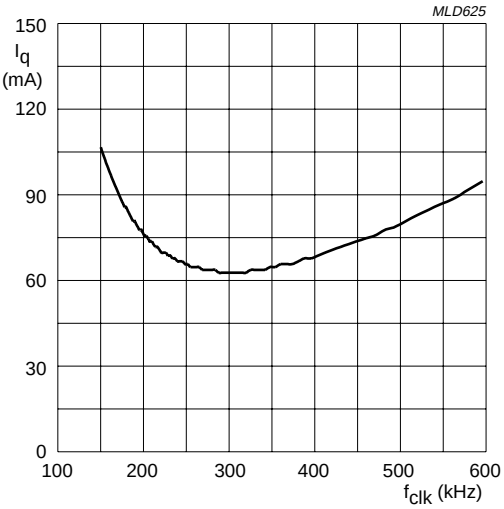
V_P = ±21 V; P_o = 1 W in 2 × 8 Ω.
(1) 10 kHz.
(2) 1 kHz.
(3) 100 Hz.

Fig.29 Total harmonic distortion plus noise as a function of clock frequency.



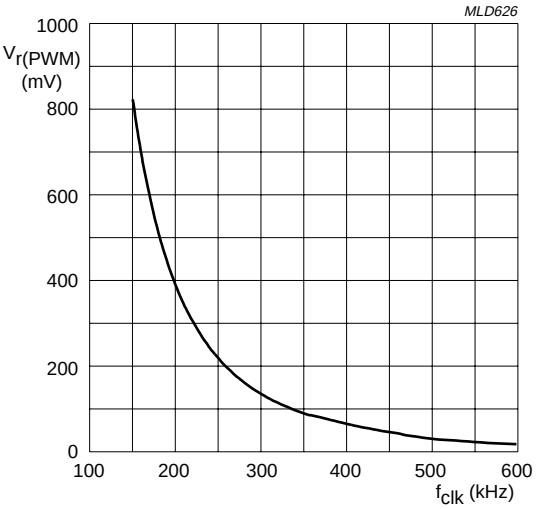
V_P = ±21 V; R_L = 2 × 8 Ω; f_i = 1 kHz; THD + N = 10%.

Fig.30 Output power as a function of clock frequency.



V_P = ±25 V; R_L = open-circuit.

Fig.31 Quiescent current as a function of clock frequency.

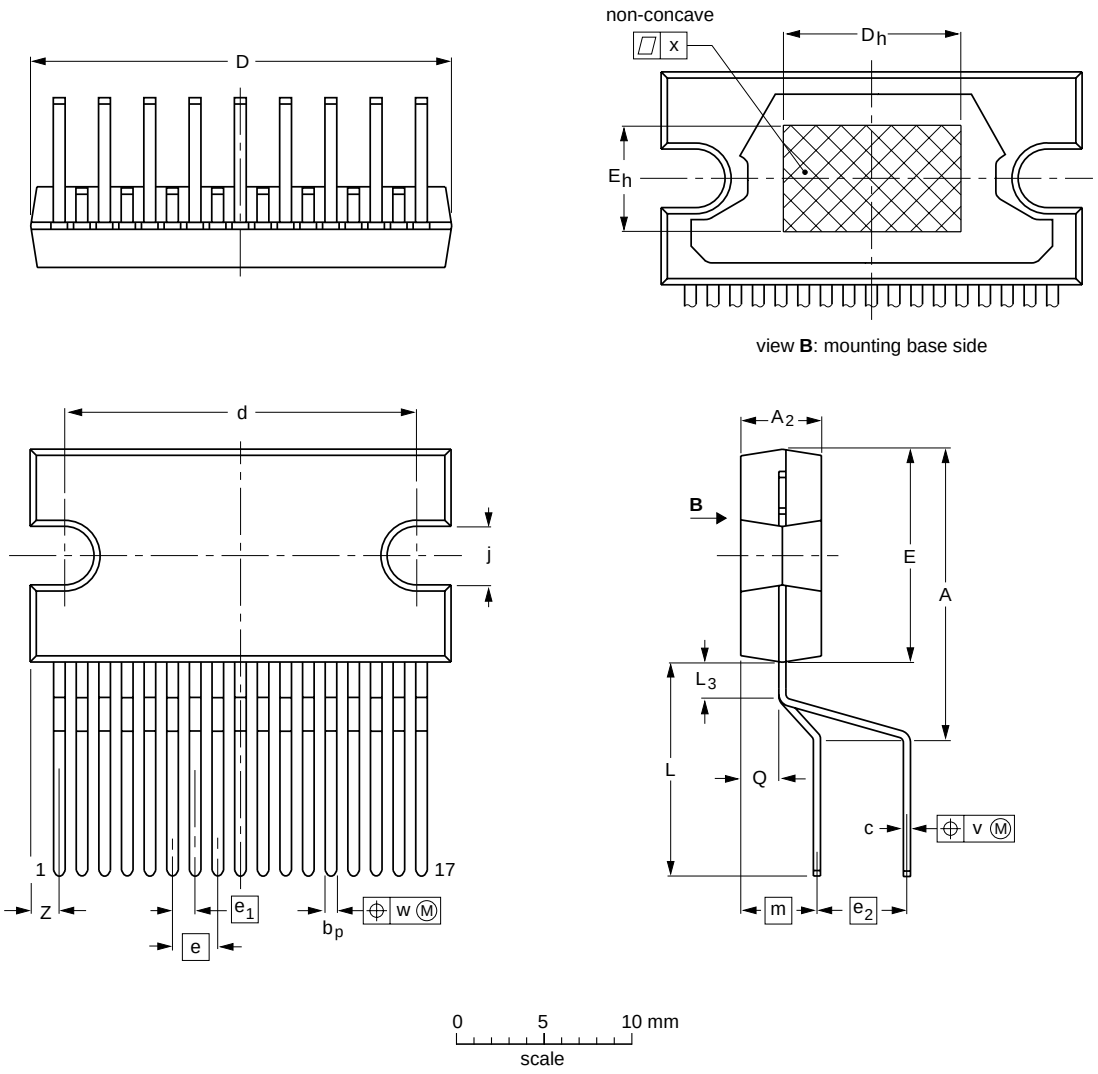


V_P = ±25 V; R_L = 2 × 8 Ω.

Fig.32 PWM residual voltage as a function of clock frequency.

16 PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						~~97-12-16~~ 99-12-17

17 SOLDERING

17.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

17.2 Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

17.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

17.4 Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

18 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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