DATA SHEET

TDA8358J
Full bridge vertical deflection output circuit in LVDMOS with east-west amplifier

Product specification
Supersedes data of 1999 Dec 22

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Philips Semiconductors

PHILIPS

Full bridge vertical deflection output circuit in LVDMOS with east-west amplifier

TDA8358J

FEATURES

- Few external components required
- High efficiency fully DC-coupled vertical bridge output circuit
- Vertical flyback switch with short rise and fall times
- Built-in guard circuit
- Thermal protection circuit
- Improved EMC performance due to differential inputs
- East-west output stage.

GENERAL DESCRIPTION

The TDA8358J is a power circuit for use in 90° and 110° colour deflection systems for 25 to 200 Hz field frequencies, and for 4 : 3 and 16 : 9 picture tubes. The IC contains a vertical deflection output circuit, operating as a high efficiency class G system. The full bridge output circuit allows DC coupling of the deflection coil in combination with single positive supply voltages.

The east-west output stage is able to supply the sink current for a diode modulator circuit.

The IC is constructed in a Low Voltage DMOS (LVDMOS) process that combines bipolar, CMOS and DMOS devices. DMOS transistors are used in the output stage because of absence of second breakdown.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	supply voltage		7.5	12	18	V
V_{FB}	flyback supply voltage		$2 \times V_P$	45	66	V
$I_{q(P)(av)}$	average quiescent supply current	during scan	–	10	15	mA
$I_{q(FB)(av)}$	average quiescent flyback supply current	during scan	–	–	10	mA
P_{tot}	total power dissipation		–	–	15	W
Inputs and outputs						
$V_{i(p-p)}$	input voltage (peak-to-peak value)		–	1000	1500	mV
$I_{o(p-p)}$	output current (peak-to-peak value)		–	–	3.2	A
Flyback switch						
$I_{o(peak)}$	maximum (peak) output current	$t \leq 1.5$ ms	–	–	±1.8	A
East-west amplifier						
V_o	output voltage		–	–	68	V
$V_{I(bias)}$	input bias voltage		2	–	3.2	V
I_o	output current		–	–	750	mA
Thermal data; in accordance with IEC 747-1						
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	ambient temperature		–25	–	+85	°C
T_j	junction temperature		–	–	+150	°C

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TDA8358J

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8358J	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

BLOCK DIAGRAM

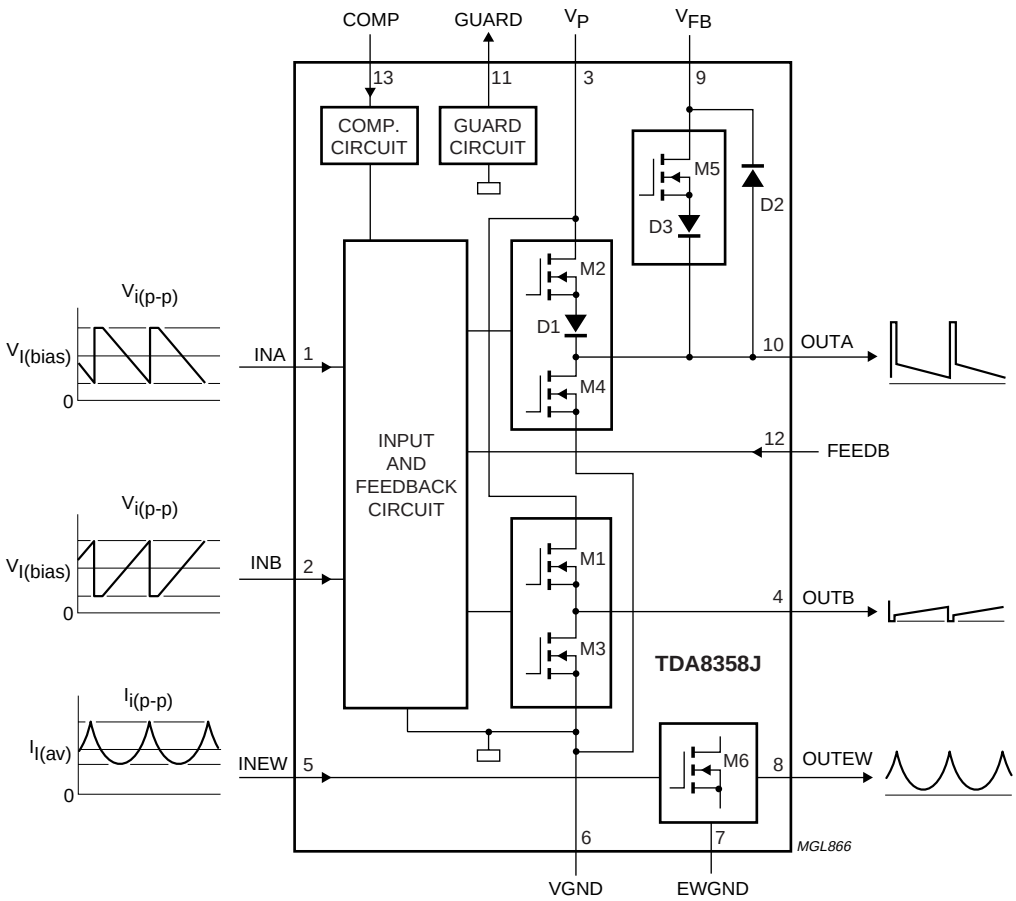
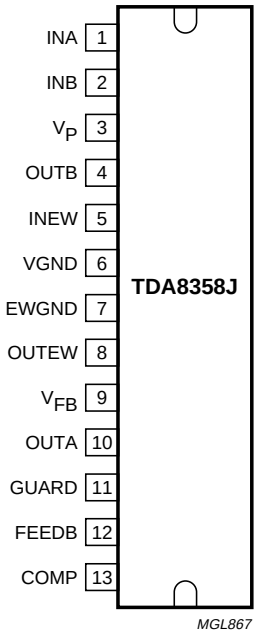


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INA	1	positive vertical input
INB	2	negative vertical input
V_P	3	supply voltage
OUTB	4	vertical output voltage B
INEW	5	east-west input voltage
VGND	6	vertical ground
EWGND	7	east-west ground
OUTEW	8	east-west output voltage
V_{FB}	9	flyback supply voltage
OUTA	10	vertical output voltage A
GUARD	11	guard output voltage
FEEDB	12	input measuring resistor
COMP	13	input compensation current



The die has been glued to the metal block of the package. If the metal block is not insulated from the heatsink, the heatsink shall only be connected directly to pin VGND.

Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Vertical output stage

The vertical driver circuit has a bridge configuration. The deflection coil is connected between the complimentary driven output amplifiers. The differential input circuit is voltage driven. The input circuit is specially designed for direct connection to driver circuits delivering a differential signal but it is also suitable for single-ended applications. For processors with output currents, the currents are converted to voltages by the conversion resistors R_{CV1} and R_{CV2} (see Fig.3) connected to pins INA and INB. The differential input voltage is compared with the voltage across the measuring resistor R_M, thus providing feedback information. The voltage across R_M is proportional with the output current. The relationship between the differential input voltage and the output current is defined by:

$$V_{i(dif)(p\text{-}p)} = I_{o(p\text{-}p)} \times R_M;\ V_{i(dif)(p\text{-}p)} = V_{INA} - V_{INB}$$

The output current should not exceed 3.2 A (p-p) and is determined by the value of R_M and R_{CV}. The allowable input voltage range is 100 mV to 1.6 V for each input. The formula given does not include internal bondwire resistances. Depending on the value of R_M and the internal bondwire resistance (typical value 50 mΩ) the actual value of the current in the deflection coil will be about 5% lower than calculated.

Flyback supply

The flyback voltage is determined by the flyback supply voltage V_{FB}. The principle of two supply voltages (class G) allows to use an optimum supply voltage V_P for scan and an optimum flyback supply voltage V_{FB} for flyback, thus very high efficiency is achieved. The available flyback output voltage across the coil is almost equal to V_{FB}, due to the absence of a coupling capacitor which is not required in a bridge configuration. The very short rise and fall times of the flyback switch are determined mainly by the slew rate value of more than 300 V/μs.

Protection

The output circuit contains protection circuits for:

- Too high die temperature
- Overvoltage of output A.

Guard circuit

A guard circuit with output pin GUARD is provided.

The guard circuit generates a HIGH-level during the flyback period. The guard circuit is also activated for one of the following conditions:

- During thermal protection ($T_j \approx 170$ °C)
- During an open-loop condition.

The guard signal can be used for blanking the picture tube and signalling fault conditions. The vertical synchronization pulses of the guard signal can be used by an On Screen Display (OSD) microcontroller.

Damping resistor compensation

HF loop stability is achieved by connecting a damping resistor R_{D1} (see Fig.4) across the deflection coil. The current values in R_{D1} during scan and flyback are significantly different. Both the resistor current and the deflection coil current flow into measuring resistor R_M, resulting in a too low deflection coil current at the start of the scan.

The difference in the damping resistor current values during scan and flyback have to be externally compensated in order to achieve a short settling time.

For that purpose a compensation resistor R_{CMP} is connected between pins OUTA and COMP. The value of R_{CMP} is calculated by:

$$R_{CMP} = \frac{(V_{FB} - V_{loss(FB)} - V_P) \times R_{D1} \times (R_S + 300)}{(V_{FB} - V_{loss(FB)} - I_{coil(peak)} \times R_{coil}) \times R_M}$$

where:

- R_{coil} is the coil resistance
- $V_{loss(FB)}$ is the voltage loss between pins V_{FB} and OUTA at flyback.

East-west amplifier

The east-west amplifier is current driven. The output can only sink currents of the diode modulator circuit.
A feedback resistor (see Fig.4) has to be connected between the input and output of the inverting east-west amplifier in order to convert the east-west correction input current into an output voltage. The output voltage of the east-west circuit at pin OUTEW is given by:

$$V_{OUTEW} \approx I_{INEW} \times R_{EWF} + V_{INEW}$$

The maximum output voltage is $V_{o(max)} = 68$ V, while the maximum output current of the circuit is $I_{o(max)} = 750$ mA.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		–	18	V
V_{FB}	flyback supply voltage		–	68	V
$\Delta V_{VGND-EWGND}$	voltage difference between pins VGND and EWGND		–	0.3	V
V_n	DC voltage				
	pins OUTA and OUTEW	note 1	–	68	V
	pin OUTB		–	V_P	V
	pins INA, INB, INEW, GUARD, FEEDB, and COMP		–0.5	V_P	V
I_n	DC current				
	pins OUTA and OUTB	during scan (p-p)	–	3.2	A
	pins OUTA and OUTB	at flyback (peak); $t \leq 1.5$ ms	–	±1.8	A
	pins INA, INB, INEW, GUARD, FEEDB, and COMP		–20	+20	mA
	pin OUTEW		–	750	mA
I_{lu}	latch-up current	input current into any pin; pin voltage is $1.5 \times V_P$; T_j = 150 °C	–	+200	mA
		input current out of any pin; pin voltage is $-1.5 \times V_P$; T_j = 150 °C	–200	–	mA
V_{es}	electrostatic handling voltage	machine model; note 2	–350	+350	V
		human body model; note 3	–4000	+4000	V
P_{EW}	east-west power dissipation	note 4	–	4	W
P_{tot}	total power dissipation		–	15	W
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–25	+85	°C
T_j	junction temperature	note 5	–	+150	°C

Notes

1. When the voltage at pin OUTA supersedes 70 V the circuit will limit the voltage.
2. Equivalent to 200 pF capacitance discharge through a 0 Ω resistor.
3. Equivalent to 100 pF capacitance discharge through a 1.5 kΩ resistor.
4. For repetitive time durations of $t < 0.1$ ms or a non-repetitive time duration of $t < 5$ ms the maximum (peak) east-west power dissipation $P_{EW(peak)}$ = 15 W.
5. Internally limited by thermal protection at $T_j \approx 170$ °C.

THERMAL CHARACTERISTICS

In accordance with IEC 747-1.

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case		4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W

CHARACTERISTICS

V_P = 12 V; V_{FB} = 45 V; f_{vert} = 50 Hz; $V_{I(bias)}$ = 880 mV; T_{amb} = 25 °C; measured in test circuit of Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_P	operating supply voltage		7.5	12	18	V
V_{FB}	flyback supply voltage	note 1	$2 \times V_P$	45	66	V
$I_{q(P)(av)}$	average quiescent supply current	during scan	–	10	15	mA
$I_{q(P)}$	quiescent supply current	no signal; no load	–	45	75	mA
$I_{q(FB)(av)}$	average quiescent flyback supply current	during scan	–	–	10	mA
Inputs A and B						
$V_{i(p-p)}$	input voltage (peak-to-peak value)	note 2	–	1000	1500	mV
$V_{I(bias)}$	input bias voltage	note 2	100	880	1600	mV
$I_{I(bias)}$	input bias current		–	25	35	µA
Outputs A and B						
$V_{loss(1)}$	voltage loss first scan part	note 3				
		I_o = 1.1 A	–	–	4.5	V
		I_o = 1.6 A	–	–	6.6	V
$V_{loss(2)}$	voltage loss second scan part	note 4				
		I_o = –1.1 A	–	–	3.3	V
		I_o = –1.6 A	–	–	4.8	V
$I_{o(p-p)}$	output current (peak-to-peak value)		–	–	3.2	A
LE	linearity error	$I_{o(p-p)}$ = 3.2 A; notes 5 and 6				
		adjacent blocks	–	1	2	%
		non-adjacent blocks	–	1	3	%
V_{offset}	offset voltage	across R_M; $V_{i(dif)}$ = 0 V				
		$V_{I(bias)}$ = 200 mV	–	–	±15	mV
		$V_{I(bias)}$ = 1 V	–	–	±20	mV
$\Delta V_{offset(T)}$	offset voltage variation with temperature	across R_M; $V_{i(dif)}$ = 0 V	–	–	40	µV/K
V_O	DC output voltage	$V_{i(dif)}$ = 0 V	–	$0.5 \times V_P$	–	V
$G_{v(ol)}$	open-loop voltage gain	notes 7 and 8	–	60	–	dB
$f_{-3dB(h)}$	high –3 dB cut-off frequency	open-loop	–	1	–	kHz
G_v	voltage gain	note 9	–	1	–	
$\Delta G_{v(T)}$	voltage gain variation with temperature		–	–	10^{-4}	K^{-1}
PSRR	power supply rejection ratio	note 10	80	90	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback switch						
$I_{o(peak)}$	maximum (peak) output current	$t \leq 1.5$ ms	–	–	±1.8	A
$V_{loss(FB)}$	voltage loss at flyback	note 11				
		$I_o = 1.1$ A	–	7.5	8.5	V
		$I_o = 1.6$ A	–	8	9	V
Guard circuit						
$V_{O(grd)}$	guard output voltage	$I_{O(grd)} = 100$ µA	5	6	7	V
$V_{O(grd)(max)}$	allowable guard voltage	maximum leakage current $I_{L(max)} = 10$ µA	–	–	18	V
$I_{O(grd)}$	output current	$V_{O(grd)} = 0$ V; not active	–	–	10	µA
		$V_{O(grd)} = 4.5$ V; active	1	–	2.5	mA
East-west amplifier						
V_o	output voltage	at pin OUTEW	–	–	68	V
V_{loss}	voltage loss	$I_o = 750$ mA; note 12	–	–	5	V
$V_{I(bias)}$	input bias voltage		2	2.5	3.2	V
$I_{I(bias)}$	input bias current	into pin INEW; note 13				
		$I_o = 100$ mA	–	2.5	–	µA
		$I_o = 500$ mA	–	11.5	–	µA
$G_{v(ol)}$	open-loop voltage gain		–	30	–	dB
THD	harmonic distortion		–	0.5	1	%
$f_{-3dB(h)}$	high –3 dB cut-off frequency		–	–	1	MHz

Notes

1. To limit V_{OUTA} to 68 V, V_{FB} must be 66 V due to the voltage drop of the internal flyback diode between pins OUTA and V_{FB} at the first part of the flyback.
2. Allowable input range for both inputs: $V_{I(bias)} + V_i < 1600$ mV and $V_{I(bias)} - V_i > 100$ mV.
3. This value specifies the sum of the voltage losses of the internal current paths between pins V_P and OUTA, and between pins OUTB and GND. Specified for $T_j = 125$ °C. The temperature coefficient for $V_{loss(1)}$ is a positive value.
4. This value specifies the sum of the voltage losses of the internal current paths between pins V_P and OUTB, and between pins OUTA and GND. Specified for $T_j = 125$ °C. The temperature coefficient for $V_{loss(2)}$ is a positive value.
5. The linearity error is measured for a linear input signal without S-correction and is based on the 'on screen' measurement principle. This method is defined as follows. The output signal is divided in 22 successive equal time parts. The 1st and 22nd parts are ignored, and the remaining 20 parts form 10 successive blocks k. A block consists of two successive parts. The voltage amplitudes are measured across R_M, starting at k = 1 and ending at k = 10, where V_k and V_{k+1} are the measured voltages of two successive blocks. V_{min}, V_{max} and V_{avg} are the minimum, maximum and average voltages respectively. The linearity errors are defined as:

   a) $LE = \frac{V_k - V_{k+1}}{V_{avg}} \times 100\%$ (adjacent blocks)

   b) $LE = \frac{V_{max} - V_{min}}{V_{avg}} \times 100\%$ (non adjacent blocks)
6. The linearity errors are specified for a minimum input voltage at pin 1 or pin 2 of 300 mV. Lower input voltages lead to voltage dependent S-distortion in the input stage.
7. $G_{v(ol)} = \frac{V_{OUTA} - V_{OUTB}}{V_{FEEDB} - V_{OUTB}}$
8. Pin FEEDB not connected.
9. $G_V = \frac{V_{FEEDB} - V_{OUTB}}{V_{INA} - V_{INB}}$
10. $V_{P(ripple)} = 500$ mV (RMS value); 50 Hz < $f_{P(ripple)}$ < 1 kHz; measured across R_M.
11. This value specifies the internal voltage loss of the current path between pins V_{FB} and OUTA.
12. This value specifies the internal voltage loss of the current path between pins OUTEW and EWGND.
13. Measured for $R_{EWF} = 10$ kΩ; $R_{EWL} = 30$ Ω; $V_o = 6$ V.
    a) For $I_o = 100$ mA and a voltage of 9 V at R_{EWL} connected to the line output transformer, the east-west amplifier input current (see Fig.4) is $I_i = 300$ µA.
    b) For $I_o = 500$ mA and a voltage of 21 V at R_{EWL} connected to the line output transformer, the east-west amplifier input current (see Fig.4) is $I_i = 350$ µA.

APPLICATION INFORMATION

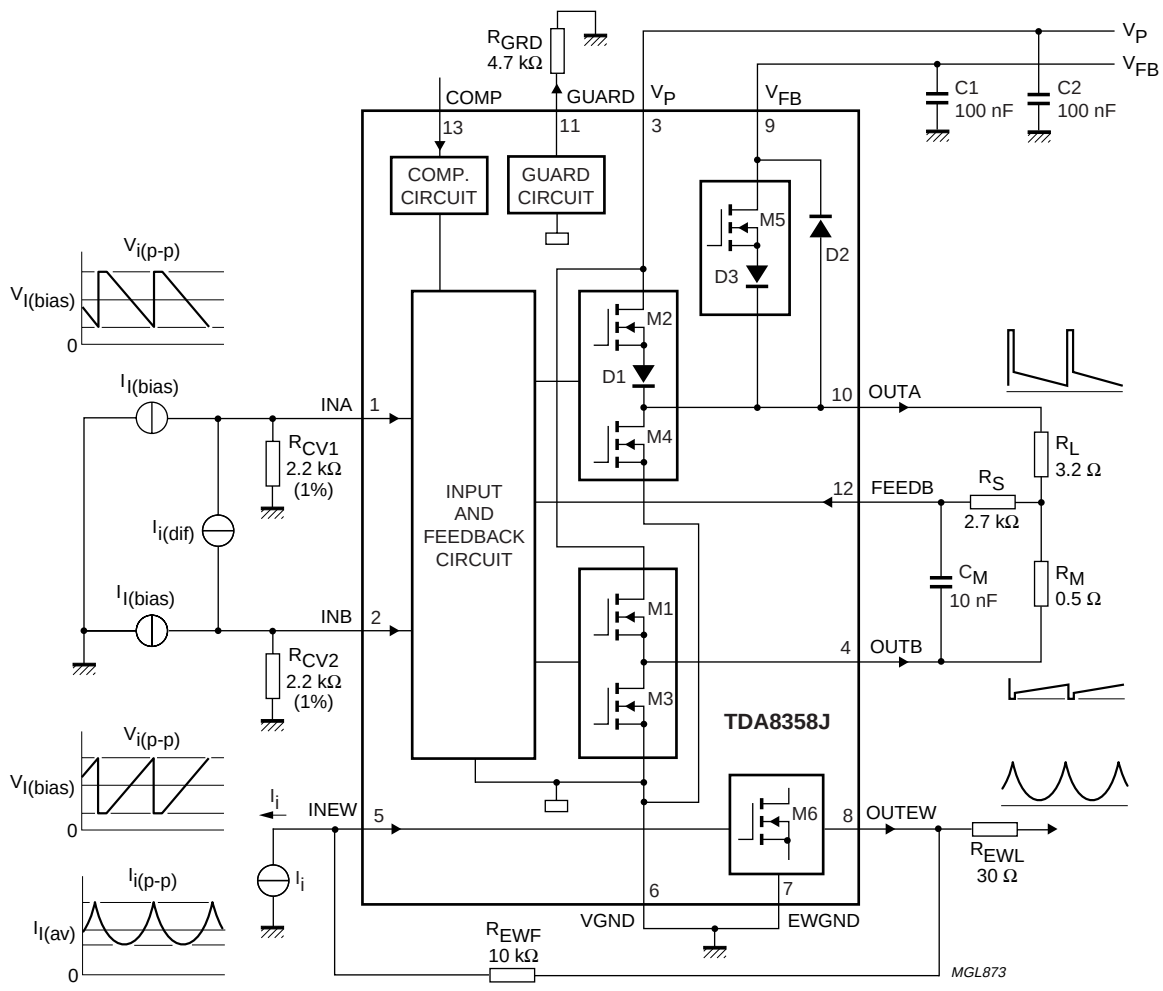
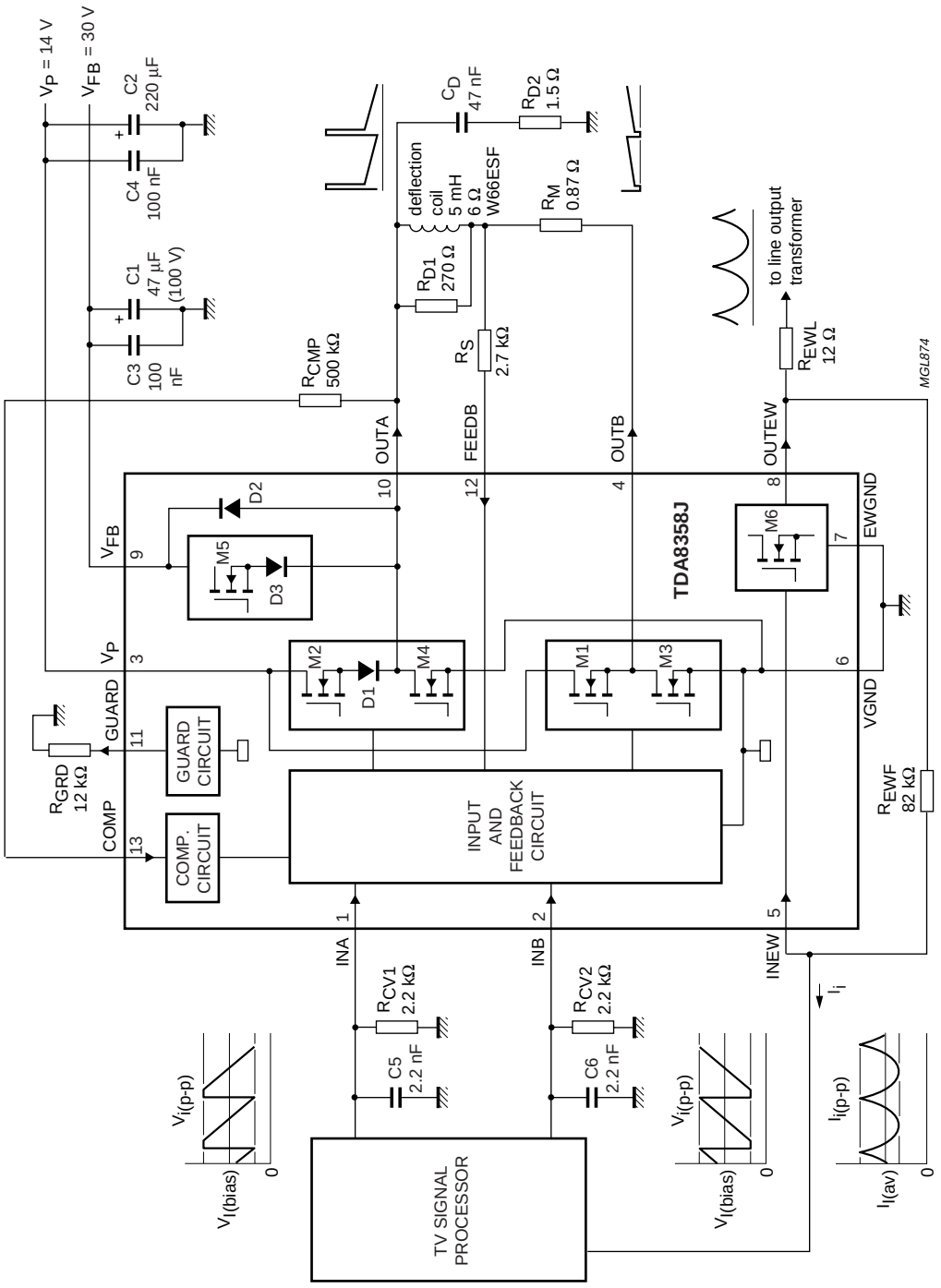


Fig.3 Test diagram.



f_{vert} = 50 Hz; t_{FB} = 640 µs; $I_{I(bias)}$ = 400 µA; $I_{i(p-p)}$ = 475 µA; $I_{o(p-p)}$ = 2.4 A.

Fig.4 Application diagram.

R_M calculation

Before calculating the measuring resistor (R_M), the differential input voltage [$V_{i(dif)}$] has to be known. This voltage can be measured between pins INA and INB. The calculation is as follows: $R_M = \frac{V_{i(dif)(p-p)}}{I_{o(p-p)}}$

Most of the TV signal processors from Philips have a current output. This current has to be converted by resistors at the input of the TDA8358J (R_{CV1} and R_{CV2}). The voltage across these resistors can be calculated. The differential input voltage is given in the following equation (see also Fig 5):

$V_{i(dif)(p-p)} = I_{i1(p-p)} \times R_{CV1} - [-I_{i2(p-p)}] \times R_{CV2}$

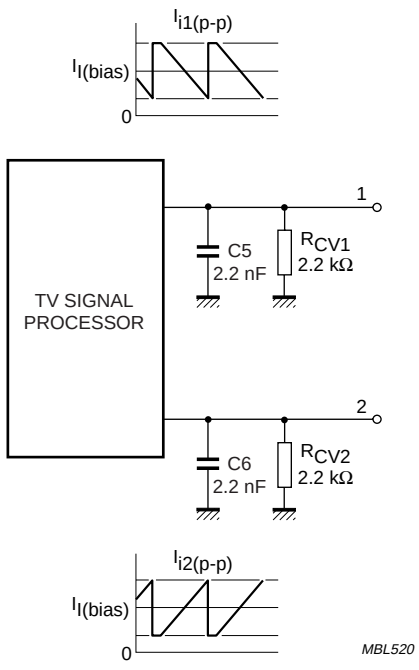


Fig.5 Differential input voltage.

Values for these currents are, for instance:
$I_{i(bias)}$ = 400 µA; $I_{i1(p-p)} = I_{i2(p-p)}$ = 475 µA.

Therefore the differential input voltage be as follows:
$V_{i(dif)(p-p)}$ = 475 µA × 2.2 kΩ − (−475 µA × 2.2 kΩ)
= 2.09 V

Supply voltage calculation

For calculating the minimum required supply voltage, several specific application parameter values have to be known. These parameters are the required maximum (peak) deflection coil current $I_{coil(peak)}$, the coil impedance R_{coil} and L_{coil} and the measuring resistance of R_M. The required maximum (peak) deflection coil current should also include the overscan.

The deflection coil resistance has to be multiplied by 1.2 in order to take account of hot conditions.

Chapter “Characteristics” supplies values for the voltage losses of the vertical output stage. For the first part of the scan the voltage loss is given by $V_{loss(1)}$. For the second part of the scan the voltage loss is given by $V_{loss(2)}$.

The voltage drop across the deflection coil during scan is determined by the coil impedance. For the first part of the scan the inductive contribution and the ohmic contribution to the total coil voltage drop are of opposite sign, while for the second part of the scan the inductive part and the ohmic part have the same sign.

For the vertical frequency the maximum frequency occurring must be applied to the calculations.

The required power supply voltage V_P for the first part of the scan is given by:

$$V_{P(1)} = I_{coil(peak)} \times (R_{coil} + R_M) - L_{coil} \times 2I_{coil(peak)} \times f_{vert(max)} + V_{loss(1)}$$

The required power supply voltage V_P for the second part of the scan is given by:

$$V_{P(2)} = I_{coil(peak)} \times (R_{coil} + R_M) + L_{coil} \times 2I_{coil(peak)} \times f_{vert(max)} + V_{loss(2)}$$

The minimum required supply voltage V_P shall be the highest of the two values $V_{P(1)}$ and $V_{P(2)}$. Spread in supply voltage and component values also has to be taken into account.

Flyback supply voltage calculation

If the flyback time is known, the required flyback supply voltage can be calculated by the simplified formula:

$$V_{FB} = I_{coil(p-p)} \times \frac{R_{coil} + R_M}{1 - e^{-t_{FB}/x}}$$

where:

$$x = \frac{L_{coil}}{R_{coil} + R_M}$$

The flyback supply voltage calculated this way is approximately 5% to 10% higher than required.

Calculation of the power dissipation of the vertical output stage

The power dissipation of the vertical output stage is given by the formula:

$P_V = P_{sup} - P_L$

The power to be supplied is given by the formula:

$$P_{sup} = V_P \times \frac{I_{coil(peak)}}{2} + V_P \times 0.015\ [A] + 0.3\ [W]$$

In this formula 0.3 [W] represents the average value of the losses in the flyback supply.

The average external load power dissipation in the deflection coil and the measuring resistor is given by the formula:

$$P_L = \frac{(I_{coil(peak)})^2}{3} \times (R_{coil} + R_M)$$

Example

Table 1 Application values

SYMBOL	VALUE	UNIT
$I_{coil(peak)}$	1.2	A
$I_{coil(p-p)}$	2.4	A
L_{coil}	5	mH
R_{coil}	6	Ω
R_M	0.6	Ω
f_{vert}	50	Hz
t_{FB}	640	µs

Table 2 Calculated values

SYMBOL	VALUE	UNIT
V_P	14	V
$R_M + R_{coil}$ (hot)	7.8	Ω
t_{vert}	0.02	s
x	0.000641	
V_{FB}	30	V
P_{sup}	8.91	W
P_L	3.74	W
P_V	5.17	W

Power dissipation calculation for the east-west stage

In general the shape of the east-west output wave form is a parabola. The output voltage will be higher at the beginning and end of the vertical scan compared to the voltage at the scan middle, while the output current will be higher at the scan middle. This results in an almost uniform power dissipation distribution during scan. Therefore the power dissipation can be calculated by multiplying the average values of the output voltage and the output current of pin OUTEW.

When verifying the dissipation the switch-on and switch-off dissipation should also be taken into account. Power dissipation during start-up can be 3 to 5 times higher than during normal operation.

Heatsink calculation

The value of the heatsink can be calculated in a standard way with a method based on average temperatures. The required thermal resistance of the heatsink is determined by the maximum die temperature of 150 °C. **In general we recommend a design for an average die temperature not exceeding 130 °C.** It should be noted that the heatsink thermal resistance $R_{th(h-a)}$ found by performing a standard calculation will be lower then normally found for a vertical deflection stand alone device, due to the contribution of the EW power dissipation to this value.

EXAMPLE

Measured or known values:

P_{EW} = 3 W; P_V = 6 W; T_{amb} = 40 °C; T_j = 130 °C; $R_{th(j-c)}$ = 4 K/W; $R_{th(c-h)}$ = 1 K/W.

The required heatsink thermal resistance is given by:

$$R_{th(h-a)} = \frac{T_j - T_{amb}}{P_{EW} + P_V} - (R_{th(j-c)} + R_{th(c-h)})$$

When we use the values known we find:

$$R_{th(h-a)} = \frac{130 - 40}{3 + 6} - (4 + 1) = 5\ K/W$$

The heatsink temperature will be:

$T_h = T_{amb} + R_{th(h-a)} \times P_{tot} = 40 + 5 \times 9 = 85$ °C

Equivalent thermal resistance network

The TDA8358J has two independent power dissipating systems, the vertical output circuit and the east-west circuit.

It is recommended to verify the individual maximum (peak) junction temperatures of both circuits. Therefore the maximum (peak) power dissipations of the circuits and also the heatsink temperature should be measured. The maximum (peak) junction temperatures can be calculated by using an equivalent thermal network (see Fig.6).

The network only includes the contribution of the maximum (peak) power dissipation $P_{TRv(peak)}$, being the dissipation of the most critical transistor internally connected to pins OUTA and VGND. The model assumes equivalent maximum (peak) power dissipations during the different vertical scan stages for all the functionally paired transistors. The calculated maximum (peak) junction temperatures should not exceed T_j = 150 °C.

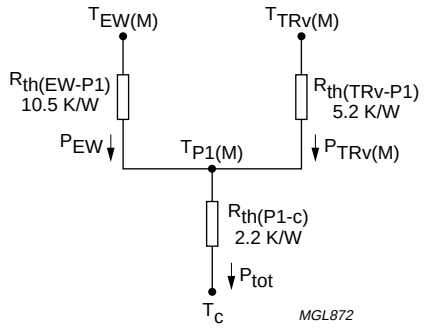


Fig.6 Equivalent thermal resistance network.

EXAMPLE

Measured or known values:

- The east-west power dissipation: P_{EW} = 3 W
- The vertical power dissipation: P_V = 6 W
- The maximum (peak) power dissipation of the most critical transistor: $P_{TRv(peak)}$ = 5 W
- The case temperature: T_c = 85 °C.

The IC total power dissipation is:

$P_{tot} = P_{EW} + P_V = 6 + 3 = 9$ W

It should be noted that the allowed IC total power dissipation is P_{tot} = 15 W (maximum value).

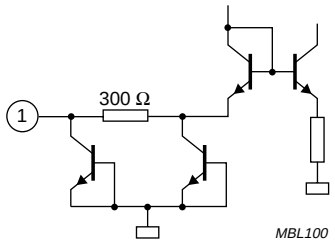
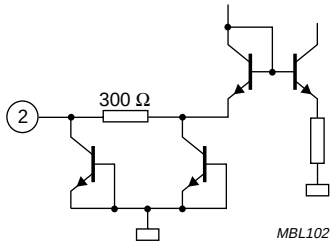
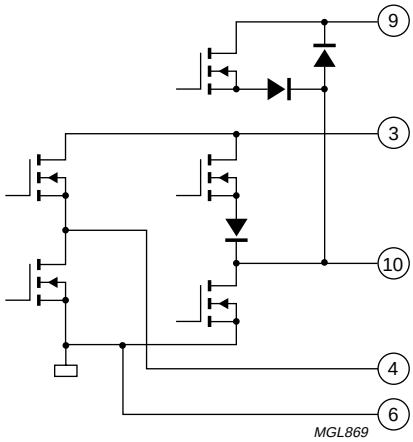
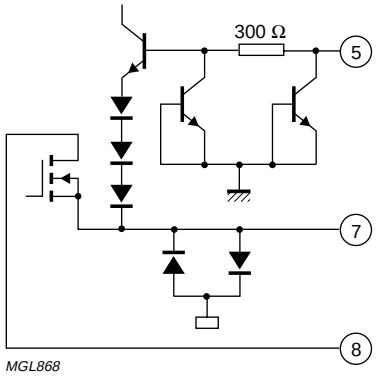
The maximum (peak) temperature $T_{P1(peak)}$ is given by:

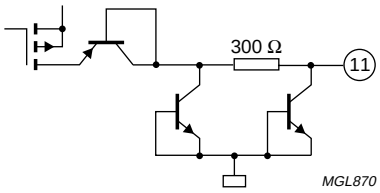
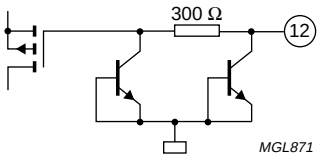
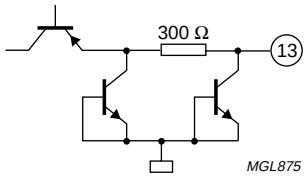
- $T_{P1(peak)} = T_c + (P_{EW} + P_{TRv(peak)}) \times R_{th(P1-c)}$
  $= 85 + (3 + 5) \times 2.2 = 102.6$ °C

The maximum (peak) junction temperatures for the output circuits are given by:

- $T_{j(EW)(peak)} = T_{P1(peak)} + R_{th(EW-P1)} \times P_{EW}$
  $= 102.6 + 10.5 \times 3 = 134.1$ °C
- $T_{j(TRv)(peak)} = T_{P1(peak)} + R_{th(TRv-P1)} \times P_{TRv(peak)}$
  $= 102.6 + 5.2 \times 5 = 128.6$ °C

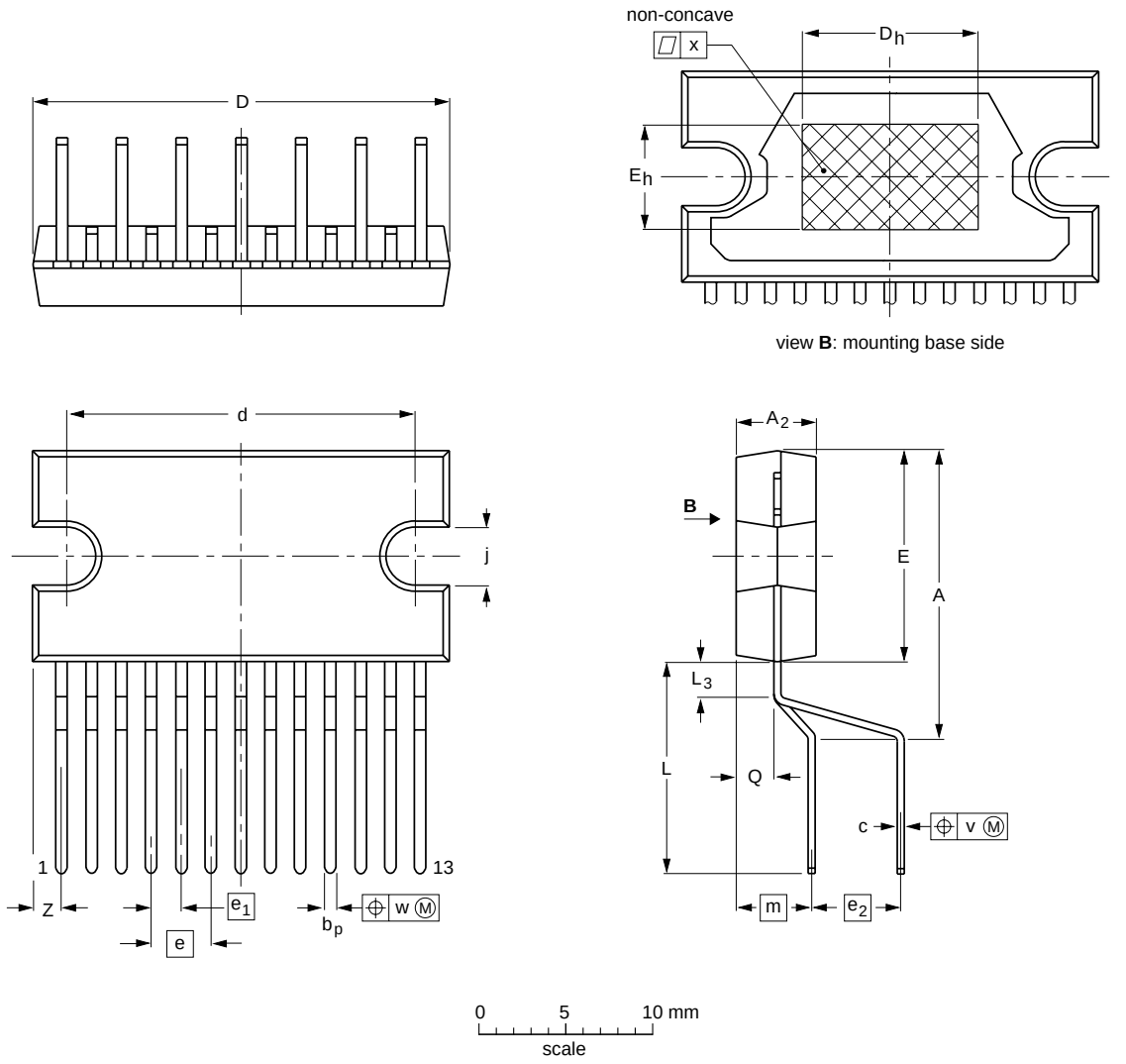
INTERNAL PIN CONFIGURATION

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	INA	
2	INB	
3	V_P	
4	OUTB	
6	VGND	
9	V_{FB}	
10	OUTA	
5	INEW	
7	EWGND	
8	OUTEW	

PIN	SYMBOL	EQUIVALENT CIRCUIT
11	GUARD	
12	FEEDB	
13	COMP	

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm) **SOT141-6**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						~~97-12-16~~ 99-12-17

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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