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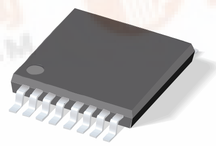


TPS40050
TPS40051
TPS40053

SLUS540B – DECEMBER 2002 – REVISED MARCH 2003

WIDE-INPUT SYNCHRONOUS BUCK CONTROLLER

FEATURES

- **Operating Input Voltage 8 V to 40 V**
- **Input Voltage Feed-Forward Compensation**
- **< 1 % Internal 0.7-V Reference**
- **Programmable Fixed-Frequency Up to 1 MHz Voltage Mode Controller**
- **Internal Gate Drive Outputs for High-Side and Synchronous N-Channel MOSFETs**
- **16-Pin PowerPAD™ Package (θ_{JC} = 2°C/W)**
- **Thermal Shutdown**
- **Externally Synchronizable**
- **Programmable High-Side Current Limit**
- **Programmable Closed-Loop Soft-Start**
- **TPS40050 Source Only**
- **TPS40051 Source/Sink**
- **TPS40053 Source/Sink With V_{OUT} Prebias**

APPLICATIONS

- **Networking Equipment**
- **Telecom Equipment**
- **Base Stations**
- **Servers**

DESCRIPTION

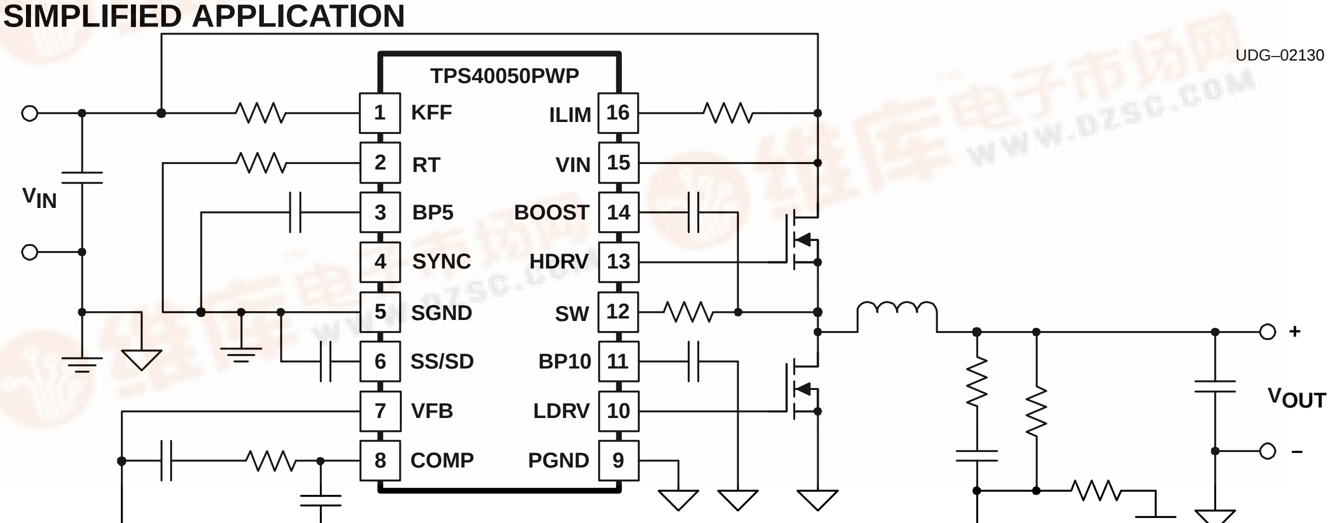
The TPS4005x is a family of high-voltage, wide input (8 V to 40 V), synchronous, step-down converters. The TPS4005x family offers design flexibility with a variety of user programmable functions, including soft-start, UVLO, operating frequency, voltage feed-forward, high-side current limit, and loop compensation.

The TPS4005x are also synchronizable to an external supply. They incorporate MOSFET gate drivers for external N-channel high-side and synchronous rectifier (SR) MOSFETs. Gate drive logic incorporates anti-cross conduction circuitry to prevent simultaneous high-side and synchronous rectifier conduction. The TPS40051 and TPS40053 permit the output to sink current by allowing the synchronous rectifier to turn on without the switch node (SW) first collapsing.

The TPS4005x uses voltage feed-forward control techniques to provide good line regulation over the wide (4:1) input voltage range, and fast response to input line transients with near constant gain with input variation which eases loop compensation.

The externally programmable current limit provides pulse-by-pulse current limit, as well as hiccup mode operation utilizing an internal fault counter for longer duration overloads.

SIMPLIFIED APPLICATION



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	LOAD CURRENT	PACKAGE	PART NUMBER
–40°C to 85°C	SOURCE	Plastic HTSSOP (PWP)(1)	TPS40050PWP
	SOURCE/SINK	Plastic HTSSOP (PWP)(1)	TPS40051PWP
	SOURCE/SINK(2)	Plastic HTSSOP (PWP)(1)	TPS40053PWP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS40050PWPR). See the application section of the data sheet for PowerPAD drawing and layout information.

(2) Source only mode (DCM) during soft-start only. Source/sink during normal operation.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

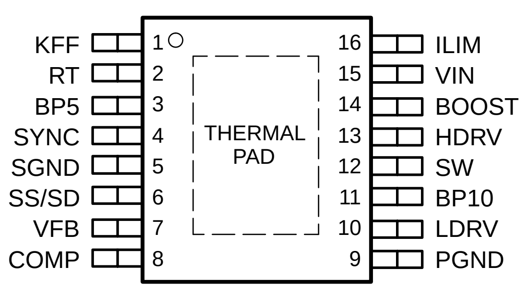
		TPS40050 TPS40051 TPS40053	UNIT
Input voltage range, VI	VIN	45	V
	VFB, KFF, SS, SYNC	–0.3 to 6	
	SW	–0.3 to 45	
	SW, transient < 50 ns	–2.5	
Output voltage range, V_O	COMP, KFF, RT, SS	–0.3 to 6	
Output current, I_{OUT}	RT	200	μA
Operating virtual junction temperature range, T_J		–40 to 125	°C
Storage temperature, T_{stg}		–55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I	8		40	V
Operating free-air temperature, T_A	–40		85	°C

PWP PACKAGE(3)(4)
(TOP VIEW)



(3) For more information on the PWP package, refer to TI Technical Brief, Literature No. SLMA002.
(4) PowerPAD™ heat slug must be connected to SGND (pin 5) or electrically isolated from all other pins.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range, VIN		8		40	V
OPERATING CURRENT						
I_{DD}	Quiescent current	Output drivers not switching		1.5	3.0	mA
BP5						
V_{BP5}	Input voltage		4.7	5.0	5.2	V
OSCILLATOR/RAMP GENERATOR(3)						
f_{OSC}	Accuracy	R_T = 90.9 kΩ	480	500	550	kHz
V_{RAMP}	PWM ramp voltage(1)	V_{PEAK}–V_{VAL}		2.0		V
V_{IH}	High-level input voltage, SYNC		2		5	
V_{IL}	Low-level input voltage, SYNC				0.8	V
I_{SYNC}	Input current, SYNC			5	10	µA
	Pulse width, SYNC		50			ns
V_{RT}	RT voltage		2.38	2.50	2.58	V
	Maximum duty cycle	V_{FB} = 0 V, f_{SW} ≤ 500 kHz	85%		94%	
		V_{FB} = 0 V, 500 kHz ≤ f_{SW} ≤ 1 MHz	80%			
	Minumum duty cycle	V_{FB} ≥ 0.75 V			0%	
V_{KFF}	Feed-forward voltage		3.35	3.48	3.65	V
I_{KFF}	Feed-forward current operating range(1)		20		1100	µA
SOFT START						
I_{SS}	Soft-start source current		1.75	2.35	2.85	µA
V_{SS}	Soft-start clamp voltage			3.7		V
t_{DSCH}	Discharge time	C_{SS} = 220 pF	1.6	2.2	2.8	µs
t_{SS}	Soft-start time	C_{SS} = 220 pF, 0 V ≤ V_{SS} ≤ 1.6 V	115	155	205	
BP10						
V_{BP10}	Input voltage		9.0	9.6	10.3	V
ERROR AMPLIFIER						
V_{FB}	Feedback input voltage	T_A = 25°C	0.698	0.700	0.704	V
		0°C ≤ T_A ≤ 85°C	0.690	0.700	0.707	
		–40°C ≤ T_A ≤ 85°C	0.690	0.700	0.715	
G_{BW}	Gain bandwidth		3.0	5.0		MHz
A_{VOL}	Open loop gain		60	80		dB
I_{OH}	High-level output source current		2.0	4.0		mA
I_{OL}	Low-level output sink current		2.5	4.0		
V_{OH}	High-level output voltage	I_{SOURCE} = 500 µA	3.2	3.5		V
V_{OL}	Low-level output voltage	I_{SINK} = 500 µA		0.20	0.35	
I_{BIAS}	Input bias current	V_{FB} = 0.7 V		100	200	nA

(1) Ensured by design. Not production tested.
(2) All parameters measured at zero power dissipation.
(3) I_{KFF} increases with SYNC frequency, I_{KFF} decreases with maximum duty cycle

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ELECTRICAL CHARACTERISTICS

T_J = –40°C to 85°C, V_{IN} = 24 V_{dc}, R_T = 90.9 kΩ, I_{KFF} = 150 µA, f_{SW} = 500 kHz (unless otherwise noted)

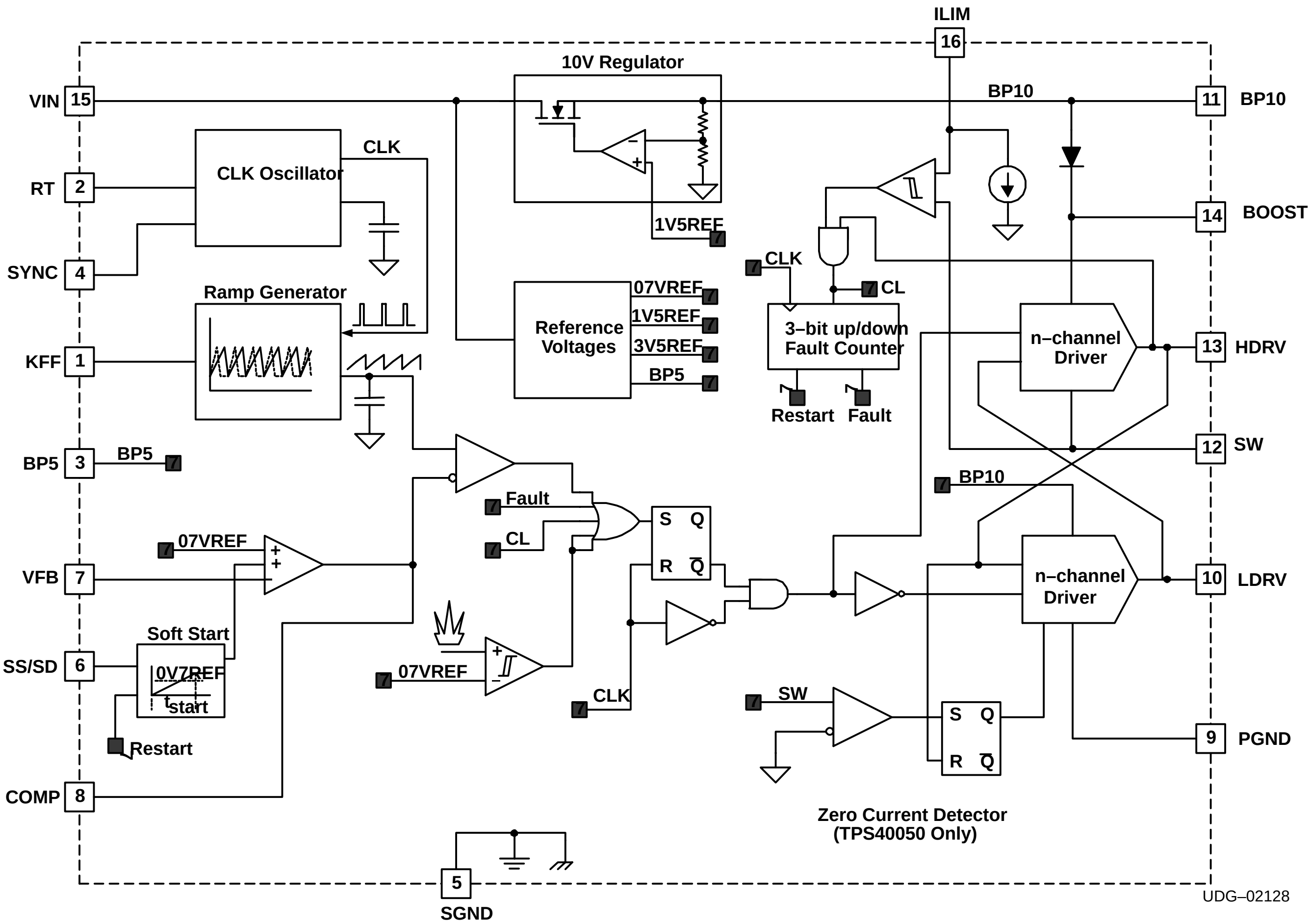
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{SINK}	Current limit sink current		8.6	10.0	11.5	µA
	Propagation delay to output	V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 0.5 V)		300		ns
		V_{ILIM} = 23.7 V, V_{SW} = (V_{ILIM} – 2 V)		200		
t_{ON}	Switch leading-edge blanking pulse time(1)		100			
t_{OFF}	Off time during a fault			7		cycles
V_{OS}	Offset voltage SW vs. ILIM	T_A = 25°C	–125		–30	mV
		V_{ILIM} = 23.6 V, 0°C ≤ T_A ≤ 85°C	–140	–75	–15	
		V_{ILIM} = 23.6 V, –40°C ≤ T_A ≤ 85°C	–140		10	
OUTPUT DRIVER						
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 2200 pF		48	96	ns
t_{LFALL}	Low-side driver fall time			24	48	
t_{HRISE}	High-side driver rise time	C_{LOAD} = 2200 pF, (HDRV – SW)		48	96	
t_{HFALL}	High-side driver fall time			36	72	
V_{OH}	High-level ouput voltage, HDRV	I_{HDRV} = –0.1 A (HDRV – SW)	BOOST –1.5 V	BOOST –1.0 V		V
V_{OL}	Low-level ouput voltage, HDRV	I_{HDRV} = 0.1 A (HDRV – SW)			0.75	
V_{OH}	High-level ouput voltage, LDRV	I_{LDRV} = –0.1 A	BP10 –1.4 V	BP10 – 1.0 V		
V_{OL}	Low-level ouput voltage, LDRV	I_{LDRV} = 0.1 A			0.5	
	Minimum controllable pulse width			100	150	ns
SS/SD SHUTDOWN						
V_{SD}	Shutdown threshold voltage	Outputs off	90	125	150	mV
V_{EN}	Device active threshold voltage		190	210	245	
BOOST REGULATOR						
V_{BOOST}	Output voltage	V_{IN} = 24.0 V	31.5	32.5	33.5	V
RECTIFIER ZERO CURRENT COMPARATOR (TPS40050/TPS40053 SS ONLY)						
V_{SW}	Switch voltage	LDRV output OFF	–5.5	–0.5	4.5	mV
SW NODE						
I_{LEAK}	Leakage current(1)				25	µA
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature(1)			165		°C
	Hysteresis(1)			20		
UVLO						
V_{UVLO}	KFF programmable threshold voltage	R_{KFF} = 39.2 kΩ	8.19	9.00	9.58	V

(1) Ensured by design. Not production tested.
(2) All parameters measured at zero power dissipation.
(3) I_{KFF} increases with SYNC frequency, I_{KFF} decreases with maximum duty cycle

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOST	14	O	Gate drive voltage for the high side N-channel MOSFET. The BOOST voltage is 9 V greater than the input voltage. A 0.1-µF ceramic capacitor should be connected from this pin to the SW pin.
BP5	3	O	5-V reference. This pin should be bypassed to ground with a 0.1-µF ceramic capacitor. **This pin is not for external use.**
BP10	11	O	10-V reference used for gate drive of the N-channel synchronous rectifier. This pin should be bypassed by a 1-µF ceramic capacitor. **This pin is not for external use.**
COMP	8	O	Output of the error amplifier, input to the PWM comparator. A feedback network is connected from this pin to the VFB pin to compensate the overall loop. The comp pin is internally clamped above the peak of the ramp to improve large signal transient response.
HDRV	13	O	Floating gate drive for the high-side N-channel MOSFET. This pin switches from BOOST (MOSFET on) to SW (MOSFET off).
ILIM	16	I	Current limit pin, used to set the overcurrent threshold. An internal current sink from this pin to ground sets a voltage drop across an external resistor connected from this pin to VCC. The voltage on this pin is compared to the voltage drop (VIN –SW) across the high side MOSFET during conduction.
KFF	1	I	A resistor is connected from this pin to VIN to program the amount of voltage feed-forward. The current fed into this pin is internally divided and used to control the slope of the PWM ramp.
LDRV	10	O	Gate drive for the N-channel synchronous rectifier. This pin switches from BP10 (MOSFET on) to ground (MOSFET off).
PGND	9	–	Power ground reference for the device. There should be a low-impedance path from this pin to the source(s) of the lower MOSFET(s).
RT	2	I	A resistor is connected from this pin to ground to set the internal oscillator and switching frequency.
SGND	5	–	Signal ground reference for the device.
SS/SD	6	I	Soft-start programming pin. A capacitor connected from this pin to ground programs the soft-start time. The capacitor is charged with an internal current source of 2.3 µA. The resulting voltage ramp on the SS pin is used as a second non-inverting input to the error amplifier. Output voltage regulation is controlled by the SS voltage ramp until the voltage on the SS pin reaches the internal reference voltage of 0.7 V. Pulling this pin low disables the controller.
SW	12	I	This pin is connected to the switched node of the converter and used for overcurrent sensing. The TPS40050 and TPS40053 versions use this pin for zero current sensing as well.
SYNC	4	I	Syncronization input for the device. This pin can be used to synchronize the oscillator to an external master frequency.
VFB	7	I	Inverting input to the error amplifier. In normal operation the voltage on this pin is equal to the internal reference voltage, 0.7 V.
VIN	15	I	Supply voltage for the device.

SIMPLIFIED BLOCK DIAGRAM



APPLICATION INFORMATION

SETTING THE SWITCHING FREQUENCY (PROGRAMMING THE CLOCK OSCILLATOR)

The TPS4005x has independent clock oscillator and ramp generator circuits. The clock oscillator serves as the master clock to the ramp generator circuit. The switching frequency, f_{SW} in kHz, of the clock oscillator is set by a single resistor (R_T) to ground. The clock frequency is related to R_T, in kΩ by equation (1) and the relationship is charted in Figure 2.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \right) k\Omega \qquad (1)$$

PROGRAMMING THE RAMP GENERATOR CIRCUIT

The ramp generator circuit provides the actual ramp used by the PWM comparator. The ramp generator provides voltage feed-forward control by varying the PWM ramp slope with line voltage, while maintaining a constant ramp magnitude. Varying the PWM ramp directly with line voltage provides excellent response to line variations since the PWM does not have to wait for loop delays before changing the duty cycle. (See Figure 1).

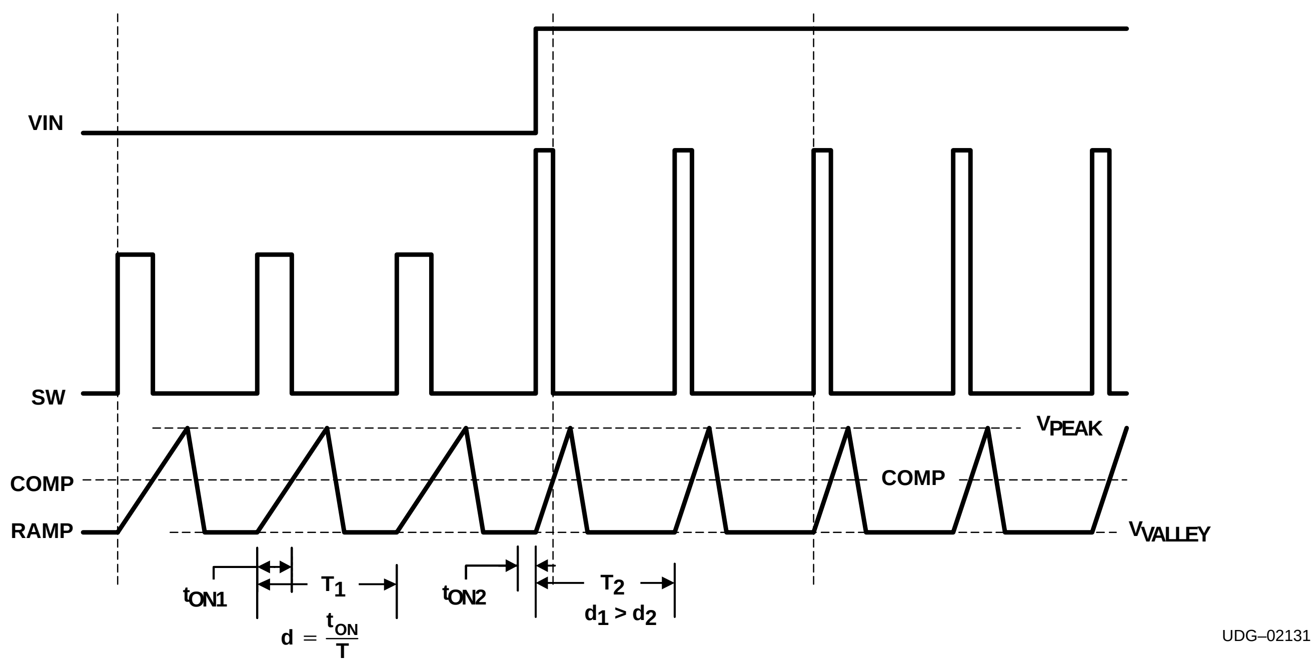


Figure 1. Voltage Feed-Forward Effect on PWM Duty Cycle

APPLICATION INFORMATION

The PWM ramp must be faster than the master clock frequency or the PWM is prevented from starting. The PWM ramp time is programmed via a single resistor (R_{KFF}) pulled up to VIN. R_{KFF} is related to R_T, and the minimum input voltage, $V_{IN(min)}$ through the following:

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5\right) \times \left(58.14 \times R_T + 1340\right)\,\Omega \quad (2)$$

where:

- $V_{IN(min)}$ is the ensured minimum start-up voltage. The actual start-up voltage is nominally about 10% lower at 25°C.
- R_T is the timing resistance in kΩ

The curve showing the R_{KFF} required for a given switching frequency, f_{SW}, is shown in Figure 3.

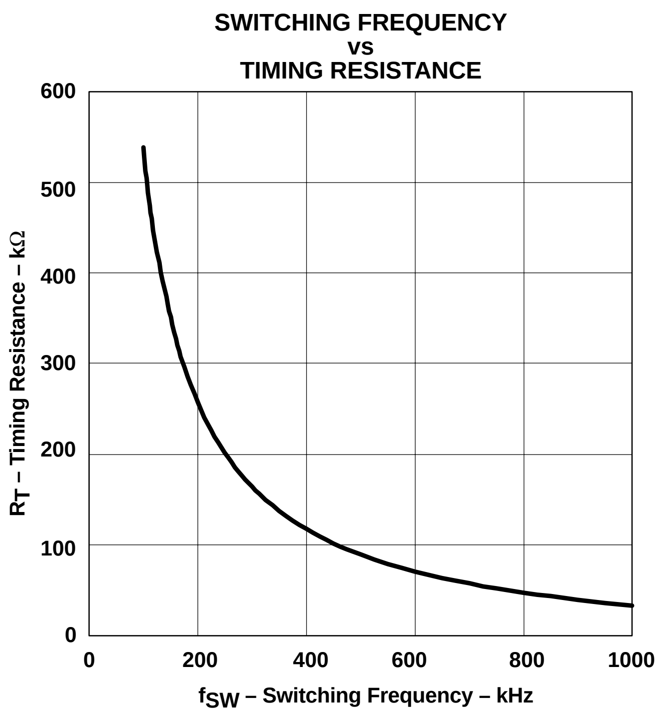


Figure 2

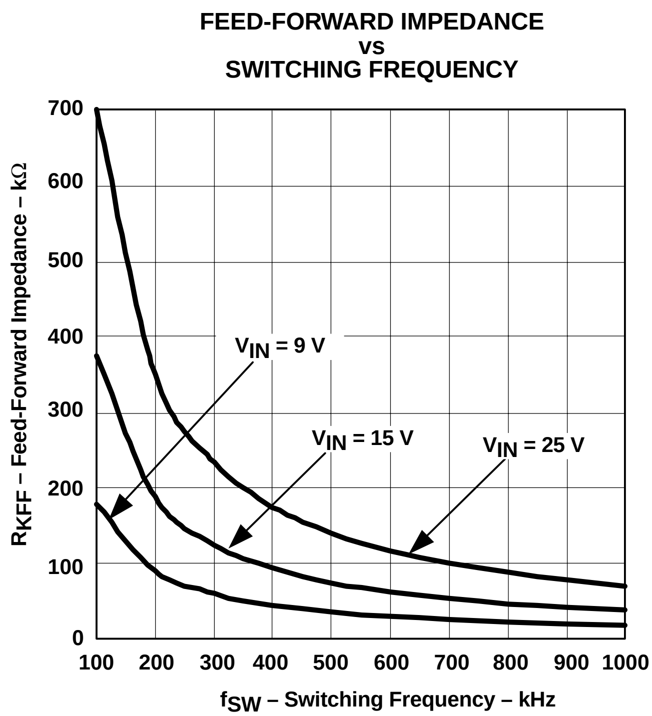


Figure 3

APPLICATION INFORMATION

UVLO OPERATION

The TPS4005x uses variable (user programmable) UVLO protection. The UVLO circuit holds the soft-start low until the input voltage has exceeded the user programmable undervoltage threshold.

The TPS4005x uses the feed-forward pin, KFF, as a user programmable low-line UVLO detection. This variable low-line UVLO threshold compares the PWM ramp duration to the oscillator clock period. An undervoltage condition existis if the TPS4005x receives a clock pulse before the ramp has reached 90% of its full amplitude. The ramp duration is a function of the ramp slope, which is directly related to the current into the KFF pin. The KFF current is a function of the input voltage and the resistance from KFF to the input voltage. The KFF resistor can be referenced to the oscillator frequency as descibed in equation (3):

$$R_{KFF} = \left(V_{IN\,(min)} - 3.5\right) \times \left(58.14 \times R_T + 1340\right)\ \Omega \tag{3}$$

where:.

- V_{IN} is the desired start-up (UVLO) input voltage

The variable UVLO function uses a three–bit full adder to prevent spurious shut-downs or turn-ons due to spikes or fast line transients. When the adder reaches a total of seven counts in which the ramp duration is shorter than the clock cycle a powergood signal is asserted and a soft-start initiated, and the upper and lower MOSFETS are turned off.

Once the soft-start is initiated, the UVLO cicruit must see a total count of seven cycles in which the ramp duration is longer than the clock cycle before an undervoltage condition is declared. (See Figure 4).

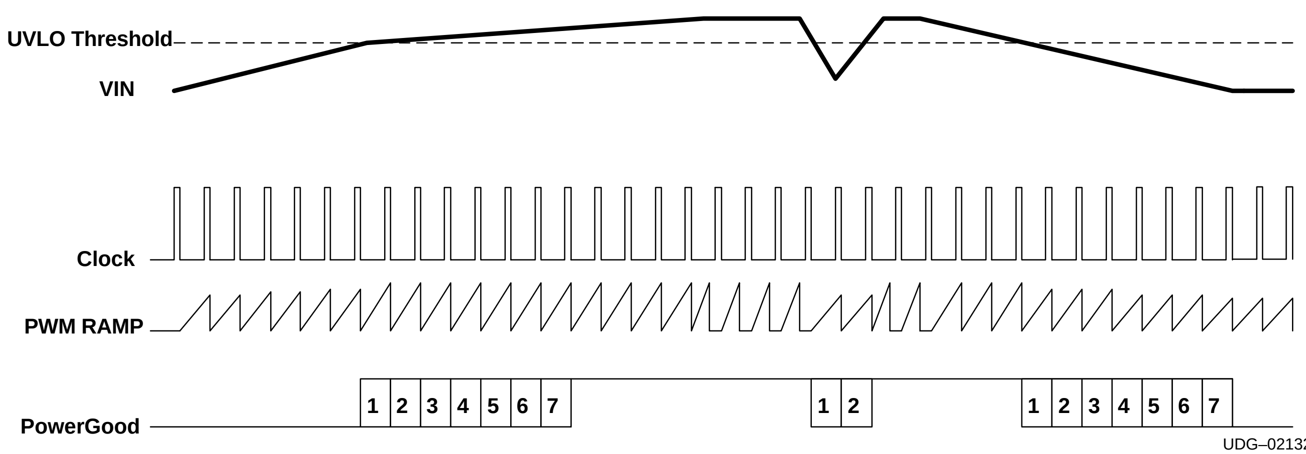


Figure 4. Undervoltage Lockout Operation

Some applications may require an additional circuit to prevent false restarts at the UVLO voltage level. This applies to applications which have high impedance on the input voltage line or which have excessive ringing on the V_{IN} line. The input voltage impedance can cause the input voltage to sag enough at start-up to cause a UVLO shutdown and subsequent restart. Excessive ringing can also affect the voltage seen by the device and cause a UVLO shutdown and restart. A simple external circuit provides a selectable amount of hysteresis to prevent the nuisance UVLO shutdown.

APPLICATION INFORMATION

Assuming a hysteresis current of 10% I_{KFF}, and the peak detector charges to 8 V and $V_{IN(min)}$ = 18 V, the value of R_A is calculated by:

$$R_A = \frac{R_{KFF} \times (8 - 3.5)}{0.1 \times \left(V_{IN(min)} - 3.5\right)} = 565\ k\Omega \cong 562\ k\Omega \quad (4)$$

C_A is chosen to maintain the peak voltage between switching cycles. To keep the capacitor charge from drooping 0.1-V, or from 8 V to 7.9 V.

$$C_A = \frac{(8 - 3.5)}{\left(R_A \times 7.9 \times f_{SW}\right)} \quad (5)$$

The value of C_A imay calculate to less than 10 pF, but some standard value up to 470 pF works adequately. The diode can be a small signal switching diode or Schottky rated for more then 20 V. Figure 5 illustrates a typical implementation using a small switching diode.

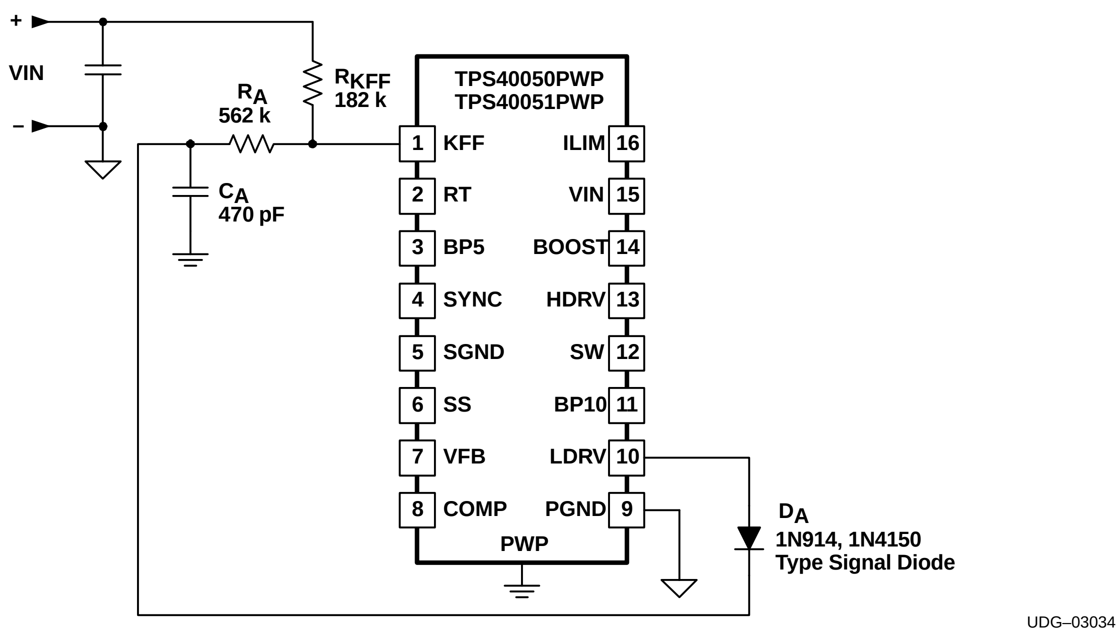


Figure 5. Hysteresis for Programmable UVLO

APPLICATION INFORMATION

SELECTING THE INDUCTOR VALUE

The inductor value determines the magnitude of ripple current in the output capacitors as well as the load current at which the converter enters discontinuous mode. Too large an inductance results in lower ripple current but is physically larger for the same load current. Too small an inductance results in larger ripple currents and a greater number of (or more expensive output capacitors for) the same output ripple voltage requirement. A good compromise is to select the inductance value such that the converter doesn't enter discontinuous mode until the load approximated somewhere between 10% and 30% of the rated output. The inductance value is described in equation (6).

$$L = \frac{\left(V_{IN} - V_O\right) \times V_O}{V_{IN} \times \Delta I \times f_{SW}} \quad \text{(Henries)} \tag{6}$$

where:.

- V_O is the output voltage
- ΔI is the peak-to-peak inductor current

CALCULATING THE OUTPUT CAPACITANCE

The output capacitance depends on the output ripple voltage requirement, output ripple current, as well as any output voltage deviation requirement during a load transient.

The output ripple voltage is a function of both the output capacitance and capacitor ESR. The worst case output ripple is described in equation (7).

$$\Delta V = \Delta I \left[ESR + \left(\frac{1}{8 \times C_O \times f_{SW}} \right) \right] \quad V_{P-P} \tag{7}$$

The output ripple voltage is typically between 90% and 95% due to the ESR component.

The output capacitance requirement typically increases in the presence of a load transient requirement. During a step load, the output capacitance must provide energy to the load (light to heavy load step) or absorb excess inductor energy (heavy to light load step) while maintaining the output voltage within acceptable limits. The amount of capacitance depends on the magnitude of the load step, the speed of the loop and the size of the inductor.

Stepping the load from a heavy load to a light load results in an output overshoot. Excess energy stored in the inductor must be absorbed by the output capacitance. The energy stored in the inductor is described in equation (8).

$$E_L = \frac{1}{2} \times L \times I^2 \quad \text{(Joules)} \tag{8}$$

where:

$$I^2 = \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right] \quad \left(\text{(Amperes)}^2\right) \tag{9}$$

where:

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions

APPLICATION INFORMATION

Energy in the capacitor is described in equation (10).

$$E_C = \frac{1}{2} \times C \times V^2 \quad \text{(Joules)} \tag{10}$$

where:

$$V^2 = \left[\left(V_f\right)^2 - \left(V_i\right)^2 \right] \quad \left(\text{Volts}^2\right) \tag{11}$$

where:

- V_f is the final peak capacitor voltage
- V_i is the initial capacitor voltage

Substituting equation (9) into equation (8), then substituting equation (11) into equation (10), then setting equation (11) equal to equation (10), and then solving for C_O yields the capacitance described in equation (12).

$$C_O = \frac{L \times \left[\left(I_{OH}\right)^2 - \left(I_{OL}\right)^2 \right]}{\left[\left(V_f\right)^2 - \left(V_i\right)^2 \right]} \quad \text{(Farads)} \tag{12}$$

PROGRAMMING SOFT START

TPS4005x uses a closed-loop approach to ensure a controlled ramp on the output during start-up. Soft-start is programmed by charging an external capacitor (C_{SS}) via an internally generated current source. The voltage on C_{SS} is fed into a separate non-inverting input to the error amplifier (in addition to FB and 0.7-V VREF). The loop is closed on the lower of the C_{SS} voltage or the internal reference voltage (0.7-V VREF). Once the C_{SS} voltage rises above the internal reference voltage, regulation is based on the internal reference. To ensure a controlled ramp-up of the output voltage the soft-start time should be greater than the L-C_O time constant as described in equation (13).

$$t_{START} \geq 2\pi \times \sqrt{L \times C_O} \quad \text{(seconds)} \tag{13}$$

There is a direct correlation between t_{START} and the input current required during start-up. The faster t_{START}, the higher the input current required during start-up. This relationship is describe in more detail in the section titled, *Programming the Current Limit* which follows. The soft-start capacitance, C_{SS}, is described in equation (14).

For applications in which the V_{IN} supply ramps up slowly, (typically between 50 ms and 100 ms) it may be necessary to increase the soft-start time to between approximately 2 ms and 5 ms to prevent nuisance UVLO tripping. The soft-start time should be longer than the time that the V_{IN} supply transitions between 6 V and 7 V.

$$C_{SS} = \frac{2.3\ \mu A}{0.7\ V} \times t_{START} \quad \text{(Farads)} \tag{14}$$

APPLICATION INFORMATION

PROGRAMMING CURRENT LIMIT

The TPS4005x uses a two-tier approach for overcurrent protection. The first tier is a pulse-by-pulse protection scheme. Current limit is implemented on the high-side MOSFET by sensing the voltage drop across the MOSFET when the gate is driven high. The MOSFET voltage is compared to the voltage dropped across a resistor connected from VIN pin to the ILIM pin when driven by a constant current sink. If the voltage drop across the MOSFET exceeds the voltage drop across the ILIM resistor, the switching pulse is immediately terminated. The MOSFET remains off until the next switching cycle is initiated.

The second tier consists of a fault counter. The fault counter is incremented on an overcurrent pulse and decremented on a clock cycle without an overcurrent pulse. When the counter reaches seven (7) a restart is issued and seven soft-start cycles are initiated. Both the upper and lower MOSFETs are turned off during this period. The counter is decremented on each soft-start cycle. When the counter is decremented to zero, the PWM is re-enabled. If the fault has been removed the output starts up normally. If the output is still present the counter counts seven overcurrent pulses and re-enters the second-tier fault mode. See Figure 6 for typical overcurrent protection waveforms.

The minimum current limit setpoint (I_{LIM}) depends on t_{START}, C_O, V_O, and the load current at turn-on (I_L).

$$I_{LIM} = \left[\frac{\left(C_O \times V_O\right)}{t_{START}} \right] + I_L \quad \text{(Amperes)} \tag{15}$$

The current limit programming resistor (R_{ILIM}) is calculated using equation (16).

$$R_{ILIM} = \frac{I_{OC} \times R_{DS(on)[max]}}{1.12 \times I_{SINK}} + \frac{V_{OS}}{I_{SINK}} \quad (\Omega) \tag{16}$$

where:

- I_{SINK} is the current into the ILIM pin and is nominally 10 μA,
- I_{OC} is the overcurrent setpoint which is the DC output current plus one-half of the peak inductor current
- V_{OS} is the overcurrent comparator offset and is nominally –48 mV

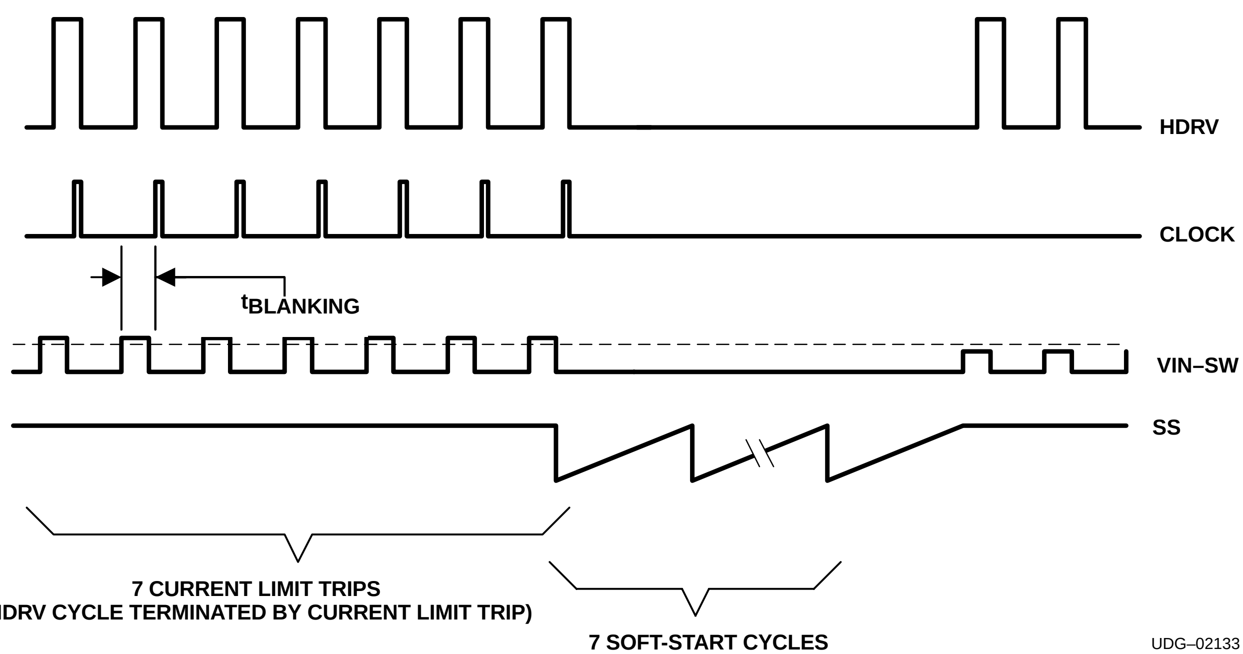


Figure 6. Typical Current Limit Protection Waveforms

APPLICATION INFORMATION

SYNCHRONIZING TO AN EXTERNAL SUPPLY

The TPS4005x can be synchronized to an external clock through the SYNC pin. The TPS4005x must be synchronized at a frequency 20% higher than its programmed free-run frequency. The clock frequency at the SYNC pin replaces the master clock generated by the oscillator circuit. Pulling the SYNC pin low programs the TPS4005x to freely run at the frequency programmed by R_T.

The higher synchronization must be factored in when programming the PWM ramp generator circuit. If the PWM ramp is interrupted by the SYNC pulse, a UVLO condition is declared and the PWM becomes disabled. Typically this is of concern under low-line conditions only. In any case, R_{KFF} needs to be adjusted for the higher switching frequency.

LOOP COMPENSATION

Voltage-mode buck-type converters are typically compensated using Type III networks. Since the TPS4005x uses voltage feedforward control, the gain of the PWM modulator with voltage feedforward circuit must be included. The modulator gain is described in Figure 7, with V_{IN} being the minimum input voltage required to cause the ramp excursion to cover the entire switching period.

$$A_{MOD} = \frac{V_{IN}}{V_S} \quad \text{or} \quad A_{MOD(dB)} = 20 \times \log\left(\frac{V_{IN}}{V_S}\right) \tag{17}$$

Duty dycle, D, varies from 0 to 1 as the control voltage, V_C, varies from the minimum ramp voltage to the maximum ramp voltage, V_S. Also, for a synchronous buck converter, $D = V_O / V_{IN}$. To get the control voltage to output voltage modulator gain in terms of the input voltage and ramp voltage,

$$D = \frac{V_O}{V_{IN}} = \frac{V_C}{V_S} \quad \text{or} \quad \frac{V_O}{V_C} = \frac{V_{IN}}{V_S}$$

Calculate the Poles and Zeros

For a buck converter using voltage mode control there is a double pole due to the output L-C_O. The double pole is located at the frequency calculated in equation (18).

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L \times C_O}} \quad \text{(Hertz)} \tag{18}$$

There is also a zero created by the output capacitance, C_O, and its associated ESR. The ESR zero is located at the frequency calculated in equation (19).

$$f_Z = \frac{1}{2\pi \times ESR \times C_O} \quad \text{(Hertz)} \tag{19}$$

The Bode plot for the open-loop control voltage to output voltage gain, V_C to V_O, for a buck converter with voltage feed-forward control operating in continuous mode is shown in Figure 8.

The maximum crossover frequency (0 dB loop gain) is calculated in equation (20).

$$f_C = \frac{f_{SW}}{4} \quad \text{(Hertz)} \tag{20}$$

Typically, f_C is selected to be close to the midpoint between the L-C_O double pole and the ESR zero. At this frequency, the control to output gain has a –2 slope (–40 dB/decade), while the Type III topology has a +1 slope (20 dB/decade), resulting in an overall closed loop –1 slope (–20 dB/decade).

APPLICATION INFORMATION

Figure 8 shows the modulator gain, L-C filter, output capacitor ESR zero, and the resulting response to be compensated.

A Type III topology, shown in Figure 9, has two zero-pole pairs in addition to a pole at the origin. The gain and phase boost of a Type III topology is shown in Figure 9. The two zeros are used to compensate the L-C_O double pole and provide phase boost. The double pole is used to compensate for the ESR zero and provide controlled gain roll-off. In many cases the second pole can be eliminated and the amplifier's gain roll-off used to roll-off the overall gain at higher frequencies.

PWM MODULATOR RELATIONSHIPS

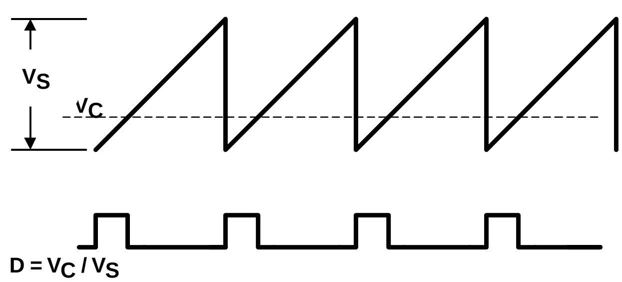


Figure 7

MODULATOR GAIN vs SWITCHING FREQUENCY

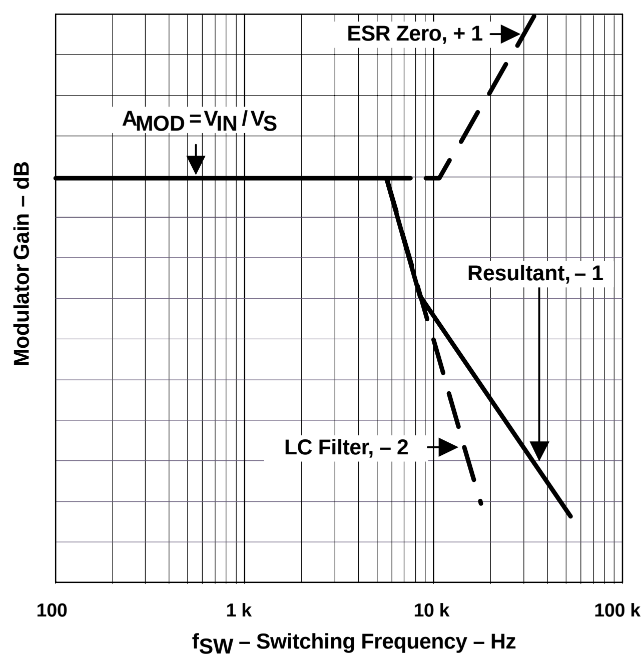


Figure 8

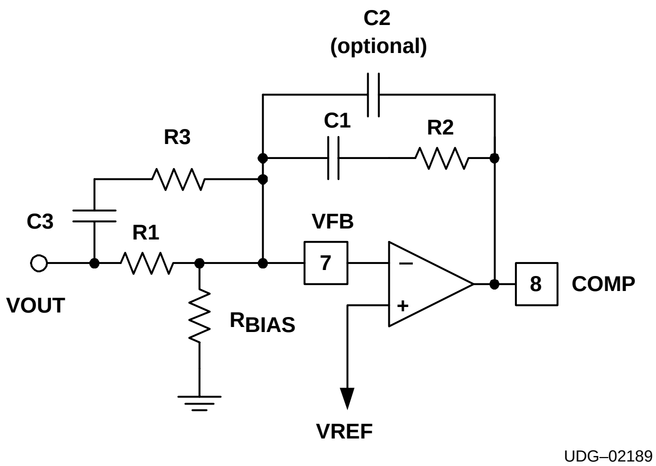


Figure 9. Type III Compensation Configuration

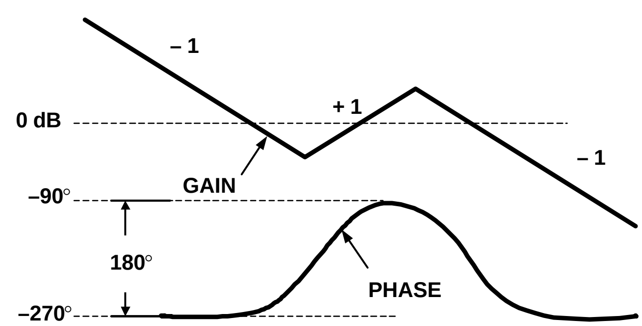


Figure 10. Type III Compensation Gain and Phase

APPLICATION INFORMATION

The poles and zeros for a type III network are described in equations (21).

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \quad \text{(Hertz)} \qquad f_{Z2} = \frac{1}{2\pi \times R1 \times C3} \quad \text{(Hertz)}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2} \quad \text{(Hertz)} \qquad f_{P2} = \frac{1}{2\pi \times R3 \times C3} \quad \text{(Hertz)} \tag{21}$$

The unity gain frequency is described in equation (22)

$$f_C = \frac{1}{2\pi \times R1 \times C2} \quad \text{(Hertz)} \tag{22}$$

The double zeros, f_{Z1} and f_{Z2} and the double poles, f_{P1} and f_{P2} are chosen from Venable's *The K Factor*[1], which states:

$$f_{Z1} = f_{Z2} = \frac{f_C}{\sqrt{K}} \quad \text{and} \quad f_{P1} = f_{P2} = f_C \times \sqrt{K} \tag{23}$$

To determine the factor K, the phase boost must be calculated knowing the desired phase margin, M, and the modulator phase shift, P, at the unity gain frequency, f_C. In addition, Boost = M–P–90. It is best to measure P, but typical values range from –140° to –170°. Then the value of K is calculated from:

$$K = \left(\mathrm{Tan}\left[\frac{\mathrm{Boost}}{4} + 45^{o} \right] \right)^2 \tag{24}$$

Calculate the value of R_{BIAS} to set the output voltage, V_{OUT}.

$$R_{BIAS} = \frac{0.7 \times R1}{V_{OUT} - 0.7} \tag{25}$$

Minimum Load Resistance

Care must be taken not to load down the output of the error amplifier with the feedback resistor, R2, that is too small. The error amplifier has a finite output source and sink current which must be considered when sizing R2. Too small a value does not allow the output to swing over its full range.

$$R2_{(MIN)} = \frac{V_{C\,(max)}}{I_{SOURCE\,(min)}} = \frac{3.45\ V}{2\ mA} = 1725\ \Omega \tag{26}$$

CALCULATING THE BOOST AN BP10 BYPASS CAPACITOR

The BOOST capacitance provides a local, low impedance source for the high-side driver. The BOOST capacitor should be a good quality, high-frequency capacitor. The size of the bypass capacitor depends on the total gate charge of the MOSFET and the amount of droop allowed on the bypass capacitor. The BOOST capacitance is described in equation (27).

$$C_{BOOST} = \frac{Q_g}{\Delta V} \quad \text{(Farads)} \tag{27}$$

The 10-V reference pin, BP10V needs to provide energy for both the synchronous MOSFET and the high-side MOSFET via the BOOST capacitor. Neglecting any efficiency penalty, the BP10V capacitance is described in equation (28).

$$C_{BP10} = \frac{\left(Q_{gHS} + Q_{gSR}\right)}{\Delta V} \quad \text{(Farads)} \tag{28}$$

APPLICATION INFORMATION

dv/dt INDUCED TURN–ON

MOSFETs are susceptible to dv/dt turn-on particularly in high-voltage (V_{DS}) applications. The turn-on is caused by the capacitor divider that is formed by C_{GD} and C_{GS}. High dv/dt conditions and drain-to-source voltage, on the MOSFET causes current flow through C_{GD} and causes the gate-to-source voltage to rise. If the gate-to-source voltage rises above the MOSFET threshold voltage, the MOSFET turns on, resulting in large shoot-through currents. Therefore, the SR MOSFET should be chosen so that the C_{GD} capacitance is smaller than the C_{GS} capacitance. A resistor with a value between 2 Ω and 5 Ω in the upper MOSFET gate return lead shapes the turn-on and dv/dt of the SW node and helps reduce the induced turn-on.

HIGH SIDE MOSFET POWER DISSIPATION

The power dissipated in the external high-side MOSFET is comprised of conduction and switching losses. The conduction losses are a function of the I_{RMS} current through the MOSFET and the $R_{DS(on)}$ of the MOSFET. The high-side MOSFET conduction losses are defined by equation (29).

$$P_{COND} = \left(I_{RMS}\right)^2 \times R_{DS(on)} \times \left(1 + TC_R \times \left[T_J - 25\right]\right) \quad \text{(Watts)} \tag{29}$$

where:

- TC_R is the temperature coefficient of the MOSFET $R_{DS(on)}$

The TC_R varies depending on MOSFET technology and manufacturer but is typically ranges between .0035 ppm/°C and .010 ppm/°C.

The I_{RMS} current for the high side MOSFET is described in equation (30).

$$I_{RMS} = I_O \times \sqrt{d} \quad \left(\text{Amperes}_{RMS}\right) \tag{30}$$

For the high-side MOSFET the switching losses are descibed in equation (31).

$$P_{SW(fsw)} = V_{IN} \times \left(\frac{I_{D1} \times ts1}{6} + \frac{I_{D2} \times ts2}{2}\right) \times f_{SW} \tag{31}$$

where:

- I_{D1} and I_{D2} are the current magnitudes at the instance of MOSFET switching (See Figure 11)

I_{D1} and I_{D2} are a function of the inductor value and load current. The inductance value is usually selected so that the converter remains in continuous mode of operation until approximately 10% to 30% of the typical load is acheived. The change in inductor current is described in equation (32).

$$\Delta I = 2 \times I_{O\ (dis)} \tag{32}$$

where:

- $I_{O\ (dis)}$ is the load current when the converter enters discontinuous mode of operation.

APPLICATION INFORMATION

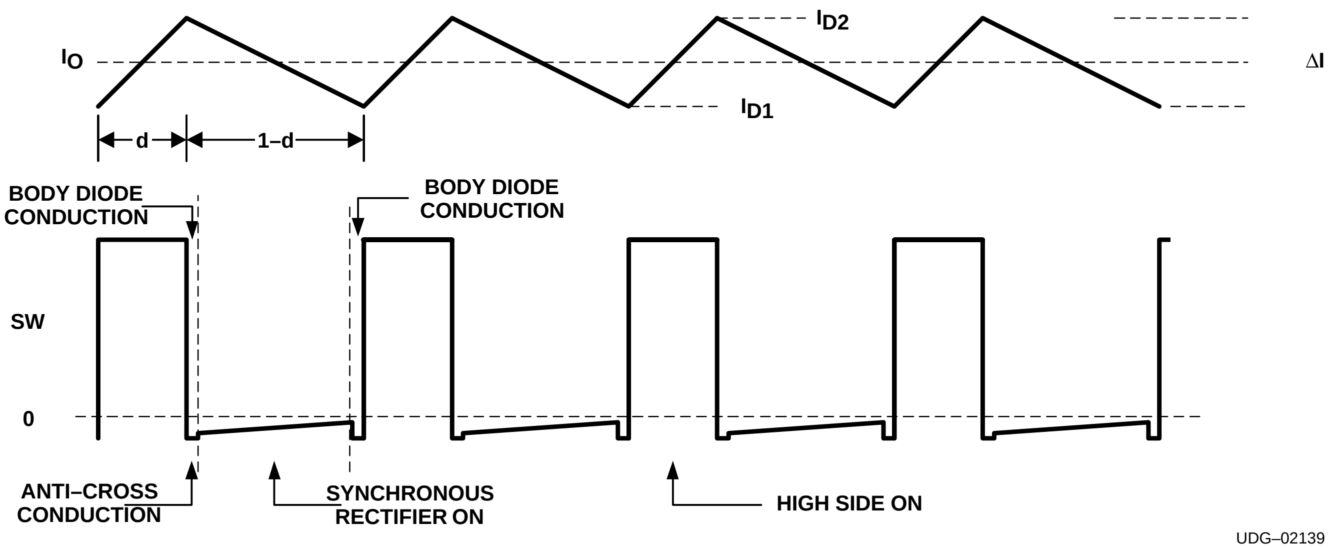


Figure 11. Inductor Current and SW Node Waveforms

I_{D1} and I_{D2} can be calculated from equations (33).

$$I_{D1} = I_O - \left(\frac{\Delta I}{2}\right) \quad \text{and} \quad I_{D2} = I_O + \left(\frac{\Delta I}{2}\right) \quad \text{(Amperes)} \tag{33}$$

where:

- ΔI is the inductor ripple current. (see Figure 11)

The converter enters discontinuous mode when $I_O = \Delta I / 2$. Refer to *Selecting the Inductor Value* section, equation (6), for more information.

The transition times, ts1 and ts2, are a function of the external MOSFETS selected. Refer to the design example for calculating ts1 and ts2.

The maximum allowable power dissipation in the MOSFET is determined by equation (34).

$$P_T = \frac{\left(T_J - T_A\right)}{\theta_{JA}} \quad \text{(Watts)} \tag{34}$$

where:

$$P_T = P_{COND} + P_{SW(fsw)} \quad \text{(Watts)} \tag{35}$$

and θ_{JA} is the package thermal impedance.

APPLICATION INFORMATION

SYNCHRONOUS RECTIFIER MOSFET POWER DISSIPATION

The power dissipated in the synchronous rectifier MOSFET is comprised of three components: $R_{DS(on)}$ conduction losses, body diode conduction losses, and reverse recovery losses. $R_{DS(on)}$ conduction losses can be found using equation (29) and the RMS current through the synchronous rectifier MOSFET is described in equation (36).

$$I_{RMS} = I_O \times \sqrt{1 - d} \quad \left(\text{Amperes}_{RMS}\right) \tag{36}$$

The body–diode conduction losses are due to forward conduction of the body diode during the anti–cross conduction delay time. The body diode conduction losses are described by equation (37).

$$P_{DC} = I_O \times V_F \times t_{DELAY} \times f_{SW} \quad (\text{Watts}) \tag{37}$$

where:

- V_F is the body diode forward voltage
- t_{DELAY} is the total delay time per switching period

The reverse recovery losses are due to the time it takes for the body diode to recovery from a forward bias to a reverse blocking state. The reverse recovery losses are described in equation (38).

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} \quad (\text{Watts}) \tag{38}$$

where:

- Q_{RR} is the reverse recovery charge of the body diode

The total synchronous rectifier MOSFET power dissipation is described in equation (39).

$$P_{SR} = P_{DC} + P_{RR} + P_{COND} \quad (\text{Watts}) \tag{39}$$

TPS4005X POWER DISSIPATION

The power dissipation in the TPS4005x is largely dependent on the MOSFET driver currents and the input voltage. The driver current is proportional to the total gate charge, Qg, of the external MOSFETs. Driver power (neglecting external gate resistance, refer to [2] can be calculated from equation (40).

$$P_D = Q_g \times V_{DR} \times f_{SW} \quad (\text{Watts}) \tag{40}$$

And the total power dissipation in the TPS40050, assuming the same MOSFET is selected for both the high-side and synchronous rectifier is described in equation (41).

$$P_T = \left(\frac{2 \times P_D}{V_{DR}} + I_Q\right) \times V_{IN} \quad (\text{Watts}) \tag{41}$$

or

$$P_T = \left(2 \times Q_g \times f_{SW} + I_Q\right) \times V_{IN} \quad (\text{Watts}) \tag{42}$$

where:

- I_Q is the quiescent operating current (neglecting drivers)

APPLICATION INFORMATION

The maximum power capability of the device's PowerPad package is dependent on the layout as well as air flow. The thermal impedance from junction to air, assuming 2 oz. copper trace and thermal pad with solder and no air flow.

$\theta_{JA} = 36.51°C/W$

The maximum allowable package power dissipation is related to ambient temperature by equation (34). Substituting equation (34) into equation (42) and solving for f_{SW} yields the maximum operating frequency for the TPS4005x. The result is described in equation (43).

$$f_{SW} = \frac{\left(\left[\frac{\left(T_J - T_A\right)}{\left(\theta_{JA} \times V_{DD}\right)}\right] - I_Q\right)}{\left(2 \times Q_g\right)} \quad (Hz) \tag{43}$$

LAYOUT CONSIDERATIONS

THE POWERPAD™ PACKAGE

The PowerPAD package provides low thermal impedance for heat removal from the device. The PowerPAD derives its name and low thermal impedance from the large bonding pad on the bottom of the device. For maximum thermal performance, the circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depends on the size of the PowerPAD package. For a 16-pin TSSOP (PWP) package the area is 5 mm x 3.4 mm [3].

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter of 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to *PowerPAD Thermally Enhanced Package*[3] and the mechanical illustration at the end of this document for more information on the PowerPAD package.

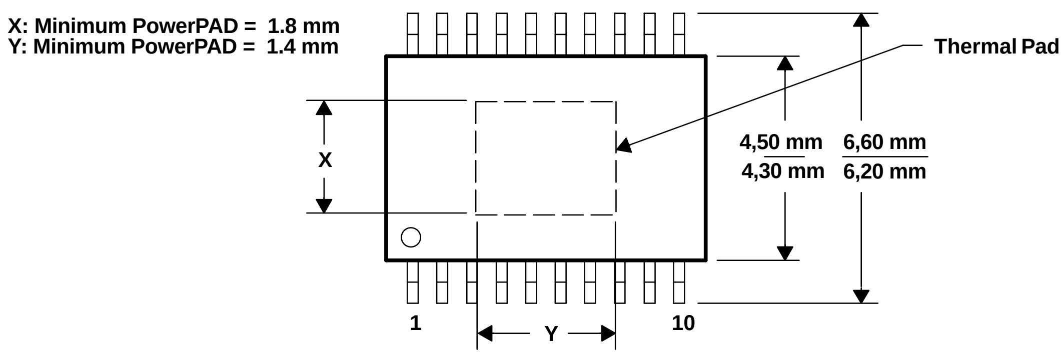


Figure 12. PowerPAD Dimensions

MOSFET PACKAGING

MOSFET package selection depends on MOSFET power dissipation and the projected operating conditions. In general, for a surface-mount applications, the DPAK style package provides the lowest thermal impedance (θ_{JA}) and, therefore, the highest power dissipation capability. However, the effectiveness of the DPAK depends on proper layout and thermal management. The θ_{JA} specified in the MOSFET data sheet refers to a given copper area and thickness. In most cases, a lowest thermal impedance of 40°C/W requires one square inch of 2-ounce copper on a G–10/FR–4 board. Lower thermal impedances can be achieved at the expense of board area. Please refer to the selected MOSFET's data sheet for more information regarding proper mounting.

GROUNDING AND CIRCUIT LAYOUT CONSIDERATIONS

The TPS4005x provides separate signal ground (SGND) and power ground (PGND) pins. It is important that circuit grounds are properly separated. Each ground should consist of a plane to minimize its impedance if possible. The high power *noisy* circuits such as the output, synchronous rectifier, MOSFET driver decoupling capacitor (BP10), and the input capacitor should be connected to PGND plane at the input capacitor.

Sensitive nodes such as the FB resistor divider, R_T, and ILIM should be connected to the SGND plane. The SGND plane should only make a single point connection to the PGND plane.

Component placement should ensure that bypass capacitors (BP10 and BP5) are located as close as possible to their respective power and ground pins. Also, sensitive circuits such as FB, RT and ILIM should not be located near high dv/dt nodes such as HDRV, LDRV, BOOST, and the switch node (SW).

DESIGN EXAMPLE

- Input Voltage: 10 Vdc to 24 Vdc
- Output voltage: 3.3 V ±2%
- Output current: 8 A (maximum, steady state), 10 A (surge, 10ms duration, 10% duty cycle maximum)
- Output ripple: 33 $mV_{P\text{-}P}$ at 8 A
- Output load response: 0.3 V => 10% to 90% step load change
- Operating temperature: –40°C to 85°C
- f_{SW}=300 kHz

1. Calculate maximum and minimum duty cycles

$$d_{MIN} = \frac{V_{O(min)}}{V_{IN(max)}} = 0.135 \quad d_{MAX} = \frac{V_{O(max)}}{V_{IN(min)}} = 0.337 \tag{44}$$

2. Select ΔI

In this case ΔI is chosen so that the converter enters discontinuous mode at 20% of nominal load.

$$\Delta I = I_O \times 2 \times 0.2 = 3.2\text{ A} \tag{45}$$

3. Calculate the power losses in the high-side MOSFET (Si7860DY)

from (30)

$$I_{RMS} = I_O \times \sqrt{d} = 8 \times \sqrt{0.337} = 4.64\text{ A} \tag{46}$$

substituting (30) into (29) yields

$$P_{COND} = {I_{RMS}}^2 \times R_{DS(on)} \times \left(1 + T_{CR} \times \left[T_J - 25°C\right]\right) \tag{47}$$

$$= 4.64^2 \times 0.008 \times (1 + 0.007 \times (150 - 25)) = 0.323\text{ W}$$

from (33)

$$I_{D1} = I_O - \frac{\Delta I}{2} = 8 - 1.6 = 6.4\text{ A} \quad I_{D2} = I_O + \frac{\Delta I}{2} = 8 + 1.6 = 9.6\text{ A} \tag{48}$$

t_{S1} (rise time) and t_{S2} (fall time) is approximated from the Gate Charge characteristics graph on the MOSFET data sheet.

Let Q2–Q1 equal the charge required to increase the gate voltage to its plateau voltage (V_{PLT}). The equivalent input capacitance during this period is:

$$C_{IN} = \frac{dQ}{dV} = \frac{4\text{ nC}}{3.5\text{ V}} = 1143\text{ pF} \tag{49}$$

The time required to charge the equivalent capacitance is:

$$3.5 = 10 - (10 - 2) \times e^{\left(\frac{-t}{R \times C}\right)};\ t1 = -R_X\,C_{IN}\,\ln\left(\frac{6.5}{8}\right) = 10 \times 1143\text{ pF} \times \ln\left(\frac{6.5}{8}\right) = 2.4\text{ ns} \tag{50}$$

where R is the effective gate drive resistance of 10 Ω.

The time it takes the drain-to-source voltage V_{DS} to fall can be found from Gate Charge graph on the data sheet. During this time in the plateau region the change in charge is:

$$\Delta Q = Q3 - Q2 = 9.5 - 5 = 4.5\text{ nC} \tag{51}$$

DESIGN EXAMPLE

During this period of time V_{GS} is held constant. Therefore the MOSFET gate drive looks like a constant current source with a current of:

$$I_{DRV} = \frac{V_{DRV} - V_{GS}}{R_{DRV}} = \frac{10 - 3.5}{10} = 650\ \text{mA} \tag{52}$$

The time it takes for V_{DS} to fall can now be calculated:

$$t_2 = \frac{\Delta Q}{I_{DRV}} = \frac{4.5\ \text{nC}}{0.65\ \text{A}} = 6.9\ \text{ns} \tag{53}$$

The total rise time is :

$$t_{S1} = t_r = t_I + t_2 = 2.4\ \text{n} + 6.9\ \text{n} = 9.3\ \text{ns} \tag{54}$$

The similarly the fall time can be found from:

$$t_3 = (Q3 - Q2) \times \frac{R_{DRV}}{V_{PLT}} = 4.5\ \text{nC} \times \frac{7.5\ \Omega}{3.5\ \text{V}} = 9.6\ \text{ns} \tag{55}$$

$$t_4 = -R_{DRV} \times C_{IN} \times \ln\left(\frac{3.5}{10}\right) = 12\ \text{ns} \tag{56}$$

The total fall time is:

$$t_{S2} = t_f = t_3 + t_4 = 9.6\ \text{ns} + 12\ \text{ns} = 21.6\ \text{ns} \tag{57}$$

Substituting t_{S1}, t_{S2}, I_{D1}, and I_{D2} into (31) yields:

$$P_{SW}\left(f_{SW}\right) = 24 \times \left(\frac{9.3\ \text{ns} \times 6.4}{6} + \frac{21.6\ \text{ns} \times 9.6}{2}\right) \times 300\ \text{kHz} = 818\ \text{mW} \tag{58}$$

The MOSFET junction temperature can be found by rearranging equation (34) and substituting equation (35)

$$T_J = \left(P_{COND} + P_{SW}\right) \times \theta_{JA} + T_A$$

4. Calculate synchronous rectifier losses

The synchronous rectifier MOSFET has two (2) loss components, conduction, and diode reverse recovery losses. The conduction losses are due to I_{RMS} losses as well as body diode conduction losses during the dead time associated with the anti-cross conduction delay.

The I_{RMS} current through the synchronous rectifier from (36)

$$I_{RMS} = I_O \times \sqrt{1 - d} = 8 \times \sqrt{1 - 0.135} = 7.44\ A_{RMS} \tag{59}$$

The synchronous MOSFET conduction loss from (29) is:

$$P_{COND} = {I_{RMS}}^2 \times R_{DS(on)} = 7.44^2 \times 0.008 \times (1 + 0.007(150 - 25)) = 0.83\ \text{W} \tag{60}$$

The body diode conduction loss from (37) is:

$$P_{DC} = I_O \times V_{FD} \times t_{dead} \times f_{SW} = 8.0\ \text{A} \times 0.8\ \text{V} \times 100\ \text{ns} \times 300\ \text{kHz} = 0.192\ \text{W} \tag{61}$$

The body diode reverse recovery loss from (38) is:

$$P_{RR} = 0.5 \times Q_{RR} \times V_{IN} \times f_{SW} = 0.5 \times 40\ \text{nC} \times 24\ \text{V} \times 300\ \text{kHz} = 0.144\ \text{W} \tag{62}$$

The total power dissipated in the synchronous rectifier MOSFET from (39) is:

$$P_{SR} = P_{RR} + P_{COND} + P_{DC} = 0.144 + 0.83 + 0.192 = 1.17\ \text{W} \tag{63}$$

DESIGN EXAMPLE

The junction temperature of the synchronous rectifier at 85°C is:

$$T_J = P_{SR} \times \theta_{JA} + T_A = (1.17) \times 40 + 85 = 132^oC \quad (64)$$

In typical applications, paralleling the synchronous rectifier MOSFET with a Schottky rectifier increases the overall converter efficiency by approximately 2% due to the lower power dissipation during the body diode conduction and reverse recovery periods.

5. Calculate the inductor value

The inductor value is calculated from (6) using (45).

$$L = \frac{(24 - 3.3) \times 3.3}{24 \times 3.2 \times 300\ \text{kHz}} = 2.96\ \mu\text{H} \quad (65)$$

A 2.9-μH Panasonic ETQP6F2R9LFA or COEV DXM1306–2R9–T is chosen.

6. Setting the switching frequency

The clock frequency is set with a resistor (R_T) from the RT pin to ground. The value of R_T can be found from equation (1), with f_{SW} in kHz.

$$R_T = \left(\frac{1}{f_{SW} \times 17.82 \times 10^{-6}} - 23 \right) \text{k}\Omega = 164\ \text{k}\Omega \quad \therefore \text{ use } 165\ \text{k}\Omega \quad (66)$$

7. Programming the ramp generator circuit

The PWM ramp is programmed through a resistor (R_{KFF}) from the KFF pin to V_{IN}. The ramp generator also controls the input UVLO voltage. For an undervoltage level of 10 V, R_{KFF} can be calculated from (2)

$$R_{KFF} = \left(V_{IN(min)} - 3.5\right)\left(58.14 \times R_T + 1340\right) \Omega = 71\ \text{k}\Omega \quad \therefore \text{ use } 71.5\ \text{k}\Omega \quad (67)$$

8. Calculating the output capacitance (C_O)

In this example the output capacitance is determined by the load response requirement of ΔV = 0.3 V for a 1 A to 8 A step load. C_O can be calculated using (12)

$$C_O = \frac{2.9\ \mu \times \left(8^2 - 1^2\right)}{\left(3.3^2 - 3.0^2\right)} = 97\ \mu\text{F} \quad (68)$$

Using (7) we can calculate the ESR required to meet the output ripple requirements.

$$33\ \text{mV} = 3.2 \left(\text{ESR} + \frac{1}{8 \times 97\ \mu\text{F} \times 300\ \text{kHz}} \right) \quad (69)$$

$$\text{ESR} = 10.3 - 3.33 = 6.97\ \text{m}\Omega \quad (70)$$

For this design example two (2) Panasonic SP EEFUEOJ1B1R capacitors, 180 μF, 12 mΩ were used.

9. Calculate the soft-start capacitor (C_{SS})

This design, requires a soft–start time (t_{START}) of 1 ms. CSS can be calculated on (14)

$$C_{SS} = \frac{2.3\ \mu\text{A}}{0.7\ \text{V}} \times 1\ \text{ms} = 3.29\ \text{nF} = 3300\ \text{pF} \quad (71)$$

DESIGN EXAMPLE

10. Calculate the current limit resistor (R_{ILIM})

The current limit set point depends on, t_{START}, V_O,C_O and I_{LOAD} at start-up as shown in (15). For this design,

$$I_{LIM} > \frac{360\ \mu F \times 3.3}{1\ ms} + 8.0 = 9.2\ A \tag{72}$$

For this design, set I_{LIM} for 11.0 A minimum. From equation (16),

$$R_{ILIM} = \frac{11 \times 0.008}{1.12 \times 10\ \mu A} + \frac{(-0.048)}{10\ \mu A} = 7.86\ k\Omega - 4.8\ k\Omega = 3.06\ k\Omega \cong 3.09\ k\Omega \tag{73}$$

11. Calculate loop compensation values

Calculate the voltage feed forward constant (A_{MOD}) from (17)

$$A_{MOD} = \frac{10}{2} = 5.0 \tag{74}$$

$$A_{MOD(dB)} = 20 \times \log(5) = 14\ dB \tag{75}$$

Calculate the output poles and zeros from (18) and (19)

$$f_{LC} = \frac{1}{2\pi\sqrt{2.9\ \mu H \times 360\ \mu F}} = 4.93\ kHz \tag{76}$$

and

$$f_Z = \frac{1}{2\pi \times 0.012 \times 180\ \mu F} = 73.7\ kHz \tag{77}$$

Select the close-loop 0 dB crossover frequency, f_C. For this example f_C = 20 kHz.

Select the double zero location for the Type III compensation network. The location for the pole–zero placement according to [1] is determined by the phase boost required at crossover. For this example a 60° phase margin is desired. The required phase boost for this example is:

$$\text{Boost} = M - P - 90^o = 60^o - (-145^o) - 90^o = 115^o \tag{78}$$

where

- M is the desired phase margin
- P is the modulator phase shift (–145° for this example)

$$K = \left(\text{Tan}\left[\frac{115^o}{4} + 45^o\right]\right)^2 \approx 11.77 \text{ and } \sqrt{K} = 3.43 \tag{79}$$

so,

$$f_{P1} = f_{P2} = \sqrt{K} \times 20\ kHz = 69\ kHz \text{ and } f_{Z1} = f_{Z2} = \frac{1}{\sqrt{K}} \times 20\ kHz = 5.8\ kHz$$

Following the K-Factor calculations described in reference [1], the double zero is placed at 5.8 kHz, and the double pole is placed at 69 kHz. Equations (21) and (22) can be solved for the component values in Figure 9. Select R1 = 100 kΩ.

DESIGN EXAMPLE

From equation (21):

$$C3 = \frac{1}{2\pi \times 100\ k\Omega \times 5.8\ kHz} = 274\ pF \approx 270\ pF,\ \text{from } f_{Z2} \tag{80}$$

$$R3 = \frac{1}{2\pi \times 270\ pF \times 69\ kHz} = 8.54\ k\Omega \approx 8.45\ k\Omega,\ \text{from } f_{P2} \tag{81}$$

$$C2 = \frac{1}{2\pi \times 100\ k\Omega \times 20\ kHz} = 79.6\ pF \cong 82\ pF,\ \text{from } f_{C} \tag{82}$$

$$R2 = \frac{1}{2\pi \times 82\ pF \times 69\ kHz} = 28.1\ k\Omega \cong 28\ k\Omega,\ \text{from } f_{P1} \tag{83}$$

$$C1 = \frac{1}{2\pi \times 28\ k\Omega \times 5.8\ kHz} = 980\ pF \approx 1000\ pF,\ \text{from } f_{Z1} \tag{84}$$

$$R_{BIAS} = \frac{0.7 \times 100k\Omega}{3.3 - 0.7} = 26.9\ k\Omega \approx 26.7\ k\Omega \tag{85}$$

GATE DRIVE CONFIGURATION

Due to the possibility of dv/dt induced turn–on from the fast MOSFET switching times, high V_{DS} voltage and low gate threshold voltage of the Si7860, the design includes a 3.3-Ω resistor in the gate return of the upper MOSFET. This resistor can be used to shape the low-to-high transition of the switch mode and reduce the tendancy of dv/dt-induced turn on.

CALCULATING THE BOOST AND BP10V BYPASS CAPACITANCE

The size of the bypass capacitor depends on the total gate charge of the MOSFET being used and the amount of droop allowed on the bypass cap. The BOOST capacitance, allowing for a 0.5 voltage droop on the BOOST pin from (27) is

$$C_{BOOST} = \frac{Q_g}{\Delta V} = \frac{13\ nC}{0.5\ V} = 26\ nF \tag{86}$$

and the BP10V capacitance from (28) is

$$C_{BP(10\ V)} = \frac{Q_{gHS} + Q_{gSR}}{\Delta V} = \frac{2 \times Q_g}{\Delta V} = \frac{26\ nC}{0.5\ V} = 52\ nF \tag{87}$$

For this application, a 0.1-µF capacitor is used for the BOOST bypass capacitor and a 1.0-µF capacitor is used for the BP10V.

Figure 13 shows component selection for the 24-V to 3.3-V at 8 A dc-to-dc converter specified in the design example.

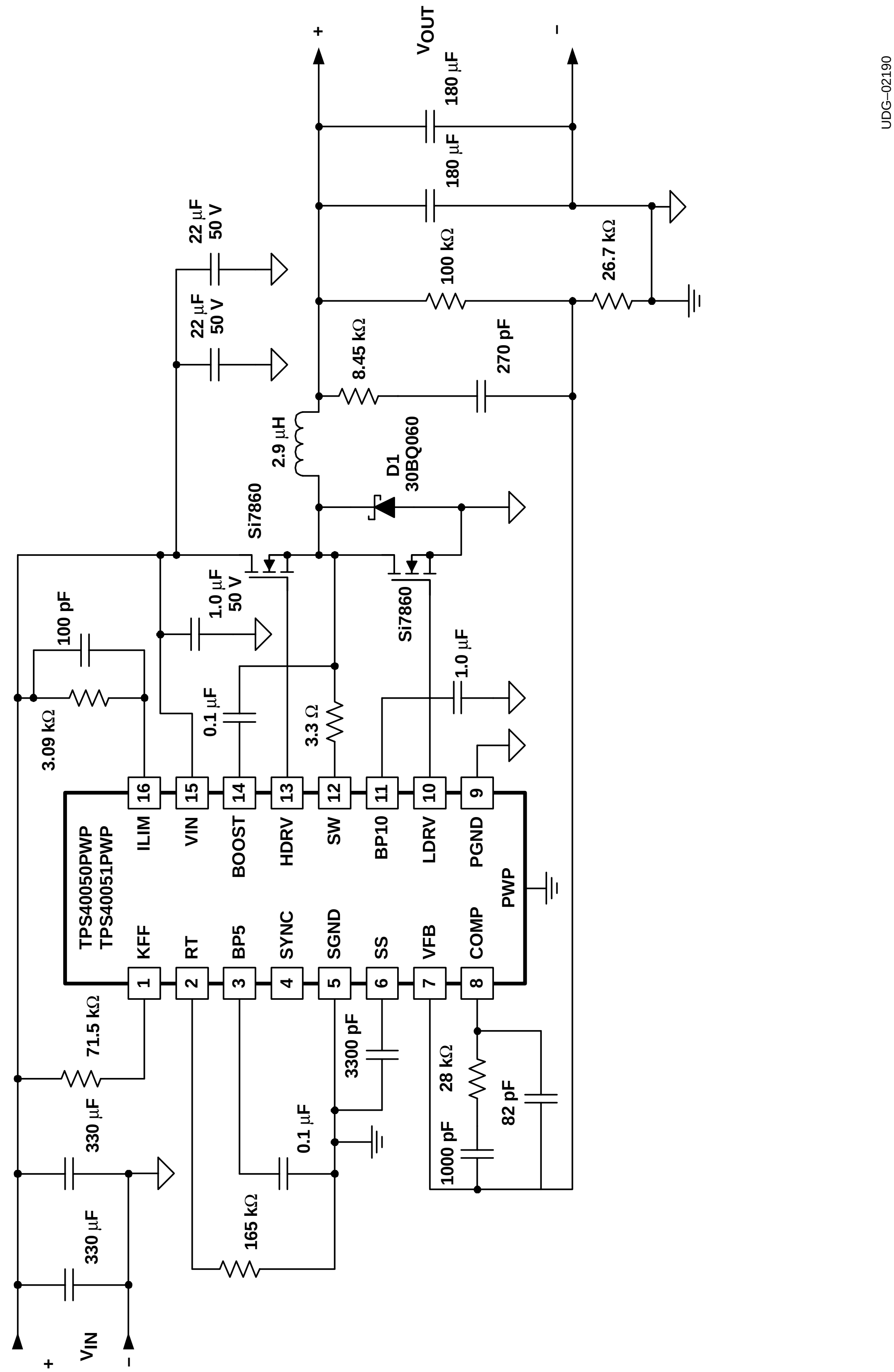


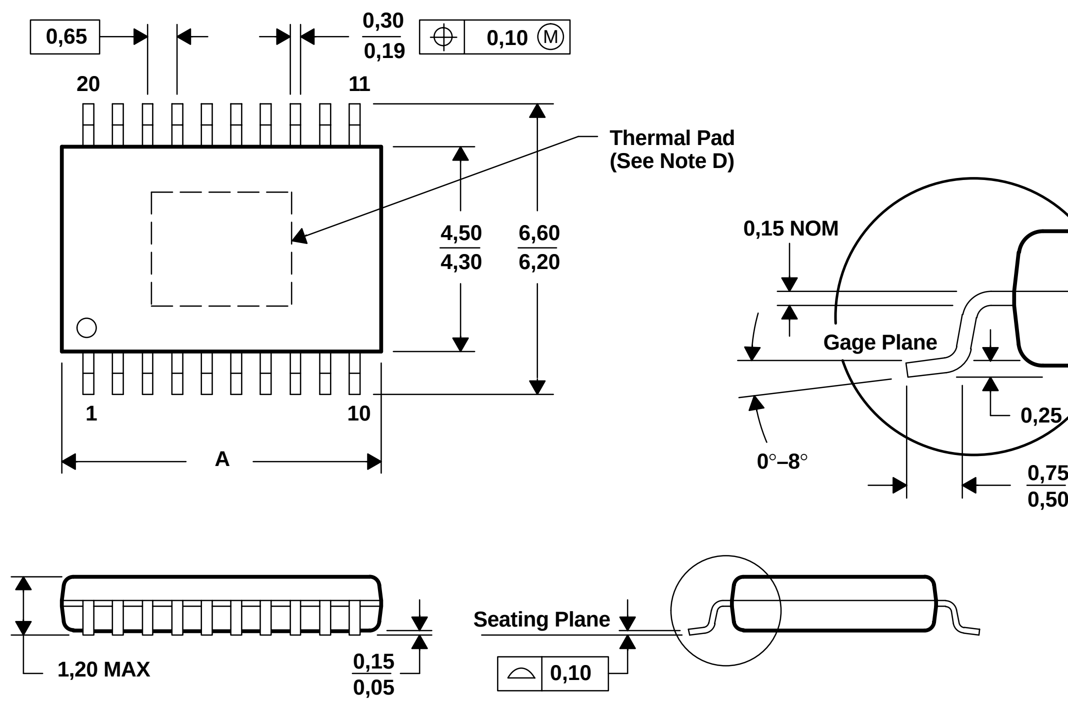
Figure 13. 24-V to 3.3-V at 8-A DC-to-DC Converter Design Example

REFERENCES

1. Venable, H. Dean, *The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis* Proceedings of Powercon 10, pp A5–1 through A5–12
2. Balogh, Laszlo, *Design and Application Guide for High Speed MOSFET Gate Drive Circuits*, Texas Instruments/Unitrode Corporation, Power Supply Design Seminar, SEM–1400 Topic 2.
3. *PowerPAD Thermally Enhanced Package* Texas Instruments, Semiconductor Group, Technical Brief: TI Literature No. SLMA002

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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