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SEMICONDUCTOR™

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100393 Low Power 9-Bit ECL-to-TTL Translator with Latches

General Description

The 100393 is a 9-bit translator for converting F100K logic levels to TTL logic levels. A LOW on the latch enable (LE) latches the data at the input state. A HIGH on the LE makes the latches transparent. A HIGH on either the ECL or TTL output enable (\overline{OE} ECL or \overline{OE} TTL), holds the outputs in a high impedance state.

The 100393 is designed with TTL, 64 mA outputs for Bus Driving capability. All ECL inputs have 50 k Ω pull-down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

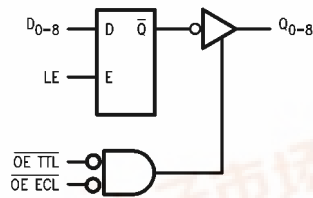
- 64 mA I_{OL} drive capability
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Latched outputs
- TTL outputs

Ordering Code:

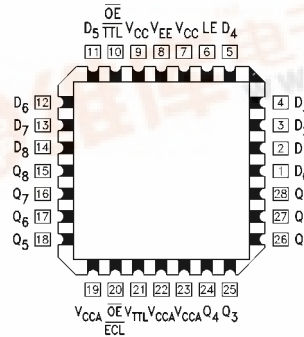
Order Number	Package Number	Package Description
100393QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
D_0 - D_8	Data Inputs (ECL)
Q_0 - Q_8	Data Outputs (TTL)
LE	Latch Enable Input (ECL)
\overline{OE} TTL	Output Enable (TTL)
\overline{OE} ECL	Output Enable (ECL)

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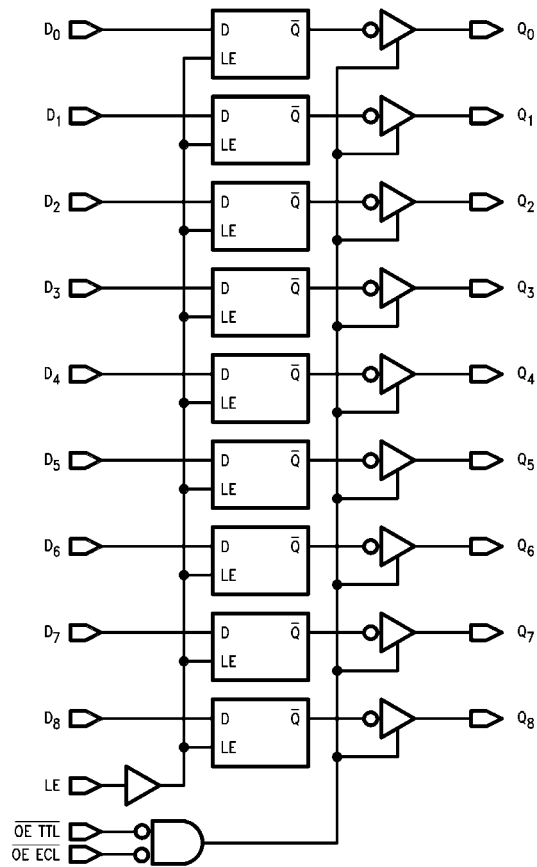


Truth Table

Inputs				Outputs
\overline{OE}_{TTL}	\overline{OE}_{ECL}	LE	D_N	Q_N
L	L	H	L	L
L	L	H	H	H
L	L	L	X	Latched
H	X	X	X	Z
X	H	X	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature (T_{STG})	-65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	-7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	-0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
TTL Input Voltage	-0.5V to +7.0V
Output Current (DC Output HIGH)	+130 mA
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	0°C to +85°C
Supply Voltage	
V_{EE}	-5.7V to -4.2V
V_{TTL}	+4.5V to +5.5V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

DC Electrical Characteristics (Note 3)

$V_{EE} = -4.2V$ to $-5.7V$; $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$, $T_C = 0°C$ to $+85°C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.5			V	$I_{OH} = -1$ mA $I_{OH} = -15$ mA $V_{IN} = V_{IL}$ (Min) or V_{IH} (Max)
V_{OL}	Output LOW Voltage			0.55 0.50	V	$I_{OL} = 64$ mA $I_{OL} = 24$ mA $V_{IN} = V_{IL}$ (Min) or V_{IH} (Max)
V_{IH}	Input HIGH Voltage	ECL Inputs	-1165	-870	mV	Guaranteed HIGH Signal for All Inputs
		\overline{OE} TTL	2.0		V	
V_{IL}	Input LOW Voltage	ECL Inputs	-1830	-1475	mV	Guaranteed LOW Signal for All Inputs
		\overline{OE} TTL		0.8	V	
I_{BVI}	Input Breakdown Current			10	μA	$V_{BI} = 7.0V$
I_{IH}	ECL Input HIGH Current	ECL Inputs		240	μA	$V_{IN} = V_{IH}$ (Max)
		\overline{OE} ECL		350		
I_{IL}	TTL Input HIGH Current	\overline{OE} TTL		5.0	μA	$V_{IN} = 2.7V$
		ECL Inputs	0.5		μA	$V_{IN} = V_{IL}$ (Min)
I_{IL}	TTL Input LOW Current	\overline{OE} TTL		-50	μA	$V_{IN} = 0.5V$
		ECL Inputs			μA	
I_{CEX}	Output HIGH Leakage Current			250	μA	
I_{OS}	Output Short-Circuit Current	-100		-225	mA	$V_{OUT} = 0.0V$, $V_{TTL} = +5.5V$
I_{OZH}	3-STATE Current Output HIGH			+50	μA	$V_{OUT} = +2.7V$
I_{OZL}	3-STATE Current Output LOW			-50	μA	$V_{OUT} = 0.5V$
V_{FCD}	Input Clamp Diode Voltage			-1.2	V	$I_{IN} = -18$ mA
I_{EE}	V_{EE} Power Supply Current	-39		-18	mA	Inputs OPEN
I_{CCH}	V_{TTL} Power Supply Current HIGH			29	mA	
I_{CCL}	V_{TTL} Power Supply Current LOW			65	mA	
I_{CCZ}	V_{TTL} Power Supply Current 3-STATE			49	mA	

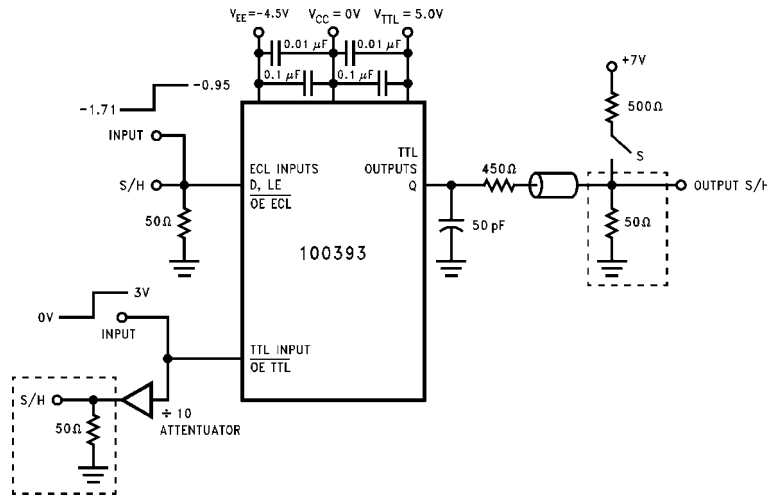
Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.3	4.8	2.3	4.8	2.3	5.3	ns	Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay LE to Output	2.3	5.6	2.3	5.6	2.3	6.4	ns	Figures 1, 2
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} TTL \downarrow to Q_N	2.0	5.5	2.0	5.5	2.0	5.5	ns	Figure 3
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OE} TTL \uparrow to Q_N	2.0	6.0	2.0	6.0	2.0	6.0	ns	Figure 3
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} ECL \uparrow to Q_N	2.4	5.6	2.4	5.6	2.4	5.6	ns	Figure 4
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OE} ECL \downarrow to Q_N	2.4	6.0	2.4	6.0	2.4	6.0	ns	Figure 4
t_S	Setup Time, D_N to LE	0.7		0.7		0.7		ns	Figures 1, 2
t_H	Hold Time, D_N to LE	1.3		1.3		1.3		ns	Figures 1, 2
$t_{PW(L)}$	Pulse Width LOW, LE	2.0		2.0		2.0		ns	Figures 1, 2

Test Circuit



Switch Positions for Parameter Testing

Parameter	S-Position
t_{PLH} , t_{PHL}	Open
t_{PHZ} , t_{PZH}	Open
t_{PLZ} , t_{PZL}	Open

FIGURE 1. AC Test Setup

Switching Waveforms

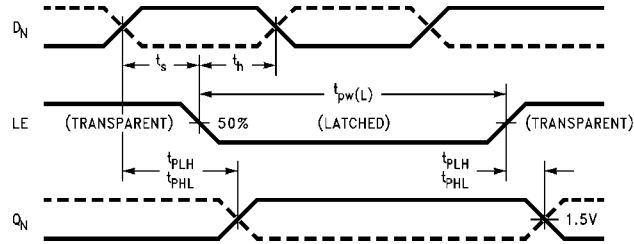


FIGURE 2. Propagation Delays, Setup and Hold Times, and Pulse Width

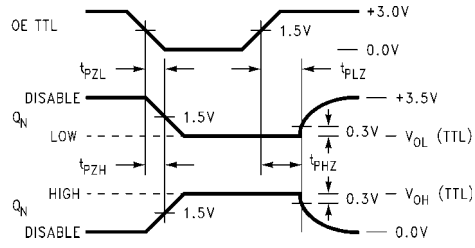


FIGURE 3. Enable and Disable Waveforms, \overline{OE} TTL

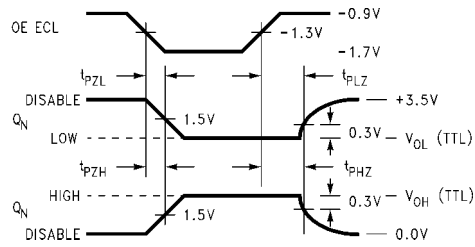
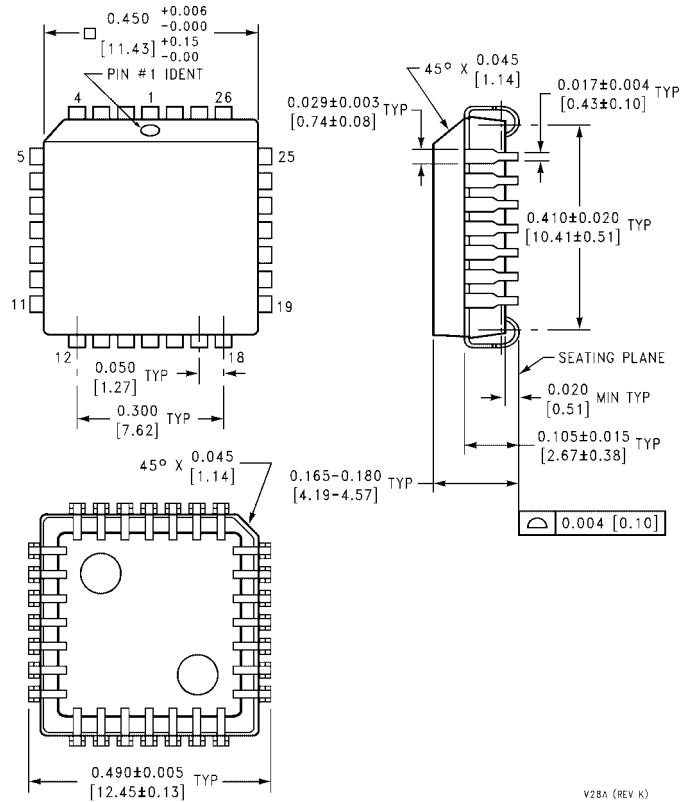


FIGURE 4. Enable and Disable Waveforms, \overline{OE} ECL

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Package Number V28A

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