

REGISTRATION PENDING

Currently Available as FRM230 (D, R, H)

December 2001

**Radiation Hardened
 N-Channel Power MOSFETs**

Features

- 8A, 200V, RDS(on) = 0.50Ω
- Second Generation Rad Hard MOSFET Results From New Design Concepts
- Gamma
 - Meets Pre-Rad Specifications to 100KRAD(Si)
 - Defined End Point Specs at 300KRAD(Si) and 1000KRAD(Si)
 - Performance Permits Limited Use to 3000KRAD(Si)
- Gamma Dot
 - Survives 3E9RAD(Si)/sec at 80% BVDSS Typically
 - Survives 2E12 Typically If Current Limited to IDM
- Photo Current
 - 3.0nA Per-RAD(Si)/sec Typically
- Neutron
 - Pre-RAD Specifications for 1E13 Neutrons/cm²
 - Usable to 1E14 Neutrons/cm²
- Single Event
 - Typically Survives 1E5ions/cm² Having an LET ≤ 35MeV/mg/cm² and a Range ≥ 30μm at 80% BVDSS

Description

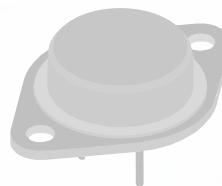
The Harris Semiconductor Sector has designed a series of SECOND GENERATION hardened power MOSFETs of both N and P channel enhancement types with ratings from 100V to 500V, 1A to 60A, and on resistance as low as 25mΩ. Total dose hardness is offered at 100K RAD(Si) and 1000KRAD(Si) with neutron hardness ranging from 1E13n/cm² for 500V product to 1E14n/cm² for 100V product. Dose rate hardness (GAMMA DOT) exists for rates to 1E9 without current limiting and 2E12 with current limiting. Heavy ion survival from signal event drain burn-out exists for linear energy transfer (LET) of 35 at 80% of rated voltage.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specially designed and processed to exhibit minimal characteristic changes to total dose (GAMMA) and neutron (n⁰) exposures. Design and processing efforts are also directed to enhance survival to heavy ion (SEE) and/or dose rate (GAMMA DOT) exposure.

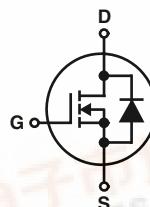
This part may be supplied as a die or in various packages other than shown above. Reliability screening is available as either non TX (commercial), TX equivalent of MIL-S-19500, TXV equivalent of MIL-S-19500, or space equivalent of MIL-S-19500. Contact the Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

Package

TO-204AA



Symbol



Absolute Maximum Ratings (TC = +25°C) Unless Otherwise Specified

	2N7274D, R, H	UNITS
Drain-Source Voltage.....	.VDS	V
Drain-Gate Voltage (RGS = 20kΩ).....	.VDGR	V
Continuous Drain Current TC = +25°CID	A
TC = +100°CID	A
Pulsed Drain Current.....	.IDM	A
Gate-Source VoltageVGS	V
Maximum Power Dissipation TC = +25°CPT	W
TC = +100°CPT	W
Derated Above +25°C	0.60	W/°C
Inductive Current, Clamped, L = 100μH, (See Test Figure).....	.ILM	A
Continuous Source Current (Body Diode).....	.IS	A
Pulsed Source Current (Body Diode)ISM	A
Operating And Storage Temperature	TJC, TSTG	°C
Lead Temperature (During Soldering) Distance > 0.063 in. (1.6mm) From Case, 10s Max.....	.TL	°C

Specifications 2N7274D, 2N7274R, 2N7274H - Registration Pending

Pre-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Drain-Source Breakdown Volts	BVDSS	VGS = 0, ID = 1mA	200	-	V
Gate-Threshold Volts	VGS(th)	VDS = VGS, ID = 1mA	2.0	4.0	V
Gate-Body Leakage Forward	IGSSF	VGS = +20V	-	100	nA
Gate-Body Leakage Reverse	IGSSR	VGS = -20V	-	100	nA
Zero-Gate Voltage Drain Current	IDSS1 IDSS2 IDSS3	VDS = 200V, VGS = 0 VDS = 160V, VGS = 0 VDS = 160V, VGS = 0, TC = +125°C	- - -	1 0.025 0.25	mA
Rated Avalanche Current	IAR	Time = 20μs	-	24	A
Drain-Source On-State Volts	VDS(on)	VGS = 10V, ID = 8A	-	4.20	V
Drain-Source On Resistance	RDS(on)	VGS = 10V, ID = 5A	-	.50	Ω
Turn-On Delay Time	td(on)	VDD = 100V, ID = 8A	-	30	ns
Rise Time	tr	Pulse Width = 3μs	-	130	
Turn-Off Delay Time	td(off)	Period = 300μs, Rg = 25Ω	-	150	
Fall Time	tf	0 ≤ VGS ≤ 10 (See Test Circuit)	-	80	
Gate-Charge Threshold	QG(th)	VDD = 100V, ID = 8A IGS1 = IGS2 0 ≤ VGS ≤ 20	1	4	nc
Gate-Charge On State	QG(on)		15	60	
Gate-Charge Total	QGM		30	120	
Plateau Voltage	VGP		3	14	V
Gate-Charge Source	QGS		3	14	nc
Gate-Charge Drain	QGD		7	29	
Diode Forward Voltage	VSD	ID = 8A, VGD = 0	0.6	1.8	V
Reverse Recovery Time	TT	I = 8A; di/dt = 100A/μs	-	600	ns
Junction-To-Case	Rθjc		-	1.67	°C/W
Junction-To-Ambient	Rθja	Free Air Operation	-	60	

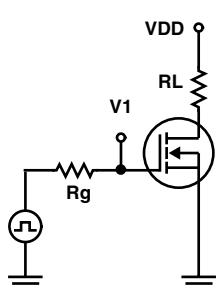


FIGURE 1. SWITCHING TIME TESTING

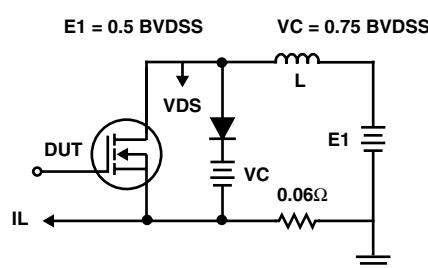


FIGURE 2. CLAMPED INDUCTIVE SWITCHING, ILM

2N7274D, 2N7274R, 2N7274H - Registration Pending

Post-Radiation Electrical Specifications TC = +25°C, Unless Otherwise Specified

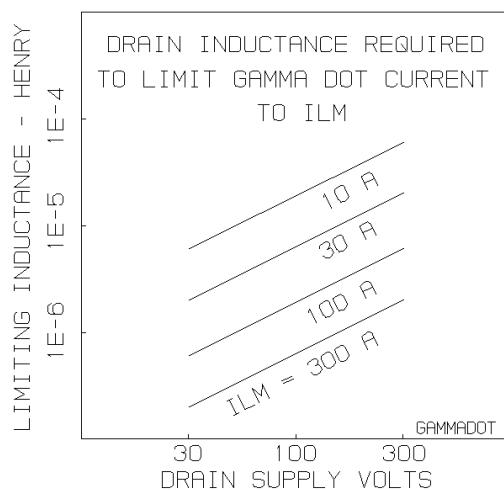
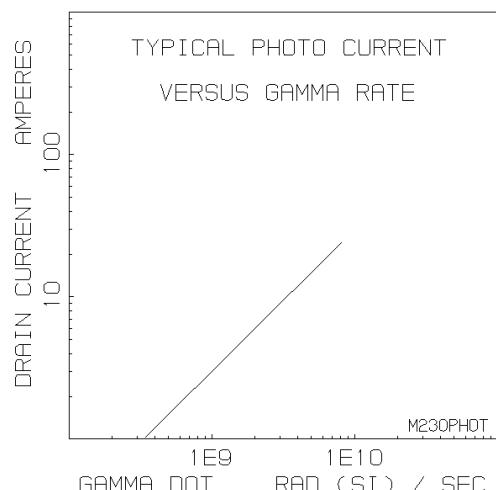
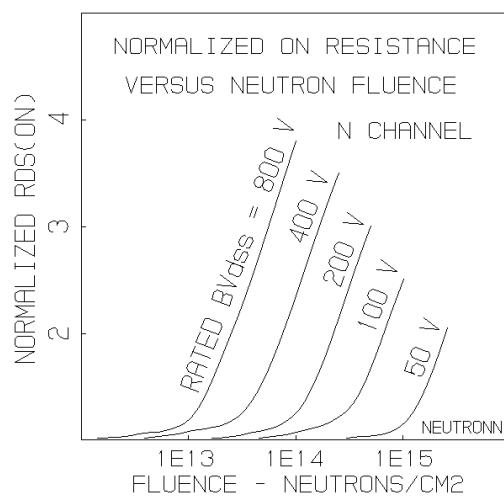
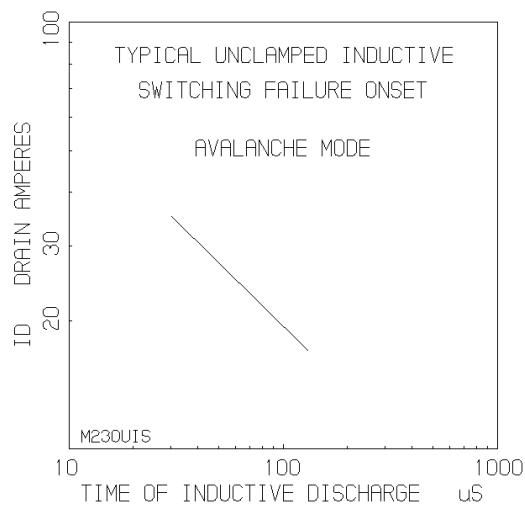
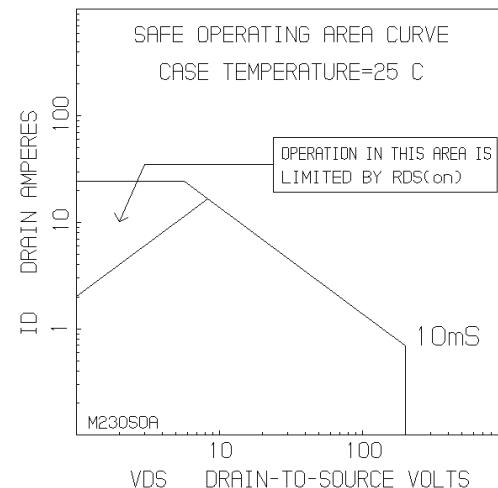
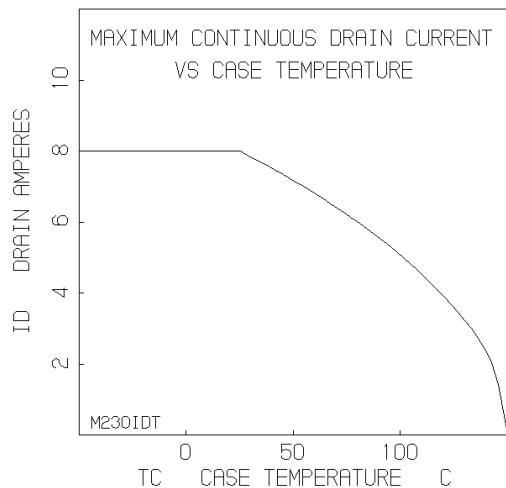
PARAMETER	SYMBOL	TYPE	TEST CONDITIONS	LIMITS		UNITS	
				MIN	MAX		
Drain-Source Breakdown Volts	(Note 4, 6)	BVDSS	2N7274D, R	VGS = 0, ID = 1mA	200	-	V
	(Note 5, 6)	BVDSS	2N7274H	VGS = 0, ID = 1mA	190	-	V
Gate-Source Threshold Volts	(Note 4, 6)	VGS(th)	2N7274D, R	VGS = VDS, ID = 1mA	2.0	4.0	V
	(Note 3, 5, 6)	VGS(th)	2N7274H	VGS = VDS, ID = 1mA	1.5	4.5	V
Gate-Body Leakage Forward	(Note 4, 6)	IGSSF	2N7274D, R	VGS = 20V, VDS = 0	-	100	nA
	(Note 5, 6)	IGSSF	2N7274H	VGS = 20V, VDS = 0	-	200	nA
Gate-Body Leakage Reverse	(Note 2, 4, 6)	IGSSR	2N7274D, R	VGS = -20V, VDS = 0	-	100	nA
	(Note 2, 5, 6)	IGSSR	2N7274H	VGS = -20V, VDS = 0	-	200	nA
Zero-Gate Voltage Drain Current	(Note 4, 6)	IDSS	2N7274D, R	VGS = 0, VDS = 160V	-	25	µA
	(Note 5, 6)	IDSS	2N7274H	VGS = 0, VDS = 160V	-	100	µA
Drain-Source On-state Volts	(Note 1, 4, 6)	VDS(on)	2N7274D, R	VGS = 10V, ID = 8A	-	4.20	V
	(Note 1, 5, 6)	VDS(on)	2N7274H	VGS = 16V, ID = 8A	-	6.30	V
Drain-Source On Resistance	(Note 1, 4, 6)	RDS(on)	2N7274D, R	VGS = 10V, ID = 5A	-	0.500	Ω
	(Note 1, 5, 6)	RDS(on)	2N7274H	VGS = 14V, ID = 5A	-	0.750	Ω

NOTES:

1. Pulse test, 300µs max
2. Absolute value
3. Gamma = 300KRAD(Si)
4. Gamma = 10KRAD(Si) for "D", 100KRAD(Si) for "R". Neutron = 1E13
5. Gamma = 1000KRAD(Si). Neutron = 1E13
6. Insitu Gamma bias must be sampled for both VGS = +10V, VDS = 0V and VGS = 0V, VDS = 80% BVDSS
7. Gamma data taken 3/03/90 on TA17632 devices by GE ASTRO SPACE; EMC/SURVIVABILITY LABORATORY; KING OF PRUSSIA, PA 19401
8. Single event drain burnout testing by Titus, J.L., et al of NWSC, Crane, IN at Brookhaven Nat. Lab. Dec 11-14, 1989
9. Neutron derivation, HARRIS Application note AN-8831, Oct. 1988

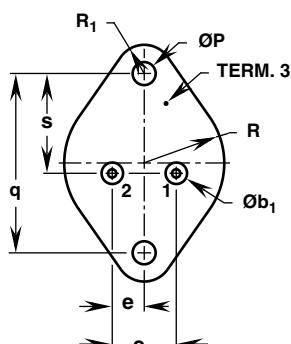
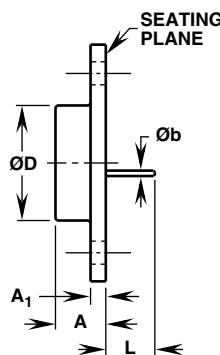
2N7274D, 2N7274R, 2N7274H - Registration Pending

Typical Performance Characteristics



2N7274D, 2N7274R, 2N7274H - Registration Pending

Packaging



NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-204AA outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of seating plane.
5. Controlling dimension: Inch.
6. Revision 1 dated 1-93.

TO-204AA

JEDEC TO-204AA HERMETIC STEEL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.310	0.330	7.88	8.38	-
A ₁	0.060	0.065	1.53	1.65	-
Øb	0.038	0.042	0.97	1.06	2, 3
Øb ₁	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e ₁	0.430 BSC		10.92 BSC		4
L	0.440	0.460	11.18	11.68	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R ₁	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE TM	FAST [®]	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FASTR TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.