FAIRCHILD SEMICONDUCTOR™

January 1993
Revised November 1999

74ABT373
Octal Transparent Latch with 3-STATE Outputs

General Description

The ABT373 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Features

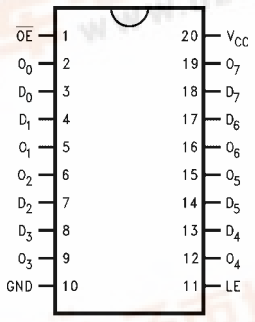
- 3-STATE outputs for bus interfacing
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50 pF and 250 pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down
- Nondestructive hot insertion capability

Ordering Code:

Order Number	Package Number	Package Description
74ABT373CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT373CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT373CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT373CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ABT373CPC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_0–O_7	3-STATE Latch Outputs

Functional Description

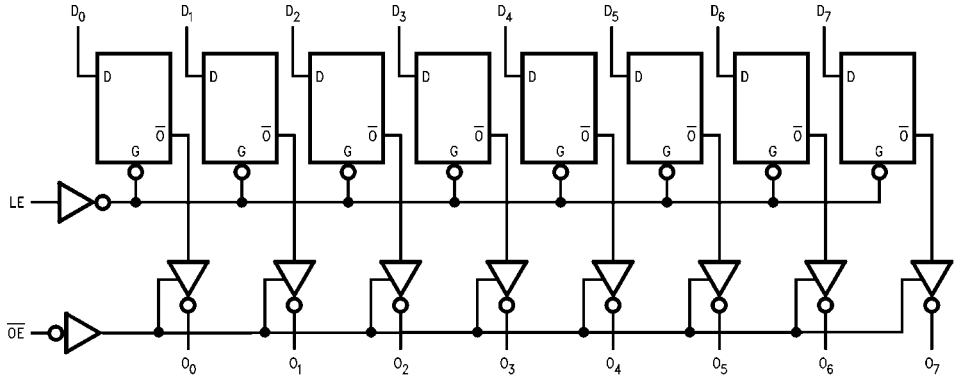
The ABT373 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	**$\overline{OE}$**	**D_n**	**O_n**
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance State

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current:	$\overline{OE}$ Pin −150 mA
(Across Comm Operating Range)	Other Pins −500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		2.5 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −32 mA
V_{OL}	Output LOW Voltage				0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				1 1	μA	Max	V_{IN} = 2.7V (Note 4) V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−1 −1	μA	Max	V_{IN} = 0.5V (Note 4) V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				10	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−10	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				50	μA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				30	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				50	μA	Max	$\overline{OE}$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs 3-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs 3-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC} or GND
I_{CCD}	Dynamic I_{CC} (Note 4)	No Load			0.12	mA/ MHz	Max	Outputs Open, LE = V_{CC} $\overline{OE}$ = GND, (Note 3) One Bit Toggling, 50% Duty Cycle

Note 3: For 8 bits toggling, I_{CCD} < 0.8 mA/MHz.

Note 4: Guaranteed, but not tested.

DC Electrical Characteristics

(SOIC Package)

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions C_L = 50 pF, R_L = 500Ω
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}		0.4	0.8	V	5.0	T_A = 25°C (Note 5)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−1.2	−0.8		V	5.0	T_A = 25°C (Note 5)
V_{OHV}	Minimum HIGH Level Dynamic Output Voltage	2.5	3.0		V	5.0	T_A = 25°C (Note 6)
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	2.0	1.7		V	5.0	T_A = 25°C (Note 7)
V_{ILD}	Maximum LOW Level Dynamic Input Voltage		0.9	0.6	V	5.0	T_A = 25°C (Note 7)

Note 5: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.

Note 6: Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

Note 7: Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

(SOIC and SSOP Packages)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.9	2.7	4.5	1.0	6.8	1.9	4.5	ns
t_{PHL}	D_n to O_n	1.9	2.8	4.5	1.0	7.0	1.9	4.5	
t_{PLH}	Propagation Delay	2.0	3.1	5.0	1.0	7.7	2.0	5.0	ns
t_{PHL}	LE to O_n	2.0	3.0	5.0	1.5	7.7	2.0	5.0	
t_{PZH}	Output Enable Time	1.5	3.1	5.3	1.0	6.7	1.5	5.3	ns
t_{PZL}		1.5	3.1	5.3	1.5	7.2	1.5	5.3	
t_{PHZ}	Output Disable Time	2.0	3.6	5.4	1.7	8.0	2.0	5.4	ns
t_{PLZ}		2.0	3.4	5.4	1.0	7.0	2.0	5.4	

AC Operating Requirements

(SOIC and SSOP Packages)

Symbol	Parameter	T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		T_A = −40°C to +85°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{TOGGLE}	Max Toggle Frequency		100		100				MHz
t_S(H)	Setup Time, HIGH	1.5			2.5		1.5		ns
t_S(L)	or LOW D_n to LE	1.5			2.5		1.5		
t_H(H)	Hold Time, HIGH	1.0			2.5		1.0		ns
t_H(L)	or LOW D_n to LE	1.0			2.5		1.0		
t_W(H)	Pulse Width, LE HIGH	3.0			3.3		3.0		ns

Extended AC Electrical Characteristics

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 8)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF (Note 9)		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 10)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	5.2	2.0	6.8	2.0	9.0	ns
t_{PHL}	D_n to O_n	1.5	5.2	2.0	6.8	2.0	9.0	
t_{PLH}	Propagation Delay	1.5	5.5	2.0	7.5	2.0	9.5	ns
t_{PHL}	LE to O_n	1.5	5.5	2.0	7.5	2.0	9.5	
t_{PZH}	Output Enable Time	1.5	6.2	2.0	8.0	2.0	10.5	ns
t_{PZL}		1.5	6.2	2.0	8.0	2.0	10.5	
t_{PHZ}	Output Disable Time	1.0	5.5	(Note 11)		(Note 11)		ns
t_{PZL}		1.0	5.5					

Note 8: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 9: This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Note 10: This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 11: The 3-STATE delay times are dominated by the RC network (500Ω, 250 pF) on the output and has been excluded from the datasheet.

Skew

(SOIC Package)

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 8 Outputs Switching (Note 12)	$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 8 Outputs Switching (Note 13)	Units
		Max	Max	
t_{OSHL} (Note 14)	Pin to Pin Skew, HL Transitions	1.0	1.5	ns
t_{OSLH} (Note 14)	Pin to Pin Skew, LH Transitions	1.0	1.5	ns
t_{PS} (Note 16)	Duty Cycle, LH–HL Skew	1.4	3.5	ns
t_{OST} (Note 14)	Pin to Pin Skew, LH/HL Transitions	1.5	3.9	ns
t_{PV} (Note 15)	Device to Device Skew, LH/HL Transitions	2.0	4.0	ns

Note 12: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Note 13: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

Note 14: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.

Note 15: Propagation delay variation is for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

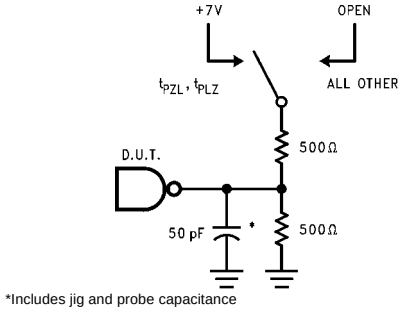
Note 16: This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5	pF	$V_{CC} = 0V$
C_{OUT} (Note 17)	Output Capacitance	9	pF	$V_{CC} = 5.0V$

Note 17: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

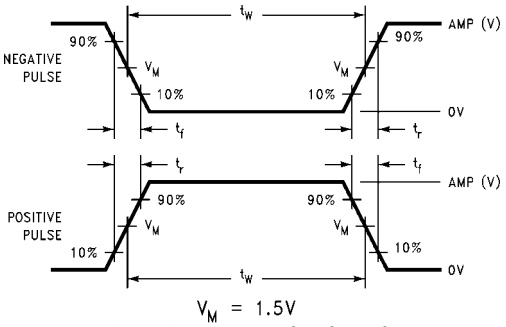


FIGURE 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

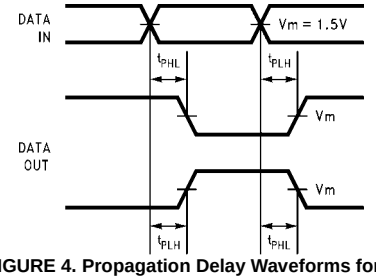


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

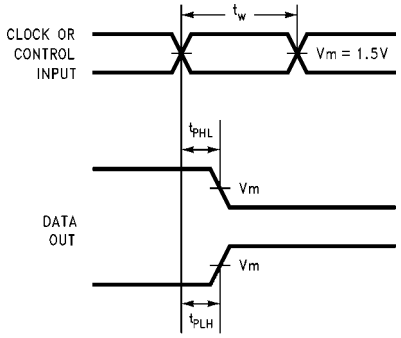


FIGURE 5. Propagation Delay, Pulse Width Waveforms

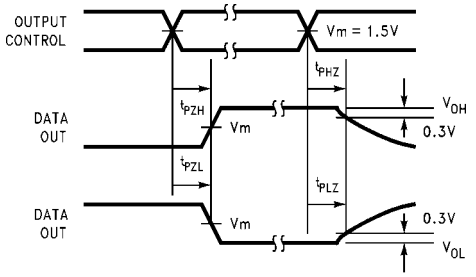


FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times

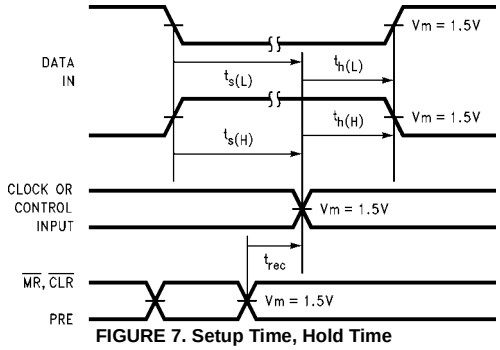
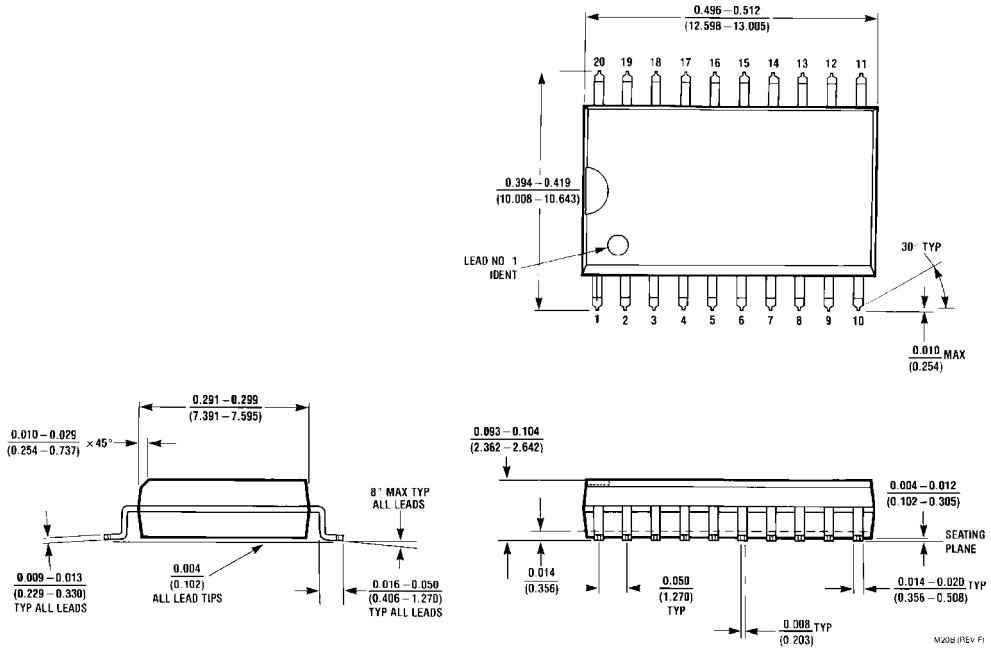


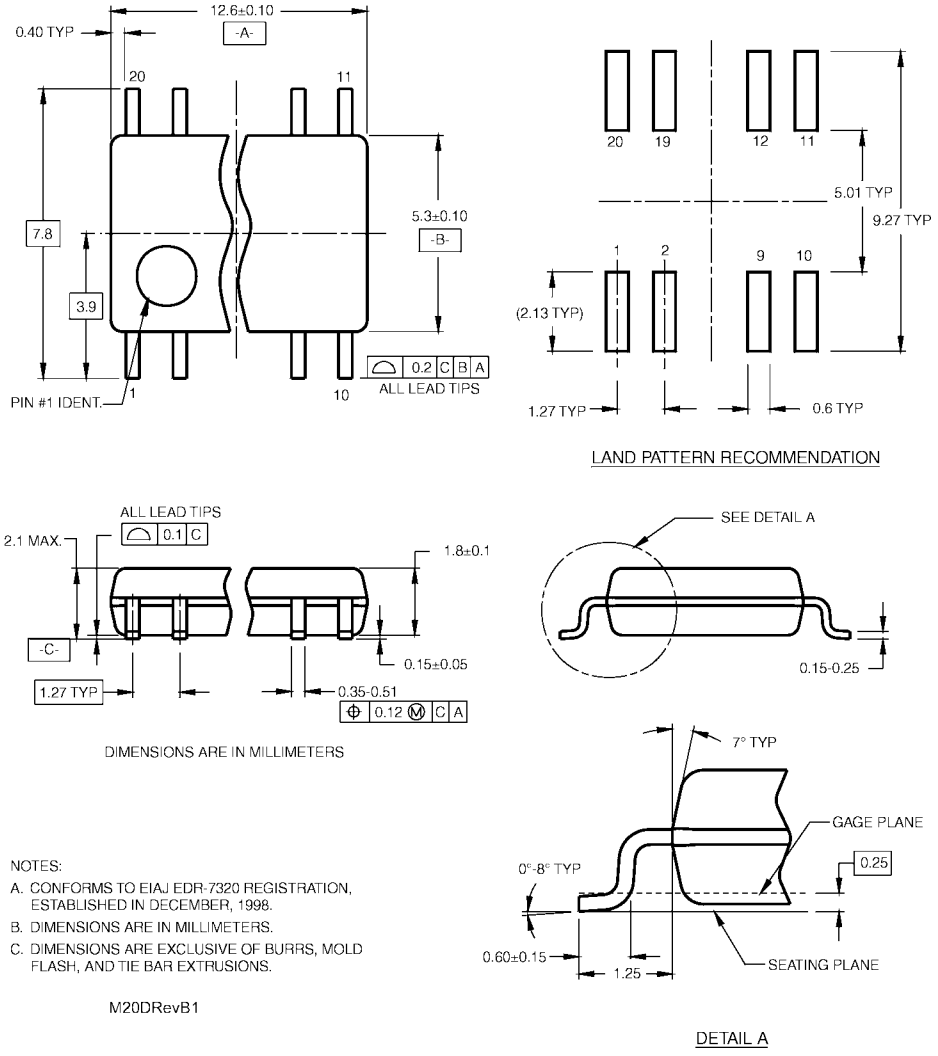
FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

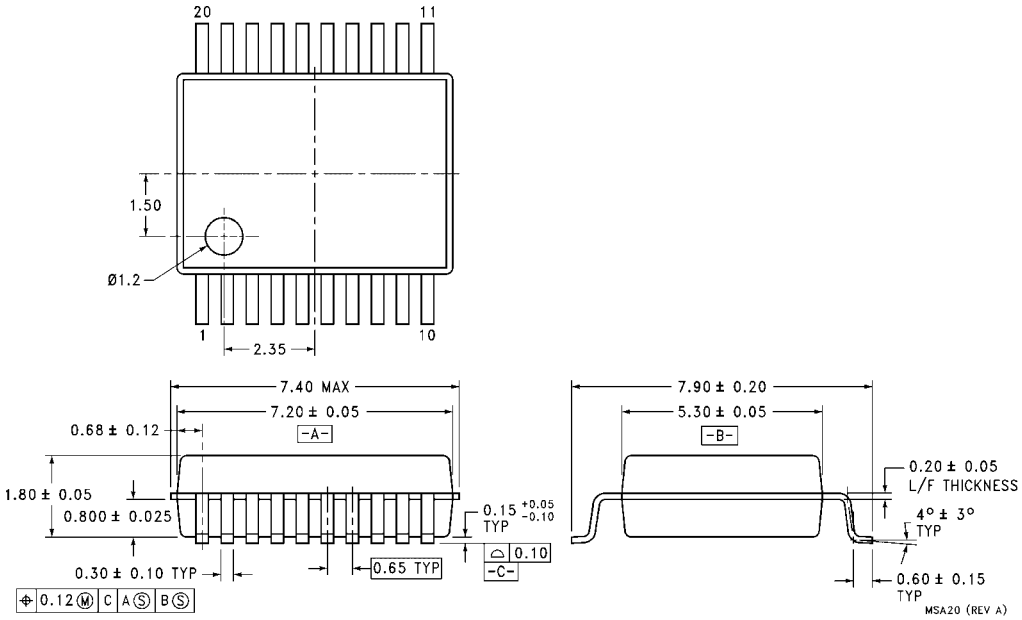
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

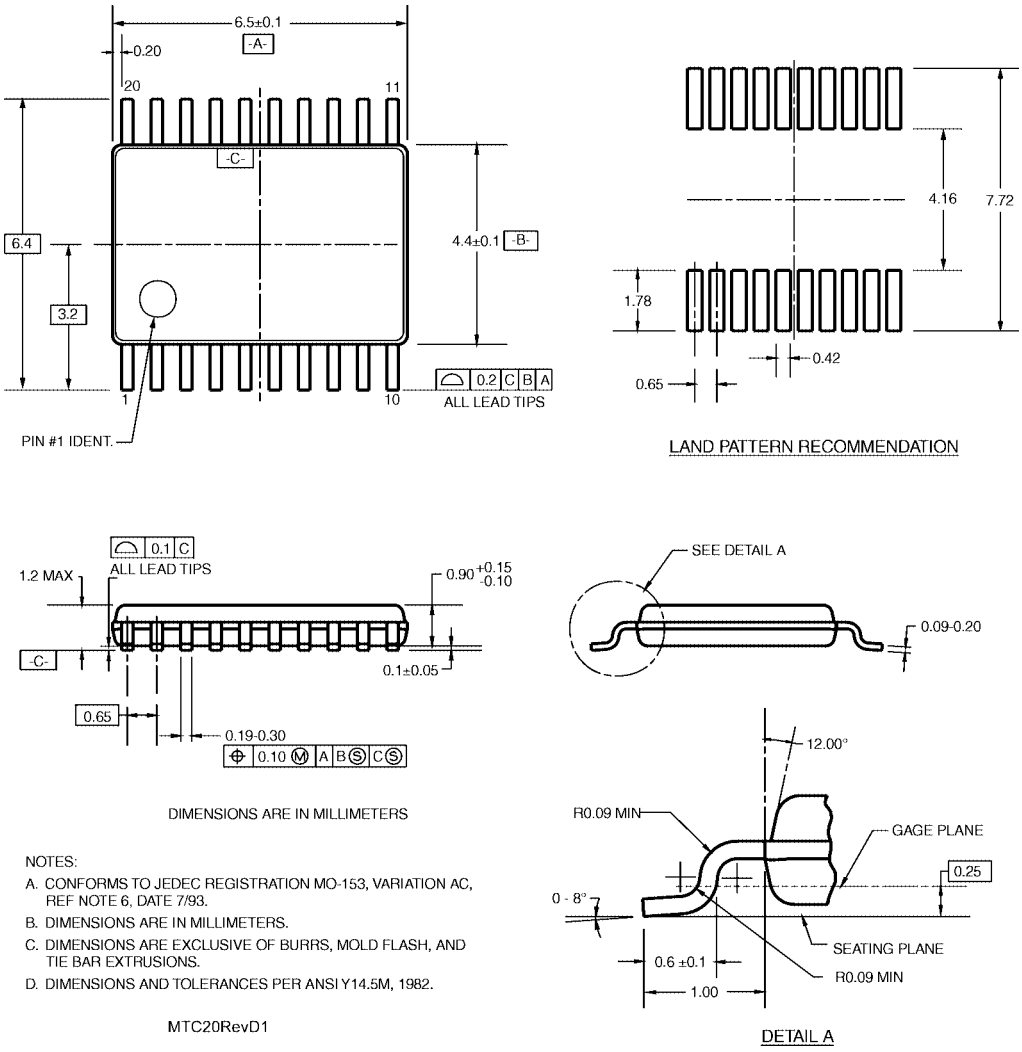
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

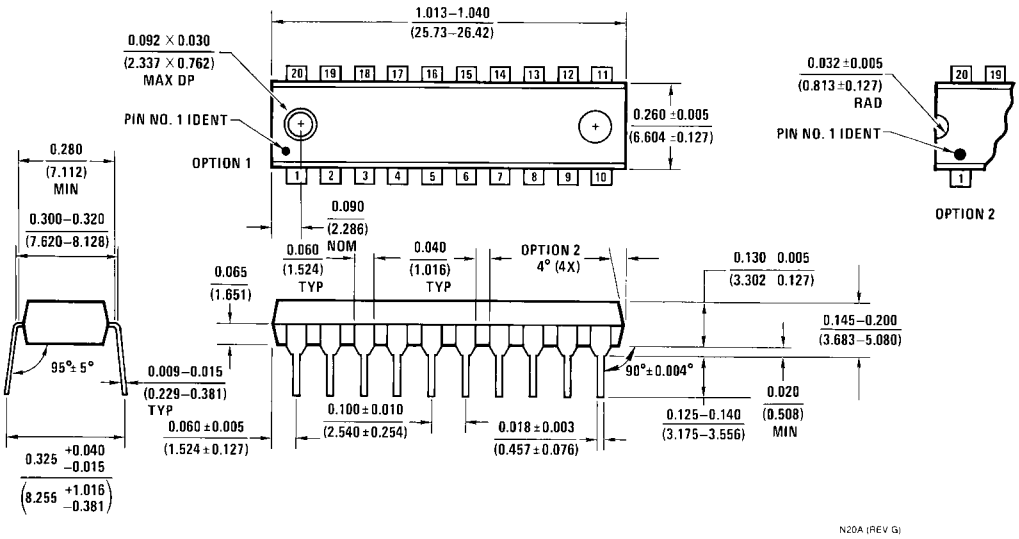
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A