FAIRCHILD SEMICONDUCTOR™

August 1999
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74ACT16374
16-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The ACT16374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (OE) are common to each byte and can be shorted together for full 16-bit operation.

Features

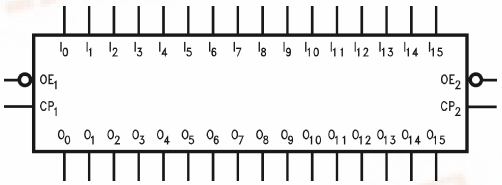
- Buffered Positive edge-triggered clock
- Separate control logic for each byte
- 16-bit version of the ACT374
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

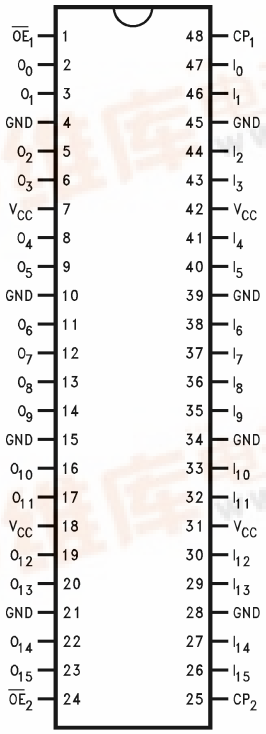
Order Number	Package Number	Package Description
74ACT16374SSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ACT16374MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP_n	Clock Pulse Input
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

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Functional Description

The ACT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

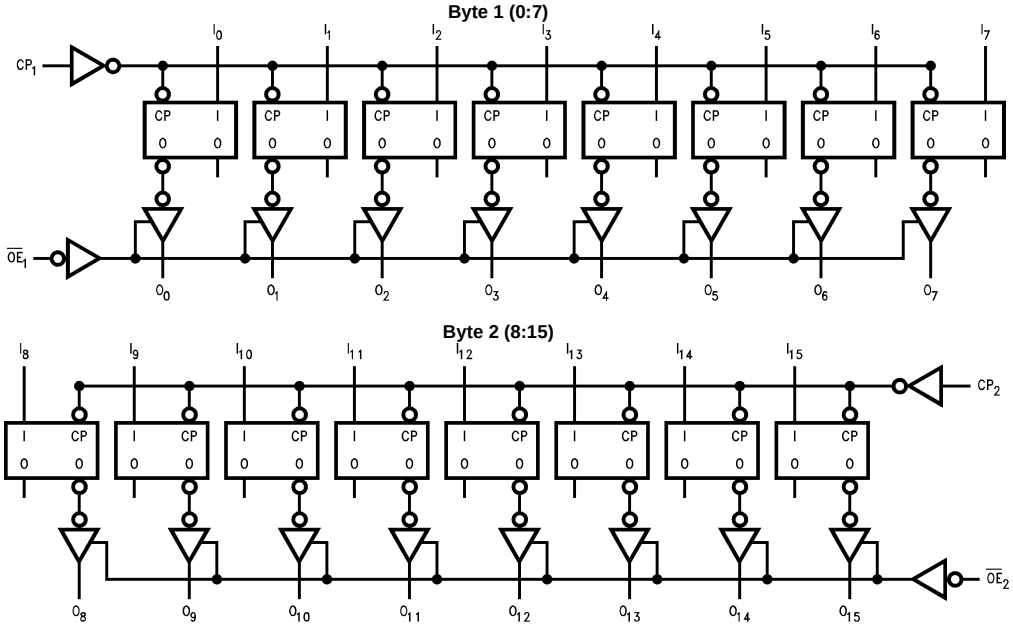
Truth Tables

Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
⌐	L	H	H
⌐	L	L	L
L	L	X	(Previous)
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
⌐	L	H	H
⌐	L	L	L
L	L	X	(Previous)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X= Immaterial
Z = HIGH Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagrams



Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin	± 50 mA
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	125 mV/ns
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$ Typ	$T_A = -40°C$ to $+85°C$ Guaranteed Limits		Units	Conditions
V_{IH}	Minimum HIGH Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum LOW Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum HIGH Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50\ \mu A$
		5.5	5.49	5.4	5.4		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		3.86	3.76	V	$I_{OH} = -24$ mA
		5.5		4.86	4.76		$I_{OH} = -24$ mA (Note 2)
V_{OL}	Maximum LOW Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50\ \mu A$
		5.5	0.001	0.1	0.1		
							$V_{IN} = V_{IL}$ or V_{IH}
		4.5		0.36	0.44	V	$I_{OL} = 24$ mA
		5.5		0.36	0.44		$I_{OL} = 24$ mA (Note 2)
I_{OZ}	Maximum 3-STATE Leakage Current	5.5		± 0.5	± 5.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{IN}	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	µA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	µA	$V_{IN} = V_{CC}$ or GND
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}					−75	mA	$V_{OHD} = 3.85V$ Min

Note 2: All outputs loaded; thresholds associated with output under test.

Note 3: Maximum test duration 2.0 ms; one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 4)	$T_A = +25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	5.0	71			67		MHz
t_{PLH}	Propagation Delay	5.0	3.1	5.3	7.9	3.1	8.4	ns
t_{PHL}	CP to O_n		3.0	5.1	7.3	3.0	7.8	
t_{PZH}	Output Enable Time	5.0	2.5	4.7	7.4	2.5	7.9	ns
t_{PZL}			3.0	5.4	8.0	2.0	8.5	
t_{PHZ}	Output Disable Time	5.0	2.1	5.1	7.9	2.1	8.2	ns
t_{PLZ}			2.0	4.8	7.4	2.0	7.9	

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

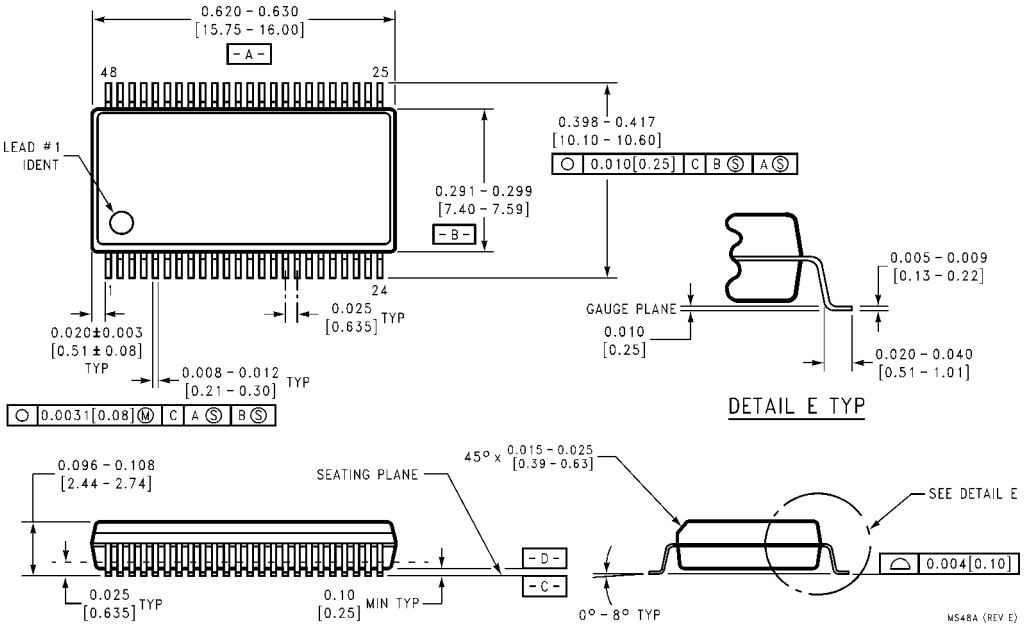
Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = +25°C$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Limits		
t_S	Setup Time, HIGH or LOW, Input to Clock	5.0	0.7	3.0	3.0	ns
t_H	Hold Time, HIGH or LOW, Input to Clock	5.0	0.8	1.0	1.0	ns
t_W	CP Pulse Width, HIGH or LOW	5.0	1.5	5.0	5.0	ns

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

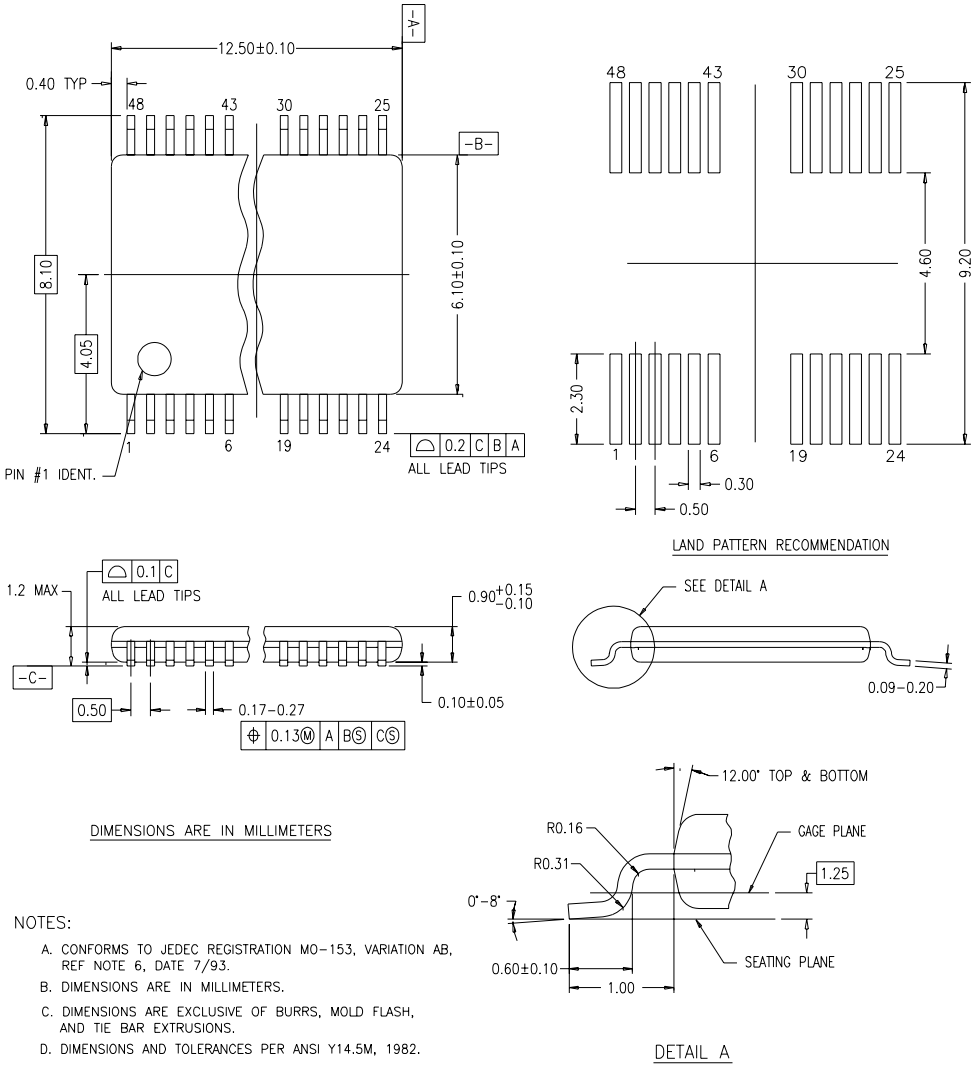
Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	30	pF	$V_{CC} = 5.0V$

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48REVB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48