MN39243FT

6 mm (type-1/3) high-sensitivity CCD area image sensor

■ Overview

The MN39243FT is a 6 mm (type-1/3) interline transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal readout. The electronic shutter function has made an exposure time of 1/10 000 seconds possible. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and super-low smear.

This device has a total of 466 032 pixels (798 horizontal × 584 vertical) and provides stable and clear images with a resolution of 480 horizontal TV-lines and 420 vertical TV-lines.

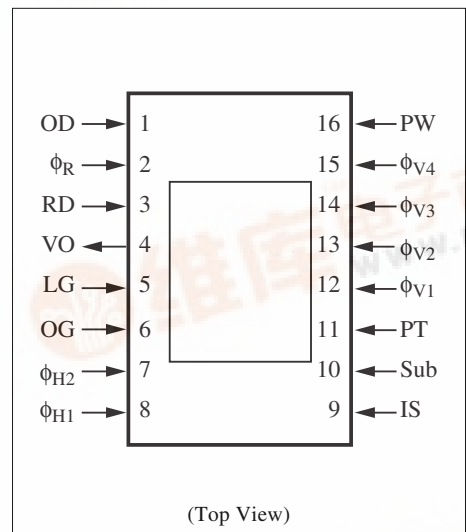| Part Number	Size	System	Color or B/W
MN39243FT	6 mm (type-1/3)	PAL	Color

■ Features

- Total number of pixels: 798 (horizontal) × 584 (vertical)
- High sensitivity
- Broad dynamic range
  (compared to our conventional CCD ×1.2)
- Low smear
- Electronic shutter
- No image distortion
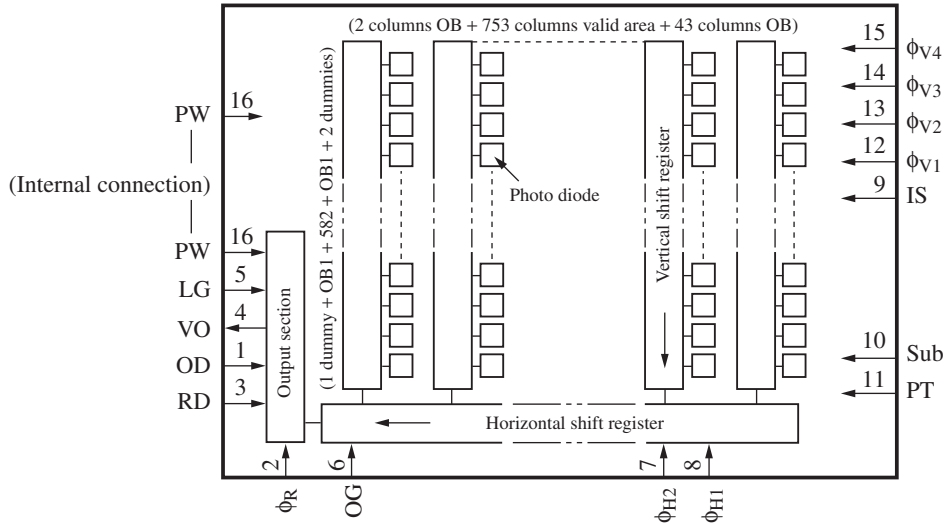- Small size enables design of compact equipment
- High reliability

■ Applications

- Camcorders, surveillance cameras, door cameras

■ Pin Assignment

Pin	Signal		Pin	Signal
1	OD →		16	← PW
2	ϕ_R →		15	← ϕ_{V4}
3	RD →		14	← ϕ_{V3}
4	VO ←		13	← ϕ_{V2}
5	LG →		12	← ϕ_{V1}
6	OG →		11	← PT
7	ϕ_{H2} →		10	← Sub
8	ϕ_{H1} →		9	← IS

(Top View)

■ Block Diagram

■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	9	IS	Horizontal CCD input source
2	ϕ_R	Reset pulse	10	Sub	Substrate
3	RD	Reset drain	11	PT	P-well for protection circuit
4	VO	Video output	12	ϕ_{V1}	Vertical shift register clock pulse 1
5	LG	Output load transistor gate	13	ϕ_{V2}	Vertical shift register clock pulse 2
6	OG	Output gate	14	ϕ_{V3}	Vertical shift register clock pulse 3
7	ϕ_{H2}	Horizontal register clock pulse 2	15	ϕ_{V4}	Vertical shift register clock pulse 4
8	ϕ_{H1}	Horizontal register clock pulse 1	16	PW	P-well

■ Absolute Maximum Ratings and Operating Conditions

Parameter		Symbol	Rating		Operating condition			Unit
			min	max	min	typ	max	
Reset drain voltage		V_{RD}	− 0.2	18.0	14.5	15.0	15.5	V
Output drain voltage		V_{OD}	− 0.2	18.0	14.5	15.0	15.5	V
Output load transistor gate voltage		V_{LG}	(Internal bias)					V
Output gate voltage		V_{OG}	(Internal bias)					V
Horizontal CCD input source voltage		V_{IS}	− 0.2	18.0	14.5	15.0	15.5	V
Protection P-well voltage		V_{PT} [3, 4]	−9.0	0.2	−7.3	−7.0	−6.7	V
P-well voltage		V_{PW}	Reference voltage		—	0	—	V
Reset	High-Low	$V_{\phi R(H-L)}$ [1]	—	5.0	3.0	3.3	3.6	V
pulse voltage	Bias	$V_{\phi R(Bias)}$ [1]	− 0.2	—	Supplied internally			V
Horizontal register		$V_{\phi H1(H)}$	—	5.0	3.0	3.3	3.6	V
clock pulse voltage 1		$V_{\phi H1(L)}$	− 0.2	—	− 0.1	0	0.1	
Horizontal register		$V_{\phi H2(H)}$	—	5.0	3.0	3.3	3.6	V
clock pulse voltage 2		$V_{\phi H2(L)}$	− 0.2	—	− 0.1	0	0.1	
Vertical shift register		$V_{\phi V1(H)}$ [3, 4]	—	18.0	14.5	15.0	15.5	V
clock pulse voltage 1		$V_{\phi V1(M)}$ [3, 4]	—	—	− 0.2	0	0.2	
		$V_{\phi V1(L)}$ [3, 4]	−9.0	—	−7.3	−7.0	−6.7	
Vertical shift register		$V_{\phi V2(M)}$ [3, 4]	—	15.0	− 0.2	0	0.2	V
clock pulse voltage 2		$V_{\phi V2(L)}$ [3, 4]	−9.0	—	−7.3	−7.0	−6.7	
Vertical shift register		$V_{\phi V3(H)}$ [3, 4]	—	18.0	14.5	15.0	15.5	V
clock pulse voltage 3		$V_{\phi V3(M)}$ [3, 4]	—	—	− 0.2	0	0.2	
		$V_{\phi V3(L)}$ [3, 4]	−9.0	—	−7.3	−7.0	−6.7	
Vertical shift register		$V_{\phi V4(M)}$ [3, 4]	—	15.0	− 0.2	0	0.2	V
clock pulse voltage 4		$V_{\phi V4(L)}$ [3, 4]	−9.0	—	−7.3	−7.0	−6.7	
Substrate voltage		V_{Sub} [2]	− 0.2	45.0	Supplied internally			V
		ϕV_{Sub} [2]			21.0	22.0	23.0	
Operating temperature		T_{opr}	−10	70	—	25	—	°C
Storage temperature		T_{stg}	−30	80	—	—	—	°C

Note) ∗1: Reset
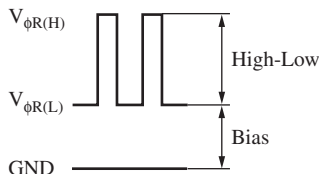
∗2: V_{Sub} when using electronic shutter function
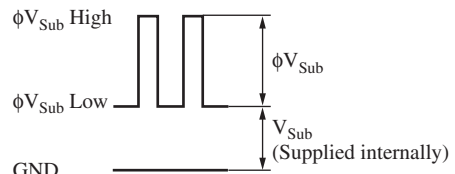
∗3: Absolute maximum rating $− 0.2 < V_{\phi V} − V_{PT} < 24.5$ (V)

∗4: Relation between V_{PT} and $V_{\phi V(L)}$
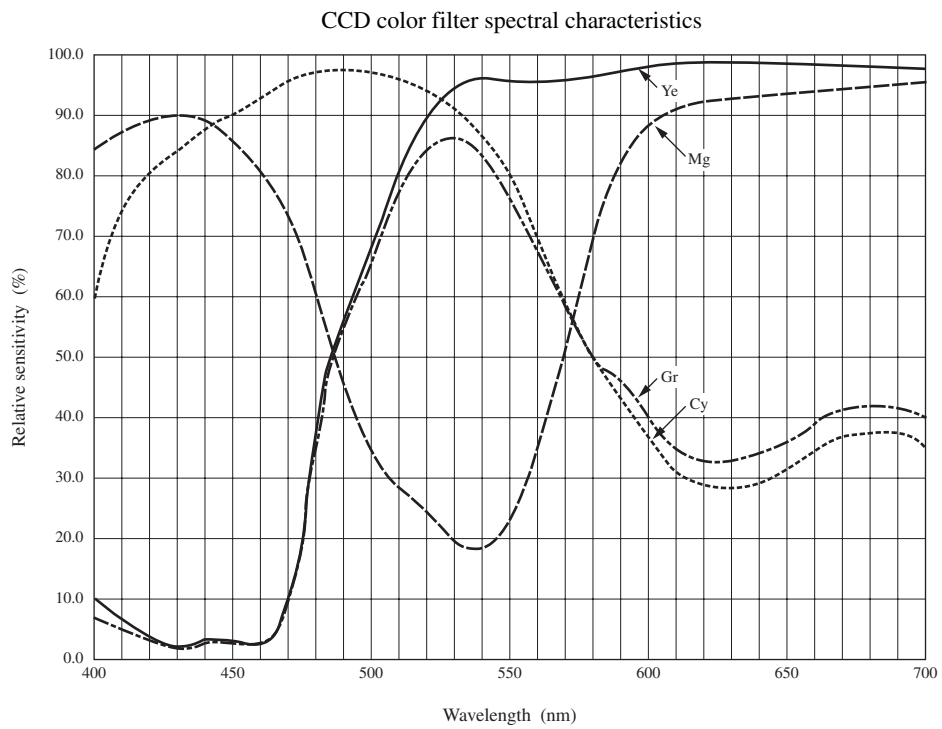
Set V_{PT} that is to meet the following conditions for VL voltage of the vertical shift clock waveform.

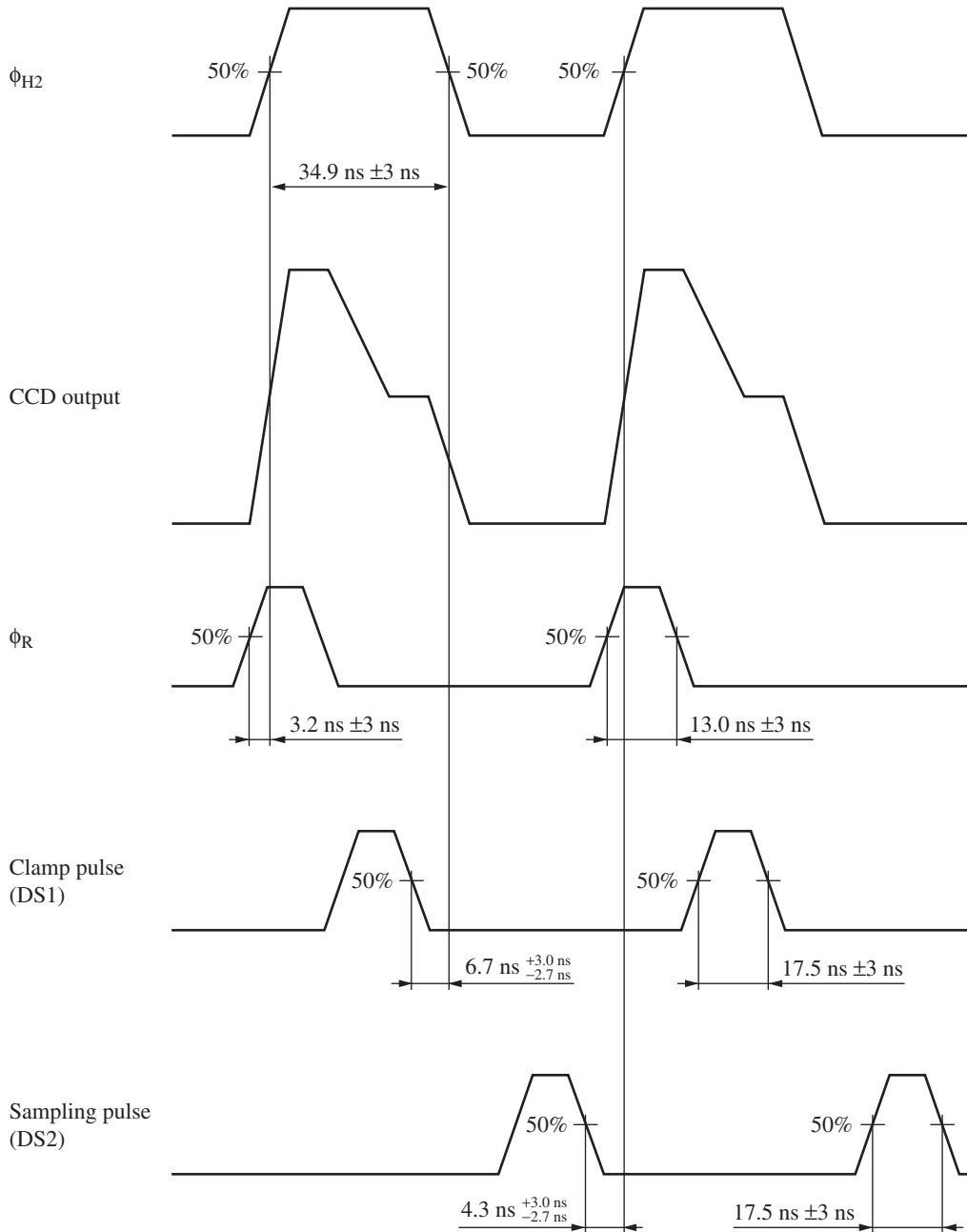$V_{PT} \le VL$ ($V_{\phi V1(L)}$ to $V_{\phi V4(L)}$)

■ Optical Characteristics

Part Number	Color or B/W	Effective pixels		Saturation output typ (mV)	Sensitivity F8 typ (mV)	Vertical smear Sm typ (dB)	Horizontal resolution typ (TV-lines)	Vertical resolution typ (TV-lines)
		H	V					
MN39243FT	Color	737	575	750	450	−100	480	420

■ Graph of Characteristics

CCD color filter spectral characteristics

Relative sensitivity (%) vs Wavelength (nm)

■ Timing Diagram

• High speed pulse timing

ϕ_{H2}

34.9 ns ±3 ns

CCD output

ϕ_R

3.2 ns ±3 ns   13.0 ns ±3 ns

Clamp pulse (DS1)

6.7 ns $^{+3.0\ ns}_{-2.7\ ns}$ 17.5 ns ±3 ns

Sampling pulse (DS2)

4.3 ns $^{+3.0\ ns}_{-2.7\ ns}$ 17.5 ns ±3 ns

■ Timing Diagram (continued)

• Rise time and fall time of each pulse

ϕ_{V1} , ϕ_{V3}

0.9   0.9

0.9 — 0.1

0.1 — 0.1

0.1

0.1

≤300 ns   ≤300 ns   ≤300 ns   ≤300 ns

ϕ_{V2} , ϕ_{V4}

0.9   0.9

0.1   0.1

≤300 ns   ≤300 ns

ϕ_{H1} , ϕ_{H2} , ϕ_R

0.9   0.9

0.1   0.1

≤10 ns   ≤10 ns

DS1, DS2

0.9   0.9

0.1   0.1

≤10 ns   ≤10 ns
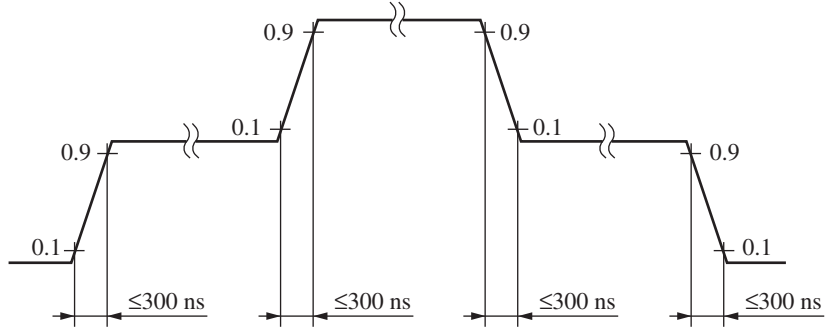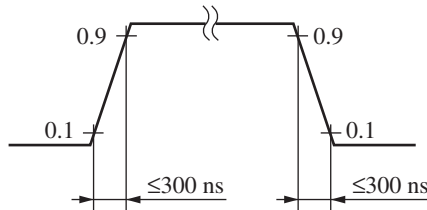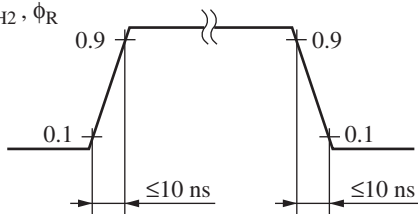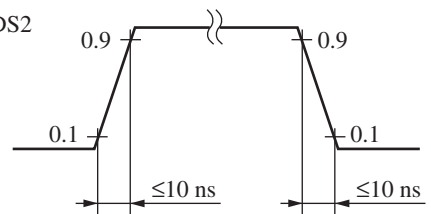
■ Package Dimensions (unit: mm)

• WDIP016-P-0500C

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