19-0400; Rev 0; 5/95

EVALUATION KIT AVAILABLE

MAXIM

330MHz, 4x1 Precision Video Multiplexer

MAX4141

General Description

The MAX4141 is a wideband 330MHz, 700V/µs 4x1 multiplexer optimized for high-definition, broadcast-quality, composite (HDTV, NTSC, PAL, SECAM) video switching arrays. The device includes four open-loop buffer amplifiers with a 0.1dB gain flatness of 150MHz, and enable and switch-control logic. The MAX4141 operates from ±5V supplies and features differential phase and gain error of only 0.01°/0.01%. The ultra-low switching glitch (less than 13mV) is positive to avoid confusion with any sync pulses.

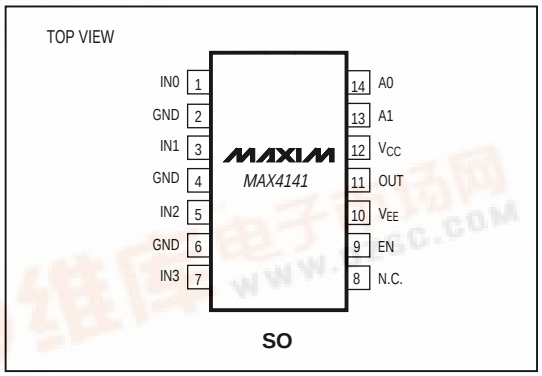
Ideal as a building block for large switch arrays, the MAX4141 features a constant, high input impedance and a disable function that puts the output into a high-impedance state and reduces the operating current to only 250µA. The open-loop architecture allows the output to drive capacitive loads without oscillation.

Other key features include -66dB crosstalk (30MHz), -74dB isolation (30MHz), less than 10mV offset voltage, and a 110MHz full-power bandwidth (1.4Vp-p). The MAX4141 is available in a 14-pin narrow SO package.

Applications

Broadcast/HDTV-Quality Color Signal Multiplexing
Video Routers and Crosspoint Arrays
RF and IF Routing
Graphics Color Signal Routing
Telecom Routing
Data Acquisition

Pin Configuration



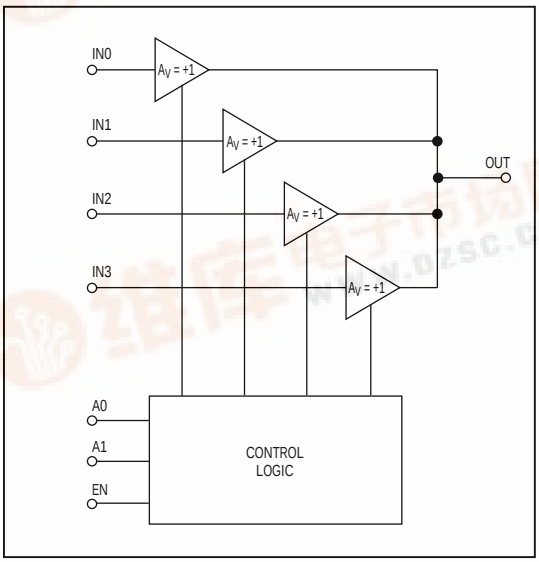
Features

- ♦ 330MHz -3dB Bandwidth
- ♦ 0.1dB Gain Flatness of 150MHz
- ♦ 700V/µs Slew Rate
- ♦ 0.01°/0.01% Differential Phase/Gain
- ♦ -66dB Crosstalk and -74dB Isolation at 30MHz
- ♦ High-Z Outputs when Disabled
- ♦ 3pF Input Capacitance
- ♦ Low Switching Glitch
- ♦ On-Board Control Logic

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4141CSD	0°C to +70°C	14 SO

Functional Diagram



330MHz, 4x1 Precision Video Multiplexer

ABSOLUTE MAXIMUM RATINGS

V_{CC}.....6V
V_{EE}.....-6V
V_{CC}-V_{EE}.....12V
Analog Input Voltage .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Digital Input Voltage.....-0.3V to (V_{CC} + 0.3V)
Duration of Short Circuit to Ground.....Continuous (Note 1)

Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.00mW/°C above +70°C).....640mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range.....-65°C to +160°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: If maximum power-dissipation rating is met.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_S = ±5V, -2.5V ≤ V_{IN} ≤ +2.5V, R_L = 5kΩ, C_L = 5pF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PARAMETERS							
Operating Supply Voltage	V_S			±4.5	±5.0	±5.5	V
Operating Supply Current	$I_{S(ON)}$	Enabled	T_A = +25°C		5.0	5.5	mA
			T_A = T_{MIN} to T_{MAX}			6.5	
Disabled Supply Current	$I_{S(OFF)}$				250	350	µA
Input Voltage Range	V_{IN}			±2.5			V
Input Bias Current	I_B	V_{IN} = 0V	Channel selected		±2.5	±4.0	µA
			Channel disabled		±0.2		
Input Resistance	R_{IN}	Channel selected			0.4		MΩ
		Channel disabled			100		
Input Capacitance	C_{IN}	V_{IN} = 0V, channel enabled or disabled			3		pF
Output Offset Voltage	V_{OS}	T_A = +25°C			±3	±10	mV
		T_A = T_{MIN} to T_{MAX}				±15	
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V		50			dB
Voltage Gain	A_V	V_{IN} = ±2.5V	T_A = +25°C	0.98		1.0	V/V
			T_A = T_{MIN} to T_{MAX}	0.97		1.0	
Output Resistance	R_{OUT}				20		Ω
Disabled Output Current	$I_{OUT(OFF)}$	V_{OUT} = 0V			10		nA
Disabled Output Resistance	R_{OUT}				30		MΩ
Disabled Output Capacitance	C_{OUT}				5		pF
Logic Input High Voltage	V_{INH}	V_S = ±4.5V to ±5.5V		2.0			V
Logic Input Low Voltage	V_{INL}	V_S = ±4.5V to ±5.5V				0.8	V
Logic Input High Current	I_{INH}	V_S = ±4.5V to ±5.5V				10	µA
Logic Input Low Current	I_{INL}	V_S = ±4.5V to ±5.5V				10	µA

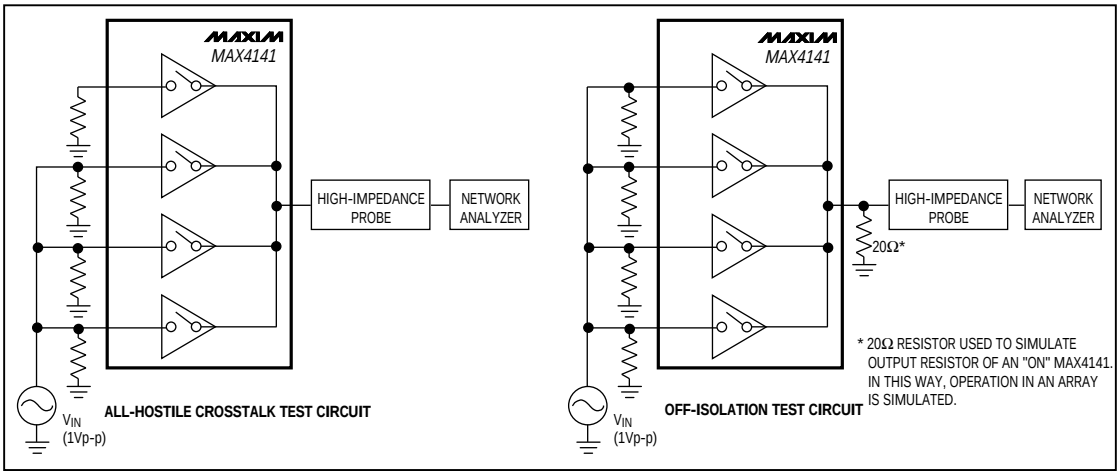
ELECTRICAL CHARACTERISTICS (continued)

(V_S = ±5V, -2.5V ≤ V_{IN} ≤ +2.5V, R_L = 5kΩ, C_L = 5pF, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PARAMETERS						
Slew Rate	SR	V_{IN} = 5Vp-p		700		V/µs
		V_{IN} = 1.4Vp-p		500		
Full-Power Bandwidth (Note 2)	f_{PBW}	V_{IN} = 1.4Vp-p		110		MHz
		V_{IN} = 5Vp-p		45		
-3dB Bandwidth	f_{3dB}	V_{IN} = 0.1Vp-p		330		MHz
Gain Flatness		DC to 30MHz		0.02		dB
		DC to 150MHz		±0.1		
Gain Peaking				0.08		dB
Small-Signal Rise Time	t_R	V_{IN} = 0.2Vp-p, 10% to 90%		950		ps
Differential Gain (Note 3)	DG	f = 3.58MHz		0.01		%
Differential Phase (Note 3)	DP	f = 3.58MHz		0.01		degrees
All-Hostile Crosstalk		V_{IN} = 1Vp-p, f = 30MHz, R_{IN} = 50Ω		66		dB
Off Isolation		V_{IN} = 1Vp-p, f = 30MHz		74		dB
Channel Switching Off Time	t_{OFF}			1.0		µs
Channel Switching On Time	t_{ON}			500		ns
Switching Transient				13		mVp-p
Group Delay		f = 3.58MHz		860		ps
Input-Output Delay Matching		Chip-to-chip, f = 3.58MHz		±0.2		degrees
Second Harmonic Distortion		f = 30MHz, V_{IN} = 1.4Vp-p, R_L = 2k		-65		dBc
Third Harmonic Distortion		f = 30MHz, V_{IN} = 1.4Vp-p, R_L = 2k		-70		dBc

Note 2: Full-Power Bandwidth is inferred from Slew Rate (SR) testing by the equation SR = ωE_P, where E_P is the peak output voltage and $\omega = 2\pi f$.

Note 3: Differential Gain and Phase are tested using a modulated ramp, 100IRE (0.714V).

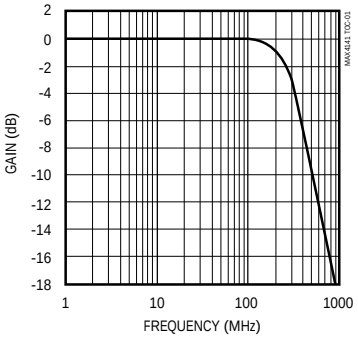


330MHz, 4x1 Precision Video Multiplexer

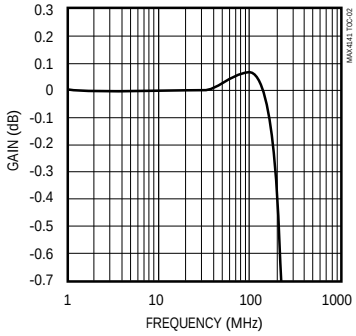
Typical Operating Characteristics

(V_S = ±5V, R_L = 5kΩ, C_L = 1pF, T_A = +25°C, unless otherwise noted.)

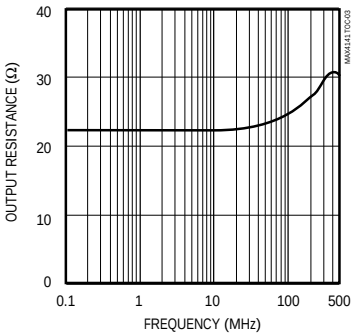
GAIN vs. FREQUENCY



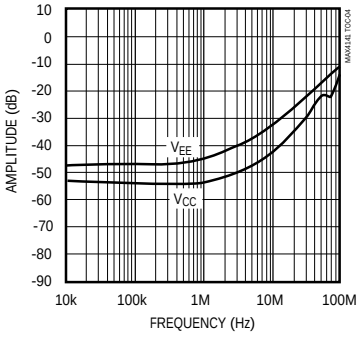
GAIN FLATNESS



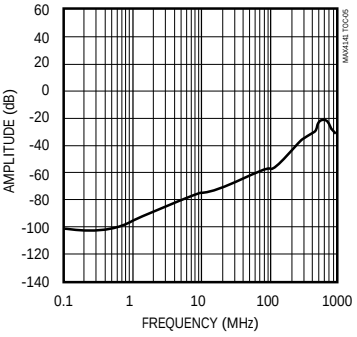
OUTPUT RESISTANCE vs. FREQUENCY



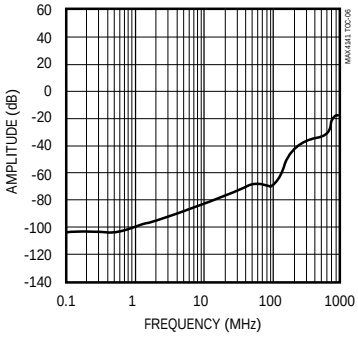
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



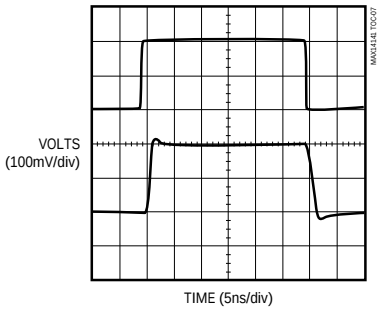
ALL-HOSTILE CROSSTALK vs. FREQUENCY



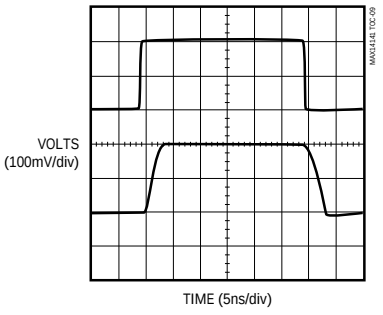
OFF ISOLATION vs. FREQUENCY



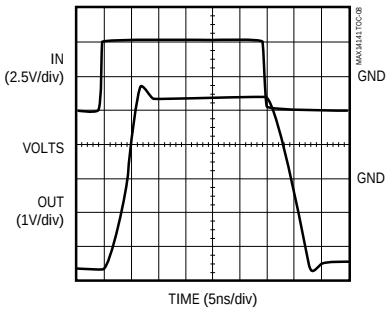
SMALL-SIGNAL PULSE RESPONSE
(C_L = 0pF, R_L = 5kΩ)



SMALL-SIGNAL PULSE RESPONSE
(C_L = 47pF, R_L = ∞)



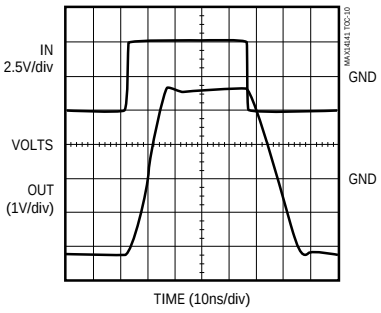
LARGE-SIGNAL PULSE RESPONSE
(C_L = 0pF, R_L = 5kΩ)



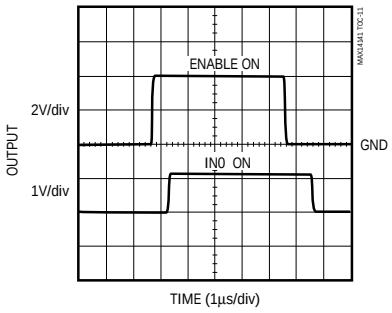
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

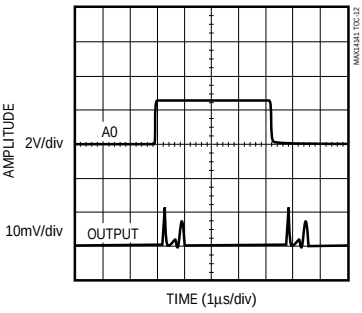
LARGE-SIGNAL PULSE RESPONSE
(C_L = 47pF, R_L = ∞)



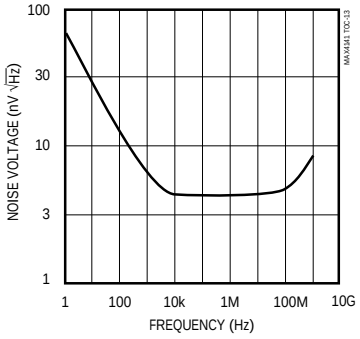
ENABLE/DISABLE DELAY TIME



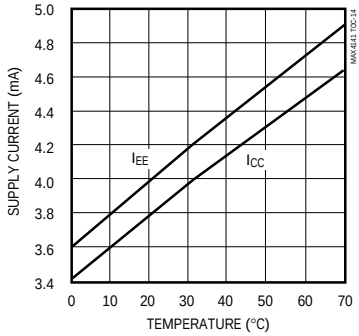
OUTPUT GLITCH AMPLITUDE



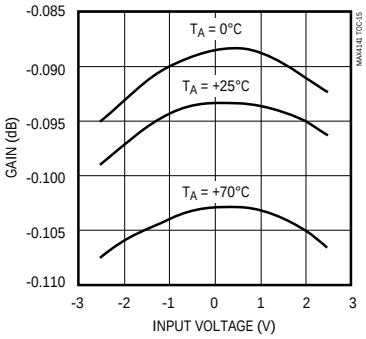
NOISE VOLTAGE vs. FREQUENCY



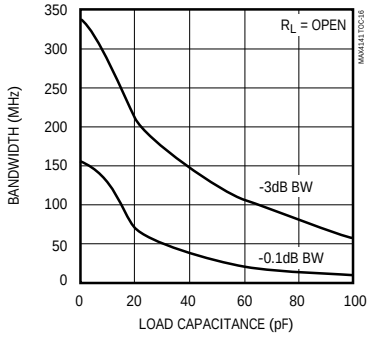
SUPPLY CURRENT vs. TEMPERATURE



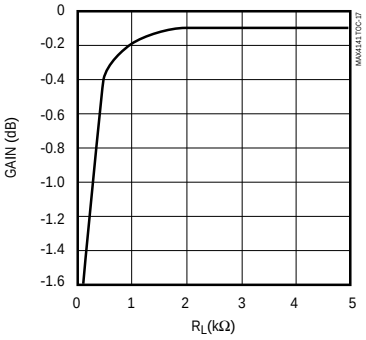
GAIN vs. INPUT VOLTAGE AND TEMPERATURE



BANDWIDTH vs. LOAD CAPACITANCE



GAIN vs. LOAD RESISTANCE



330MHz, 4x1 Precision Video Multiplexer

Pin Description

PIN	FUNCTION	DESCRIPTION
1	IN0	Signal Input
2, 4, 6	GND	Analog (Signal) Ground. Since inputs are isolated by these grounds, they should be as noise-free as possible.
3	IN1	Signal Input
5	IN2	Signal Input
7	IN3	Signal Input
8	N.C.	No Connect—not internally connected.
9	EN	Output Enable and device shutdown. A logic high on this pin enables the output. A logic low causes the output to assume a high-impedance state and reduces operating current.
10	V_{EE}	Negative Power-Supply Voltage. Decouple to power ground.
11	OUT	Signal Output
12	V_{CC}	Positive Power-Supply Voltage. Decouple to power ground.
13	A1	Channel Selection Bit. See truth tables.
14	A0	Channel Selection Bit. See truth tables.

Detailed Description

The MAX4141 video switch is manufactured with Maxim's proprietary complementary bipolar process that yields high bandwidth and low capacitance. To maintain a wide bandwidth, the MAX4141 incorporates a straightforward structure of input and output buffers. Make-before-break switching is employed to reduce noise and glitches, even when switching from part to part in large arrays. The input buffers provide a constant, high input impedance. And, they prevent the make-before-break action from feeding back to the input and causing noise and/or glitches.

The design of the switching mechanism limits the inevitable glitch to within 13mVp-p. In addition, the glitch pulse is positive to avoid confusion with any negative sync pulses.

Unity-gain output buffers isolate other inputs from the switching action of large multiplex arrays. These buffers can drive 5kΩ resistive loads. Load capacitance is limited only by system bandwidth requirements.

The MAX4141 does not contain buffer latches. The digital inputs control the switch transparently.

Applications Information

Grounding, Bypassing, and PC Board Layout

In order to obtain the MAX4141's full 330MHz bandwidth, Microstrip and Stripline techniques are recommended in most cases. To ensure your PC board does not degrade the switch's performance, it's wise to design the board for a frequency greater than 1GHz. Even with very short runs, it's good practice to use this technique at critical points, such as inputs and outputs. Whether you use a constant-impedance board or not, observe the following guidelines when designing the board:

- Do not use wire-wrap boards, because they are too inductive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- In general, surface-mount components have shorter leads and lower parasitic reactance, and give better high-frequency performance than through-hole components.
- The PC board should have at least two layers, with one side a signal layer and the other a ground plane.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.
- The ground plane should be as free from voids as possible.

On Maxim's evaluation kit, the ground plane has been removed from areas where keeping the trace capacitance to a minimum is more important than maintaining ground continuity. For example, the ground plane has been removed from beneath the IC to minimize pin capacitance.

The signal input line is approximately 0.103 inches wide to minimize inductance and to provide a constant 50Ω impedance path. It is terminated by a 50Ω chip resistor.

Bypass Components—Capacitors

Electrolytic and tantalum capacitors are available from 0.1µF to over 300µF, but have resonant frequencies below 1MHz. Ceramic capacitors are highly recommended and are available to 1µF, with the smaller values having resonant frequencies to almost 1GHz. The less expensive capacitors are constructed using a multilayer approach; high values are available, but resonant frequencies beyond a few hundred megahertz are not, because of the inductive effect of the multiple layers. More expensive, solid dielectric microwave porcelain/ceramic capacitors are available up to 1000pF with resonant frequencies beyond 20GHz. In all types, resonant frequency depends on capacitor value, voltage rating, and physical size; the larger the capacitor, the lower the resonant frequency.

We recommend ceramic surface-mount/chip capacitors. Placement of bypass capacitors on the PC board is critical, and the smaller chip capacitors allow placement as close to the part as practical. The smaller, higher frequency capacitors should be placed as close to the chip as possible, with the higher-value capacitors placed farther away.

Creating Large Arrays

The MAX4141 was designed as a building block for large arrays. The high-power drive required for internal cable drivers has a negative effect on crosstalk and increases system power consumption. Figure 1 shows an 8x1 multiplexer circuit.

Even though the MAX4141 drives capacitive loads, you may want to limit the number of switches connected together to maximize bandwidth. The MAX4141 has a finite input capacitance of about 3pF and a dynamic output resistance of about 20Ω. This causes a pole at a little more than 2.6GHz. However, in a large array with many switch inputs, the total capacitance is (N x 3pF), where "N" is the number of switches connected in parallel. The pole will be located at:

$$\frac{1}{2\pi \times \left(N \times 3pF + C_{STRAY}\right) \times 20\Omega} \text{ MHz}$$

where C_{STRAY} is the stray capacitance from the interconnect.

If the maximum number of switches that may be connected while still maintaining bandwidth is less than your system requirements, use a unity-gain buffer amplifier to isolate the switch from the remainder of the inputs.

Table 1. Truth Table

A1	A0	EN	OUT
X	X	0	High-Z
0	0	1	IN0
0	1	1	IN1
1	0	1	IN2
1	1	1	IN3

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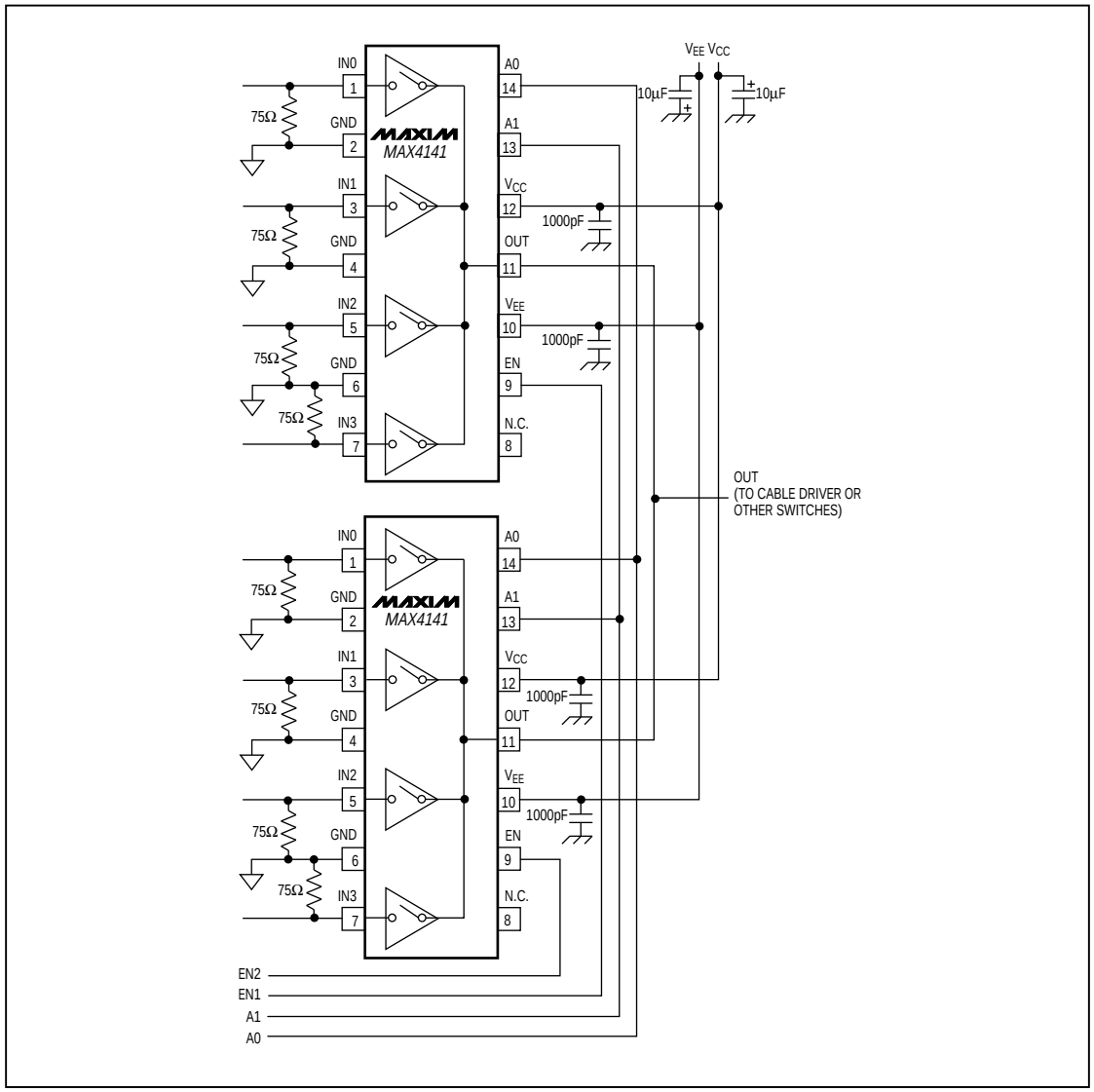

Figure 1. 8x1 Multiplexer Circuit