

FAIRCHILD
SEMICONDUCTOR™

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74F27 Triple 3-Input NOR Gate

General Description

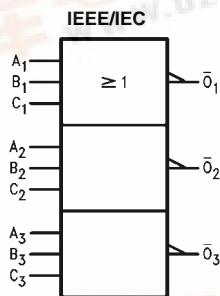
This device contains three independent gates, each of which performs the logic NOR function.

Ordering Code:

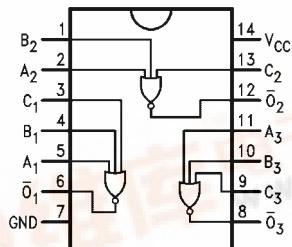
Order Number	Package Number	Package Description
74F27SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F27SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F27PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL}	Output I_{OH}/I_{OL}
A_n, B_n, C_n	Data Inputs	1.0/1.0	20 μ A/-0.6 mA	
\bar{O}_n	Data Outputs	50/33.3		-1 mA/20 mA

Function Table

Inputs			Output
A_n	B_n	C_n	\bar{O}_n
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	-0.5V to V_{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

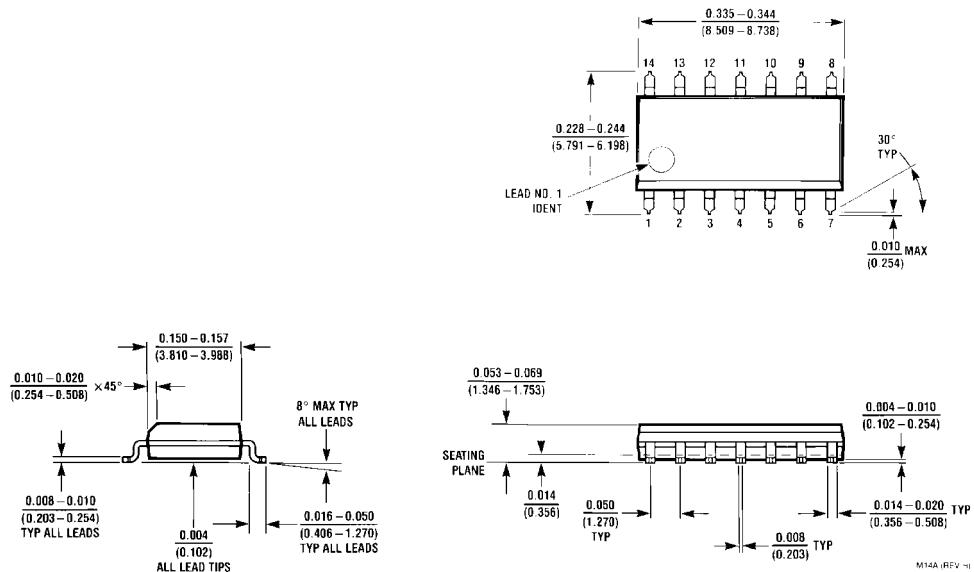
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18\text{ mA}$
V_{OH}	Output HIGH Voltage	10% V_{CC} 5% V_{CC}	2.5 2.7		V	Min	$I_{OH} = -1\text{ mA}$ $I_{OH} = -1\text{ mA}$
V_{OL}	Output LOW Voltage	10% V_{CC}		0.5	V	Min	$I_{OL} = 20\text{ mA}$
I_{IH}	Input HIGH Current			5.0	μA	Max	$V_{IN} = 2.7\text{ V}$
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	$V_{IN} = 7.0\text{ V}$
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	μA	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
I_{IL}	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5\text{ V}$
I_{OS}	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0\text{ V}$
I_{CCH}	Power Supply Current		4.0	5.5	mA	Max	$V_O = \text{HIGH}$
I_{CCL}	Power Supply Current		8.7	12.0	mA	Max	$V_O = \text{LOW}$

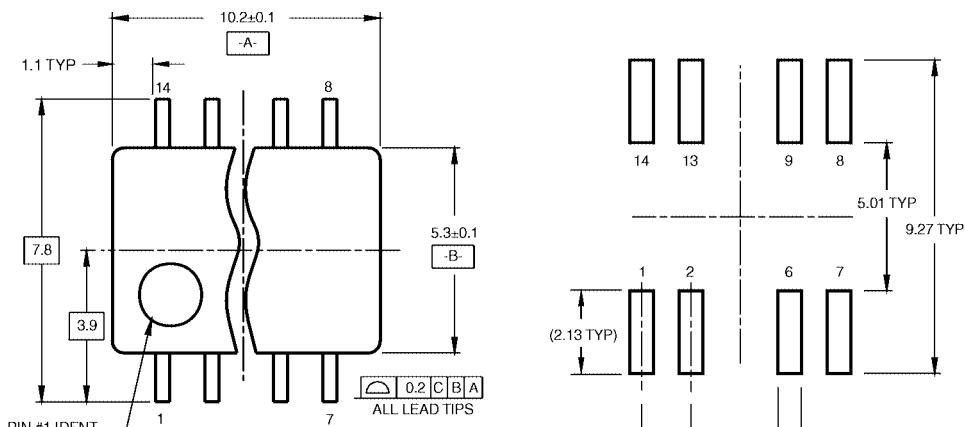
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = 0^\circ\text{C to }+70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	2.0	3.8	6.0	1.5	6.5	ns
t_{PHL}		1.0	2.6	4.0	1.0	4.5	

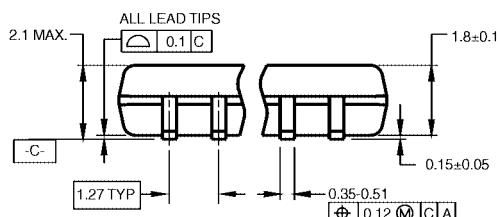
Physical Dimensions inches (millimeters) unless otherwise noted



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

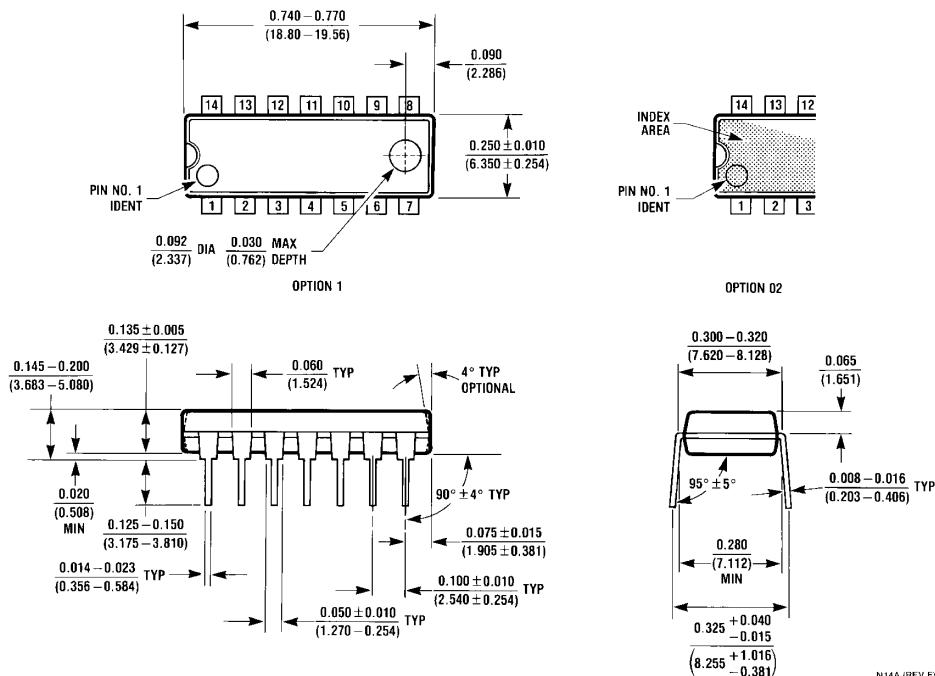
M14DRevB1

The diagram shows a cross-section of a stepped component. A vertical line on the left is labeled $0^\circ\text{--}8^\circ\text{ TYP}$ with a dimension of 0.60 ± 0.15 . A horizontal line at the bottom is labeled 1.25 . A horizontal dashed line represents the **SEATING PLANE**. A vertical dashed line represents the **GAGE PLANE**. A dimension of 0.25 is shown between the seating plane and the gage plane. An angle of 7° TYP is indicated between the seating plane and the top surface of the component. Arrows point from the labels to their respective features.

DETAIL A

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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