

FAIRCHILD
SEMICONDUCTOR™

April 1988
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74F30 8-Input NAND Gate

General Description

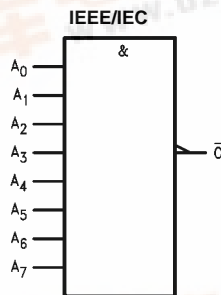
This device contains a single gate, which performs the logic NAND function.

Ordering Code:

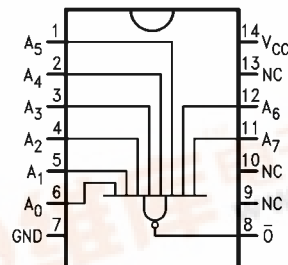
Order Number	Package Number	Package Description
74F30SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F30SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F30PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0 – A_7	Inputs	1.0/1.0	20 μ A/–0.6 mA
\bar{O}	Output	50/33.3	–1 mA/20 mA

Function Table

Inputs								Output
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	\bar{O}
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

74F30 8-Input NAND Gate

Absolute Maximum Ratings(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	–0.5V to V _{CC}
3-STATE Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

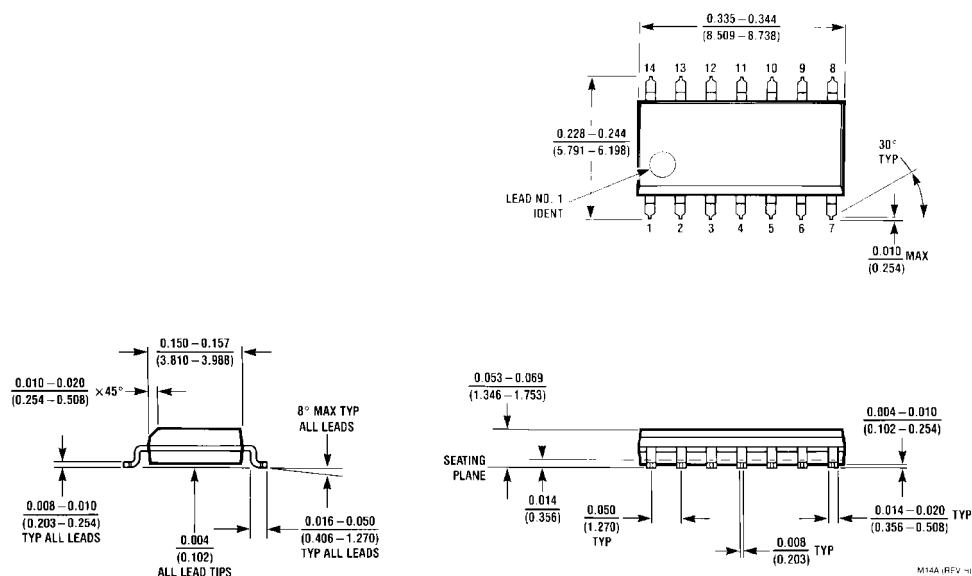
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage 10% V _{CC} 5% V _{CC}	2.5 2.7			V	Min	I _{OH} = –1 mA I _{OH} = –1 mA
V _{OL}	Output LOW Voltage 10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			–0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	–60		–150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		0.5	1.5	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			4.5	mA	Max	V _O = LOW

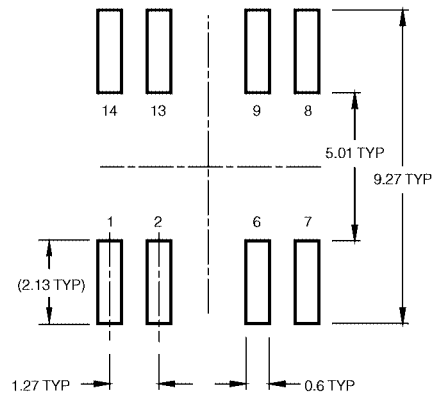
AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	1.0	3.7	5.0	1.0	5.5	ns
t _{PHL}	A _n to \bar{O}	1.5	2.8	5.0	1.5	5.5	

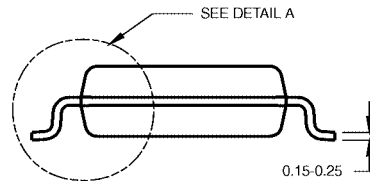
Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A**



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
FLASH, AND TIE BAR EXTRUSIONS.

7° TYP

0°-8° TYP

GAGE PLANE

SEATING PLANE

0.60±0.15

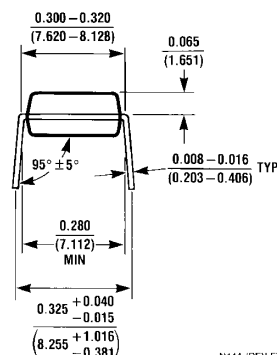
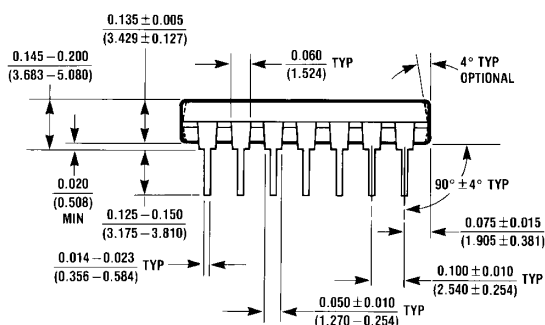
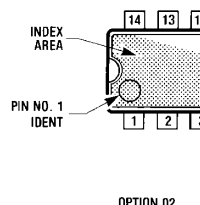
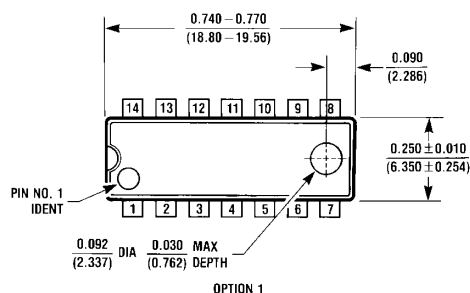
1.25

0.25

DETAIL A

DETAIL A

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

N14A (REV F)

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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