

April 1988 Revised August 2000

74F32

Quad 2-Input OR Gate

General Description

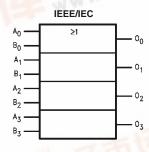
This device contains four independent gates, each of which performs the logic OR function.

Ordering Code:

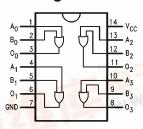
Order Number	Package Number	Package Description						
74F32SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow						
74F32SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide						
74F32MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide						
74F32PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide						

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I _{IH} /I _{IL}		
Fill Names	Description	HIGH/LOW	Output I _{OH} /I _{OL}		
A _n , B _n	Inputs	1.0/1.0	20 μA/-0.6 mA		
O _n	Outputs	50/33.3	−1 mA/20 mA		



Absolute Maximum Ratings(Note 1)

Storage Temperature -65°C to +150°C

 $\label{eq:ambient} \mbox{Ambient Temperature under Bias} \qquad -55\mbox{°C to } +125\mbox{°C} \\ \mbox{Junction Temperature under Bias} \qquad -55\mbox{°C to } +150\mbox{°C} \\ \mbox{To } +150$

 $\begin{array}{ll} {\rm V_{CC}~Pin~Potential~to~Ground~Pin} & & -0.5{\rm V}~to~+7.0{\rm V} \\ {\rm Input~Voltage~(Note~2)} & & -0.5{\rm V}~to~+7.0{\rm V} \\ \end{array}$

Input Current (Note 2) —30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with $V_{CC} = 0V$)

 $\begin{array}{lll} \mbox{Standard Output} & -0.5\mbox{V to V}_{\mbox{CC}} \\ \mbox{3-STATE Output} & -0.5\mbox{V to } +5.5\mbox{V} \end{array}$

Current Applied to Output

Recommended Operating Conditions

Free Air Ambient Temperature $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Supply Voltage +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

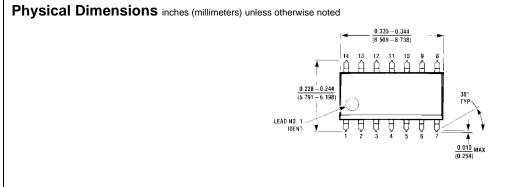
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

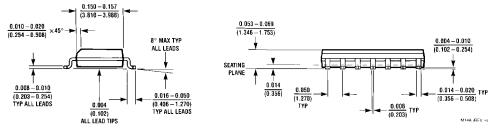
DC Electrical Characteristics

Symbol	Parameter		Min	Тур	Max	Units	V _{cc}	Conditions	
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal	
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal	
V _{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH 10	0% V _{CC}	2.5			V	Min	I _{OH} = -1 mA	
	Voltage	5% V _{CC}	2.7					$I_{OH} = -1 \text{ mA}$	
V _{OL}	Output LOW 10	10% V _{CC}			0.5	V	Min	I _{OL} = 20 mA	
	Voltage				0.5	V	IVIII	I _{OL} = 20 IIIA	
I _{IH}	Input HIGH			F.(5.0	μА	Max	V _{IN} = 2.7V	
	Current				5.0	μΛ			
I _{BVI}	Input HIGH Current				7.0	μΑ	Max	V _{IN} = 7.0V	
	Breakdown Test							VIN = 7.0 V	
I _{CEX}	Output HIGH				50	μА	Max	V _{OUT} = V _{CC}	
	Leakage Current							VOUT - VCC	
V _{ID}	Input Leakage		4.75			٧	0.0	$I_{ID} = 1.9 \mu A$	
	Test							All Other Pins Grounded	
I _{OD}	Output Leakage				3.75	μА	0.0	V _{IOD} = 150 mV	
	Circuit Current							All Other Pins Grounded	
I _{IL}	Input LOW Current				-0.6	mA	Max	V _{IN} = 0.5V	
Ios	Output Short-Circuit Current		-60		-150	mA	Max	V _{OUT} = 0V	
I _{CCH}	Power Supply Current			6.1	9.2	mA	Max	V _O = HIGH	
I _{CCL}	Power Supply Current			10.3	15.5	mA	Max	$V_O = LOW$	

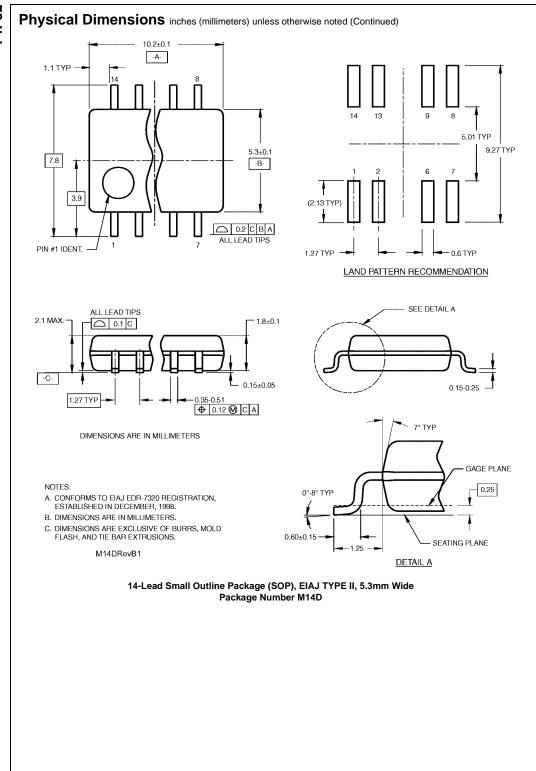
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_{A} = -55^{\circ}\text{C to } +125^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_{L} = 50 \text{ pF}$		$T_A = 0$ °C to $+70$ °C $V_{CC} = +5.0V$ $C_L = 50$ pF		Units	
		Min	Тур	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	3.0	4.2	5.6	3.0	7.5	3.0	6.6	ns	
t _{PHL}	A_n , B_n to O_n	3.0	4.0	5.3	2.5	7.5	3.0	6.3	115	

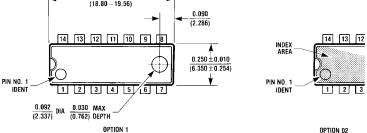


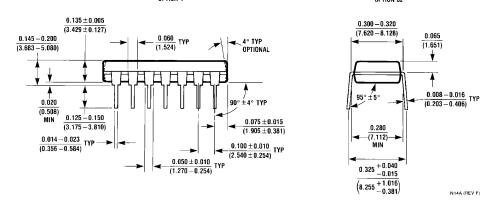


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.43 TYP -A-7.72 4.16 6.4 -B-3.2 0.2 C B A 0.65 ALL LEAD TIPS PIN #1 IDENT. LAND PATTERN RECOMMENDATION SEE DETAIL A ALL LEAD TIPS 0.90 +0.15 1.2 MAX Г 0.09-0.20 -C-L_{0.10±0.05} 0.19 - 0.30 ◆ 0.13 M A B C C 12.00° TOP & BOTTOM R0.09 MIN-GAGE PLANE NOTES: A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. 0.25 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND 0.6 ±0.1 SEATING PLANE TIE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. -1.00 R0.09 MIN MTC14RevC3 DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14





14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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