



PDSP16116/A/MC

16 by 16 Bit Complex Multiplier

The PDSP16116A will multiply two complex (16 + 16) bit words every 50ns and can be configured to output the complete complex (32 + 32) bit result within a single cycle. The data format is fractional two's complement.

The PDSP16116/A contains four 16 x 16 Array Multipliers, two 32 bit Adder/Subtractors and all the control logic required to support Block Floating Point Arithmetic as used in FFT applications. In combination with a PDSP16318, the PDSP16116A forms a two chip 10MHz Complex Multiplier Accumulator with 20 bit accumulator registers and output shifters. The PDSP16116 in combination with two PDSP16318s and two PDSP1601s forms a complete 10MHz Radix 2 DIT FFT Butterfly solution which fully supports Block Floating Point Arithmetic. The PDSP16116/A has an extremely high throughput that is suited to recursive algorithms as all calculations are performed with a single pipeline delay (two cycle fall-through).

FEATURES

- Complex Number (16 + 16) X (16 + 16) Multiplication
- Full 32 bit Result
- 20MHz Clock Rate
- Block Floating Point FFT Butterfly Support
- -1 times -1 Trap
- Two's Complement Fractional Arithmetic
- TTL Compatible I/O
- Complex Conjugation
- 2 Cycle Fall Through
- 144 pin PGA or QFP packages

APPLICATION

- Fast Fourier Transforms
- Digital Filtering
- Radar and Sonar Processing
- Instrumentation
- Image Processing

ASSOCIATED PRODUCTS

- PDSP16318/A Complex Accumulator
- PDSP16112/A (16 + 16) X (12 + 12) Complex Multiplier
- PDSP16330/A Pythagoras Processor
- PDSP1601/A ALU and Barrel Shifter
- PDSP16350 Precision Digital Modulator
- PDSP16256 Programmable FIR Filter
- PDSP16510 Single Chip FFT Processor

DS3858

ISSUE 3.0

June 2000

Ordering Information

| | | |
|---------------------------|-------|--------------------------------|
| PDSP16116 MC GC1R | 10MHz | MIL-883 screened - ceramic QFP |
| PDSP16116 MC AC1R | 10MHz | MIL-883 screened - PGA package |
| PDSP16116A MC GC1R | 20MHz | MIL-883 screened - ceramic QFP |
| PDSP16116A MC AC1R | 20MHz | MIL-883 screened - PGA package |

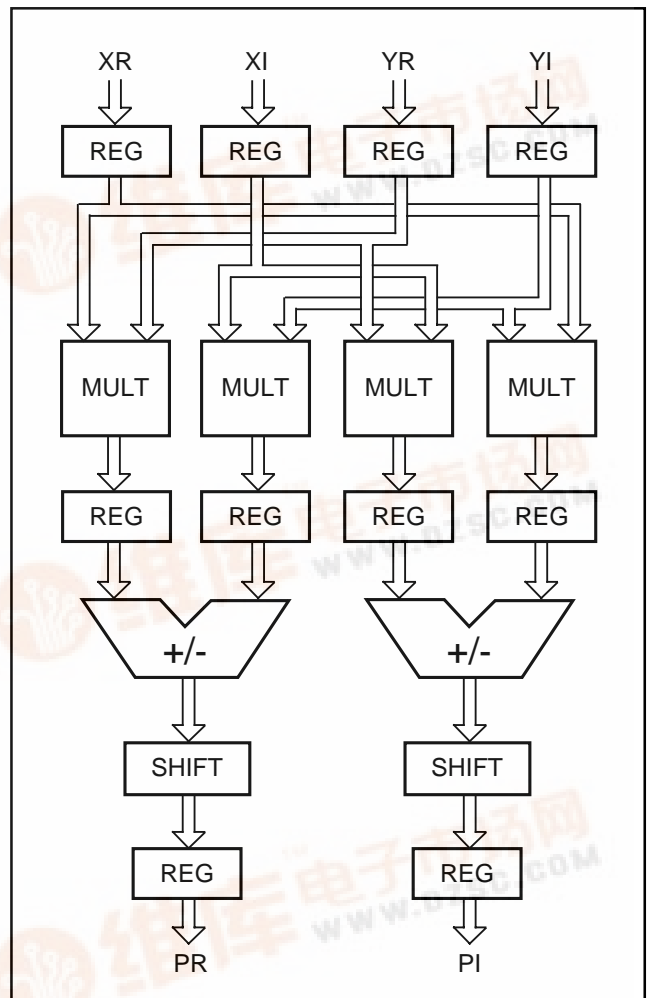


Fig.1 Simplified Block Diagram

CHANGE NOTIFICATION

The change notification requirements of MIL-M-38510 will be implemented on this device type. Known customers will be notified of any changes since last buy when ordering further parts if significant changes have been made.

| | | | | |
|------|-----------|----------|----------|---|
| Rev | A | B | C | D |
| Date | JULY 1993 | OCT 1998 | JUN 2000 | 1 |



PDSP16116/A/MC

The PDSP16116 has a number of features tailored for System applications.

-1 x -1 Trap

In multiply operations utilising Twos Complement Fractional notation, the -1 x -1 operation forms an invalid result as +1 is not representable in the fractional number range. The PDSP16116/A eliminates this problem by trapping the -1 x -1 operation and forcing the Multiplier result to become the most positive representable number.

Complex Conjugation

Many algorithms utilising complex arithmetic require conjugation of complex data stream. This operation has

traditionally required an additional ALU to multiply the imaginary component by -1. The PDSP16116 eliminates the requirement for the extra ALU by offering on chip complex conjugation of either of the two incoming complex data words with no loss in throughput.

Easy Interfacing

As with all PDSP family members the PDSP16116 has registered I/O for data and control. Data inputs have independent clock enables and data outputs have independent three state output enables.

| Signal | Type | Description | Normal mode Configuration |
|-------------------------------------|--------|---|---------------------------|
| XR15:0 | INPUT | 16 bit input for real x data | |
| XI15:0 | INPUT | 16 bit input for imag x data | |
| YR15:0 | INPUT | 16 bit input for real y data | |
| YI15:0 | INPUT | 16 bit input for imag y data | |
| PR15:0 | OUTPUT | 16 bit output for real p data | |
| PI15:0 | OUTPUT | 16 bit output for img p data | |
| CLK | INPUT | Clock, new data is loaded on rising edge of CLK | |
| $\overline{CE}X$ | INPUT | Clock, enable X-port input register | |
| $\overline{CE}Y$ | INPUT | Clock, enable Y-port input register | |
| CONX | INPUT | Conjugate X data | |
| CONY | INPUT | Conjugate Y data | |
| ROUND | INPUT | Rounds the real & imag results | |
| MBFP | INPUT | Mode select (BFP/Normal) | Tie Low |
| \overline{SOBFP} | INPUT | Start of BFP operations ** | Tie Low |
| \overline{EOPSS} | INPUT | End of pass ** | Tie Low |
| AR15:13 | INPUT | 3 MSB's from real part of A-word ** | Tie Low |
| AI15:13 | INPUT | 3 MSB's from imag part of A-word ** | Tie Low |
| WTA1:0 | INPUT | Word tag from A-word | Tie Low |
| WTB1:0 | INPUT | Word tag from B-word / shift control * | Tie Low |
| WTOUT1:0 | OUTPUT | Word tag output ** | |
| SFTA1:0 | OUTPUT | Shift control for A-word / overflow flag * | |
| SFTR2:0 | OUTPUT | Shift control for accumulator resul ** | |
| GWR4:0 | OUTPUT | Global weighting register contents ** | |
| OSEL1:0 | INPUT | Selects the desired output configuration | |
| \overline{OER} , \overline{OEI} | INPUT | Output enables | |
| VDD | POWER | +5V Supply All supply pins | |
| GND | POWER | 0V Supply must be connected | |

* Indicates pin performs different functions in BFP / Normal modes.

** Indicates pin is used only in BFP mode

Table.1 Signal Descriptions

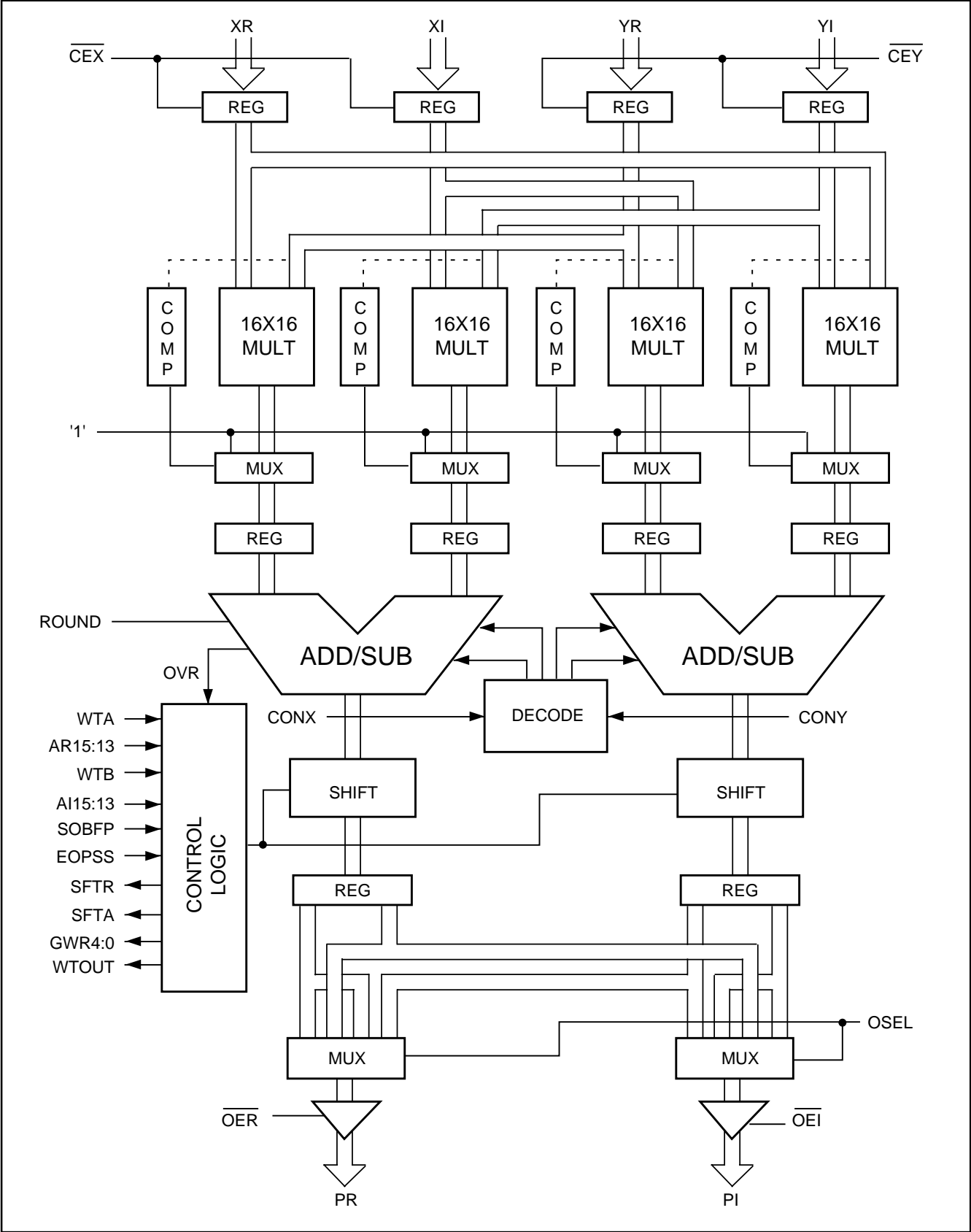
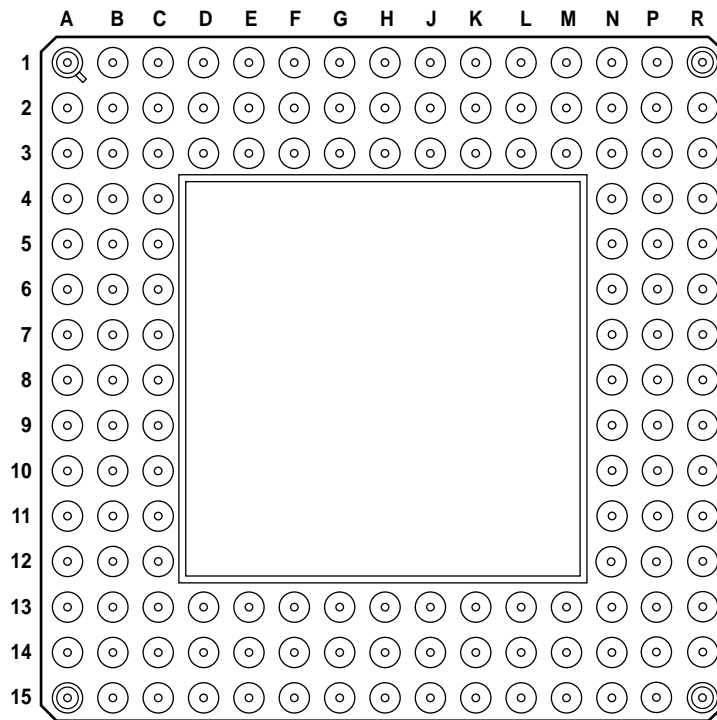


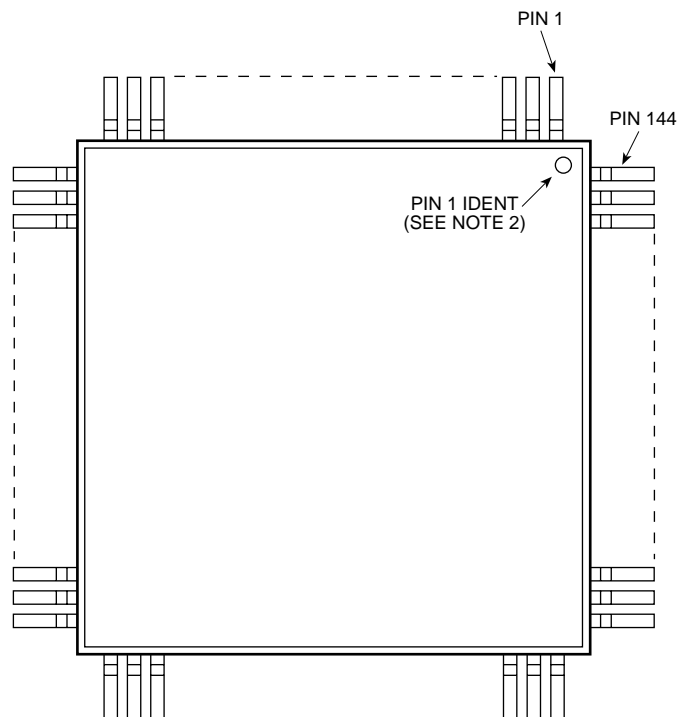
Figure 2 - Block Diagram

PDSP16116/A/MC



AC144 (POWER)

Pin connections for 144 I/O power pin grid array package (bottom view)



GC144

Pin connections for 144 I/O ceramic quad flatpack (top view)

Figure 3 Pin connection diagrams (not to scale).

| GC | AC | Signal | GC | AC | Signal | GC | AC | Signal | GC | AC | Signal |
|----|----|-------------------------|----|-----|-------------------------|-----|-----|---------------------------|-----|-----|-----------------|
| 1 | D3 | PI14 | 37 | N4 | XI1 | 73 | P2 | GND | 109 | N14 | V _{DD} |
| 2 | C2 | PI15 | 38 | P3 | XI2 | 74 | R1 | V _{DD} | 110 | M13 | GND |
| 3 | B1 | WTOUT1 | 39 | R2 | XI3 | 75 | P15 | YR12 | 111 | A14 | PR13 |
| 4 | D2 | WTOUT0 | 40 | P4 | XI4 | 76 | M14 | YR11 | 112 | B12 | PR12 |
| 5 | E3 | SFTR0 | 41 | N5 | XI5 | 77 | L13 | YR10 | 113 | C11 | PR11 |
| 6 | C1 | SFTR1 | 42 | R3 | XI6 | 78 | N15 | YR9 | 114 | A13 | PR10 |
| 7 | E2 | SFTR2 | 43 | P5 | XI7 | 79 | L14 | YR8 | 115 | B11 | PR9 |
| 8 | D1 | $\overline{\text{OEI}}$ | 44 | R4 | XI8 | 80 | M15 | YR7 | 116 | A12 | PR8 |
| 9 | F2 | CONX | 45 | N6 | XI9 | 81 | K13 | YR6 | 117 | C10 | PR7 |
| 10 | F3 | CONY | 46 | P6 | XI10 | 82 | K14 | YR5 | 118 | B10 | PR6 |
| 11 | E1 | ROUND | 47 | R5 | XI11 | 83 | L15 | YR4 | 119 | A11 | PR5 |
| 12 | G2 | AI13 | 48 | P7 | XI12 | 84 | J14 | YR3 | 120 | B13 | GND |
| 13 | G3 | AI14 | 49 | N7 | XI13 | 85 | J13 | YR2 | 121 | C12 | V _{DD} |
| 14 | F1 | AI15 | 50 | R6 | XI14 | 86 | K15 | YR1 | 122 | A10 | PR4 |
| 15 | G1 | AR13 | 51 | R7 | XI15 | 87 | J15 | YR0 | 123 | A9 | PR3 |
| 16 | H2 | AR14 | 52 | P8 | $\overline{\text{CEY}}$ | 88 | H14 | $\overline{\text{EOPSS}}$ | 124 | B8 | PR2 |
| 17 | H1 | AR15 | 53 | R8 | $\overline{\text{CEX}}$ | 89 | H15 | V _{DD} | 125 | A8 | PR1 |
| 18 | H3 | YI15 | 54 | N8 | XR15 | 90 | H13 | $\overline{\text{SOBFP}}$ | 126 | C8 | PR0 |
| 19 | J3 | YI14 | 55 | N9 | XR14 | 91 | G13 | WTB1 | 127 | C7 | PI0 |
| 20 | J1 | YI13 | 56 | R9 | XR13 | 92 | G15 | WTB0 | 128 | A7 | PI1 |
| 21 | K1 | YI12 | 57 | R10 | XR12 | 93 | F15 | WTA1 | 129 | A6 | PI2 |
| 22 | J2 | YI11 | 58 | P9 | XR11 | 94 | G14 | WTA0 | 130 | B7 | PI3 |
| 23 | K2 | YI10 | 59 | P10 | XR10 | 95 | F14 | MBFP | 131 | B6 | PI4 |
| 24 | K3 | YI9 | 60 | N10 | XR9 | 96 | F13 | CLK | 132 | C6 | V _{DD} |
| 25 | L1 | YI8 | 61 | R11 | XR8 | 97 | E15 | OSEL1 | 133 | A5 | PI5 |
| 26 | L2 | YI7 | 62 | P11 | XR7 | 98 | E14 | OSEL0 | 134 | B5 | GND |
| 27 | M1 | YI6 | 63 | R12 | XR6 | 99 | D15 | $\overline{\text{OER}}$ | 135 | A4 | PI6 |
| 28 | N1 | YI5 | 64 | R13 | XR5 | 100 | C15 | SFTA0 | 136 | A3 | PI7 |
| 29 | M2 | YI4 | 65 | P12 | XR4 | 101 | D14 | SFTA1 | 137 | B4 | PI8 |
| 30 | L3 | YI3 | 66 | N11 | XR3 | 102 | E13 | GWR0 | 138 | C5 | PI9 |
| 31 | N2 | YI2 | 67 | P13 | XR2 | 103 | C14 | GWR1 | 139 | B3 | PI10 |
| 32 | P1 | YI1 | 68 | R14 | XR1 | 104 | B15 | GWR2 | 140 | A2 | PI11 |
| 33 | M3 | YI0 | 69 | N12 | XR0 | 105 | D13 | GWR3 | 141 | C4 | PI12 |
| 34 | N3 | XI0 | 70 | N13 | YR15 | 106 | C13 | GWR4 | 142 | C3 | PI13 |
| 35 | B2 | GND | 71 | P14 | YR14 | 107 | B14 | PR15 | 143 | B9 | GND |
| 36 | A1 | V _{DD} | 72 | R15 | YR13 | 108 | A15 | PR14 | 144 | C9 | V _{DD} |

NOTE. All GND and V_{DD} pins must be used

Figure 3A - Pin connections for AC144 (Power) and GC144 packages

PDSP16116/A/MC

NORMAL MODE OPERATION

When the MBFP mode select input is held low the 'Normal' mode of operation is selected. This mode supports all Complex Multiply operations that do not require Block Floating Point arithmetic.

Multiplier Stage

Complex two's complement fractional data is loaded into the X and Y input registers via the X and Y Ports on the rising edge of CLK. The Real and Imaginary components of the fractional data are each assumed to have the following format

| | | | | | | | | | | | | | | | | |
|------------|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|------------------|
| BIT NUMBER | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WEIGHTING | S | 2 ⁻¹ | 2 ⁻² | 2 ⁻³ | 2 ⁻⁴ | 2 ⁻⁵ | 2 ⁻⁶ | 2 ⁻⁷ | 2 ⁻⁸ | 2 ⁻⁹ | 2 ⁻¹⁰ | 2 ⁻¹¹ | 2 ⁻¹² | 2 ⁻¹³ | 2 ⁻¹⁴ | 2 ⁻¹⁵ |

Where S = sign bit which has an effective weighting -2⁰

The value of the 16 bit two's complement word is

$$\text{Value} = (-1 \times S) + (\text{bit}14 \times 2^{-1}) + (\text{bit}13 \times 2^{-2}) + (\text{bit}12 \times 2^{-3}) \dots$$

The X & Y port registers are individually enabled by the $\overline{\text{CEX}}$ & $\overline{\text{CEY}}$ signals respectively. If the registers are required to be permanently enabled, then these signals may be tied to ground. On each clock cycle the contents of the input registers are passed to the four multipliers to start a new Complex Multiply operation. Each Complex Multiply operation requires four partial products (Xr x Yr), (Xr x Yi), (Xi x Yr), (Xi x Yi), all of which are calculated in parallel by the four 16 x 16 Multipliers. Only one clock cycle is required to complete the multiply stage before the Multiplier results are loaded into the Multiplier output registers for passing on to the Adder/Subtractors in the next cycle. Each multiplier produces a 31 bit result with the duplicate sign bit eliminated. The format of the output data from the Multipliers is

| | | | | | | | | | | | | | | | | |
|------------|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| BIT NUMBER | 30 | 29 | 28 | 27 | 26 | 25 | 24 | ... | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WEIGHTING | S | 2 ⁻¹ | 2 ⁻² | 2 ⁻³ | 2 ⁻⁴ | 2 ⁻⁵ | 2 ⁻⁶ | ... | 2 ⁻²³ | 2 ⁻²⁴ | 2 ⁻²⁵ | 2 ⁻²⁶ | 2 ⁻²⁷ | 2 ⁻²⁸ | 2 ⁻²⁹ | 2 ⁻³⁰ |

The effective weighting of the sign bit is -2⁰

Result Correction

Due to the nature of the fraction twos complement representation it is possible to represent -1 exactly but not 1. With conventional multipliers this causes a problem when -1 is multiplied by -1 as the multiplier produces an incorrect result. The PDSP16116 includes a trap to ensure that the most positive number (value = 1.2⁻³⁰), (hex = 7FFFFFFF) is substituted for the incorrect result. The multiplier result is therefore always a (correct) fractional value.

Complex Conjugation

Either the X or Y input data may be complex conjugated by asserting the CONX or CONY signals respectively. Asserting either of these signals has the effect of inverting (multiplying by -1) the imaginary component of the respective input. Table 3 shows the effect of CONX and CONY on the X and Y inputs.

| FUNCTION | OPERATION | CONX | CONY |
|------------|-----------------|------|------|
| X x Y | (XR+XI)x(YR+YI) | low | low |
| X x Conj Y | (XR+XI)x(YR-YI) | high | low |
| Conj X x Y | (XR-XI)x(YR+YI) | low | high |
| Invalid | Invalid | high | high |

Table 3 Conjugate Functions

Adder / Subtractor Stage

The 31 bit Real and Imaginary results from the Multipliers are passed to two 32 bit Adder/Subtractors. The Adder calculates the imaginary result ((Xr x Yi) + (Xi x Yr)) and the Subtractor calculates the Real result ((Xr x Yr) - (Xi x Yi)). Each Adder/Subtractor produces a 32 bit result with the following format.

| | | | | | | | | | | | | | | | | |
|------------|----|----------------|-----------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | ... | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WEIGHTING | S | 2 ⁰ | 2 ⁻¹ | 2 ⁻² | 2 ⁻³ | 2 ⁻⁴ | ... | 2 ⁻²² | 2 ⁻²³ | 2 ⁻²⁴ | 2 ⁻²⁵ | 2 ⁻²⁶ | 2 ⁻²⁷ | 2 ⁻²⁸ | 2 ⁻²⁹ | 2 ⁻³⁰ |

The effective weighting of the sign bit is -2¹

Rounding

The ROUND control when asserted rounds the most significant 16 bits of the full 32 bit result from the Adder/Subtractor. If the ROUND signal is active (High), then bit 16 is set to a one, rounding the most significant 16 bits of the Adder/Subtractor result. (The least significant 16 bits are unaffected). Inserting a one ensures that the rounding error is never greater than 1LSB, and that no DC bias is introduced as a result of the rounding processes.

The format of the Rounded result is;

| | | | | | | | | | | | | | | | | |
|------------|----|----------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|------------------|------------------|------------------|-----|------------------|------------------|------------------|
| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | ... | 18 | 17 | 16 | 15 | 14 | 13 | ... | 2 | 1 | 0 |
| WEIGHTING | S | 2 ⁰ | 2 ⁻¹ | 2 ⁻² | 2 ⁻³ | ... | 2 ⁻¹² | 2 ⁻¹³ | 2 ⁻¹⁴ | 2 ⁻¹⁵ | 2 ⁻¹⁶ | 2 ⁻¹⁷ | ... | 2 ⁻²⁸ | 2 ⁻²⁹ | 2 ⁻³⁰ |

← ROUNDED VALUE →
← LBSs →

The effective weighting of the sign is -2¹

Shifter

Each of the two Adder/Subtractors are followed by Shifters controlled via the WTB control input. These shifters can each apply four different shifts, however the same shift is applied to both real and imaginary components. The four shift options are:

- i) WTB1:0 = 11 Shift complex product one place to the left giving a shifter output format:

| | | | | | | | | | | | | | | | | |
|------------|----|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| BIT NUMBER | 31 | 30 | 29 | 28 | 27 | 26 | 25 | ... | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WEIGHTING | S | 2 ⁻¹ | 2 ⁻² | 2 ⁻³ | 2 ⁻⁴ | 2 ⁻⁵ | 2 ⁻⁶ | ... | 2 ⁻²⁴ | 2 ⁻²⁵ | 2 ⁻²⁶ | 2 ⁻²⁷ | 2 ⁻²⁸ | 2 ⁻²⁹ | 2 ⁻³⁰ | 2 ⁻³¹ |

The effective weighting of the sign bit is -2⁰

PDSP16116/A/MC

Part No: PDSP11616/A/MC 16 By16 Bit Complex Multiplier
 Package Type: AC144

VDD max = +5.5V = V1
 N/C = not connected

| Pin No. | Con. | Pin No. | Con. | Pin No. | Con. | Pin No. | Con. |
|---------|---------|---------|---------|---------|---------|---------|---------|
| A1 | V1 | E1 | 0V 100Ω | J1 | V1 100Ω | N1 | V1 100Ω |
| A2 | N/C | E2 | N/C | J2 | V1 100Ω | N2 | V1 100Ω |
| A3 | N/C | E3 | N/C | J3 | V1 100Ω | N3 | 0V 100Ω |
| A4 | N/C | E4 | N/C | J4 | N/C | N4 | 0V 100Ω |
| A5 | N/C | E5 | N/C | J5 | N/C | N5 | 0V 100Ω |
| A6 | N/C | E6 | N/C | J6 | N/C | N6 | 0V 100Ω |
| A7 | N/C | E7 | N/C | J7 | N/C | N7 | 0V 100Ω |
| A8 | N/C | E8 | N/C | J8 | N/C | N8 | V1 100Ω |
| A9 | N/C | E9 | N/C | J9 | N/C | N9 | V1 100Ω |
| A10 | N/C | E10 | N/C | J10 | N/C | N10 | V1 100Ω |
| A11 | N/C | E11 | N/C | J11 | N/C | N11 | V1 100Ω |
| A12 | N/C | E12 | N/C | J12 | N/C | N12 | V1 100Ω |
| A13 | N/C | E13 | N/C | J13 | 0V 100Ω | N13 | 0V 100Ω |
| A14 | N/C | E14 | V1 100Ω | J14 | 0V 100Ω | N14 | V1 |
| A15 | N/C | E15 | V1 100Ω | J15 | 0V 100Ω | N15 | 0V 100Ω |
| B1 | N/C | F1 | 0V 100Ω | K1 | V1 100Ω | P1 | V1 100Ω |
| B2 | 0V | F2 | 0V 100Ω | K2 | V1 100Ω | P2 | 0V |
| B3 | N/C | F3 | V1 100Ω | K3 | V1 100Ω | P3 | 0V 100Ω |
| B4 | N/C | F4 | N/C | K4 | N/C | P4 | 0V 100Ω |
| B5 | 0V | F5 | N/C | K5 | N/C | P5 | 0V 100Ω |
| B6 | N/C | F6 | N/C | K6 | N/C | P6 | 0V 100Ω |
| B7 | N/C | F7 | N/C | K7 | N/C | P7 | 0V 100Ω |
| B8 | N/C | F8 | N/C | K8 | N/C | P8 | V1 100Ω |
| B9 | 0V | F9 | N/C | K9 | N/C | P9 | V1 100Ω |
| B10 | N/C | F10 | N/C | K10 | N/C | P10 | V1 100Ω |
| B11 | N/C | F11 | N/C | K11 | N/C | P11 | V1 100Ω |
| B12 | N/C | F12 | N/C | K12 | N/C | P12 | V1 100Ω |
| B13 | 0V | F13 | 0V 100Ω | K13 | 0V 100Ω | P13 | V1 100Ω |
| B14 | N/C | F14 | 0V 100Ω | K14 | 0V 100Ω | P14 | 0V 100Ω |
| B15 | N/C | F15 | 0V 100Ω | K15 | 0V 100Ω | P15 | 0V 100Ω |
| C1 | N/C | G1 | 0V 100Ω | L1 | V1 100Ω | R1 | V1 |
| C2 | N/C | G2 | 0V 100Ω | L2 | V1 100Ω | R2 | 0V 100Ω |
| C3 | N/C | G3 | 0V 100Ω | L3 | V1 100Ω | R3 | 0V 100Ω |
| C4 | N/C | G4 | N/C | L4 | N/C | R4 | 0V 100Ω |
| C5 | N/C | G5 | N/C | L5 | N/C | R5 | 0V 100Ω |
| C6 | V1 | G6 | N/C | L6 | N/C | R6 | 0V 100Ω |
| C7 | N/C | G7 | N/C | L7 | N/C | R7 | 0V 100Ω |
| C8 | N/C | G8 | N/C | L8 | N/C | R8 | V1 100Ω |
| C9 | V1 | G9 | N/C | L9 | N/C | R9 | V1 100Ω |
| C10 | N/C | G10 | N/C | L10 | N/C | R10 | V1 100Ω |
| C11 | N/C | G11 | N/C | L11 | N/C | R11 | V1 100Ω |
| C12 | V1 | G12 | N/C | L12 | N/C | R12 | V1 100Ω |
| C13 | N/C | G13 | V1 100Ω | L13 | 0V 100Ω | R13 | V1 100Ω |
| C14 | N/C | G14 | 0V 100Ω | L14 | 0V 100Ω | R14 | V1 100Ω |
| C15 | N/C | G15 | V1 100Ω | L15 | 0V 100Ω | R15 | 0V 100Ω |
| D1 | V1 100Ω | H1 | 0V 100Ω | M1 | V1 100Ω | | |
| D2 | N/C | H2 | 0V 100Ω | M2 | V1 100Ω | | |
| D3 | N/C | H3 | V1 100Ω | M3 | V1 100Ω | | |
| D4 | N/C | H4 | N/C | M4 | N/C | | |
| D5 | N/C | H5 | N/C | M5 | N/C | | |
| D6 | N/C | H6 | N/C | M6 | N/C | | |
| D7 | N/C | H7 | N/C | M7 | N/C | | |
| D8 | N/C | H8 | N/C | M8 | N/C | | |
| D9 | N/C | H9 | N/C | M9 | N/C | | |
| D10 | N/C | H10 | N/C | M10 | N/C | | |
| D11 | N/C | H11 | N/C | M11 | N/C | | |
| D12 | N/C | H12 | N/C | M12 | N/C | | |
| D13 | N/C | H13 | 0V 100Ω | M13 | 0V | | |
| D14 | N/C | H14 | 0V 100Ω | M14 | 0V 100Ω | | |
| D15 | V1 100Ω | H15 | V1 | M15 | 0V 100Ω | | |

Figure 4(a) - Life Test/Burn-in connections
 NOTE: PDA is 5% and based on groups 1 and 7

PDSP16116/A/MC

Part No: PDSP16116/A/MC 16 By 16 Bit Complex Multiplier
 Package Type: GC144

| Pin No. | Con. | Pin No. | Con. | Pin No. | Con. | Pin No. | Con. |
|---------|------|---------|------|---------|------|---------|------|
| 1 | N/C | 37 | 0V | 73 | 0V | 109 | N/C |
| 2 | N/C | 38 | 0V | 74 | V1 | 110 | N/C |
| 3 | N/C | 39 | 0V | 75 | 0V | 111 | N/C |
| 4 | N/C | 40 | 0V | 76 | 0V | 112 | N/C |
| 5 | N/C | 41 | 0V | 77 | 0V | 113 | N/C |
| 6 | N/C | 42 | 0V | 78 | 0V | 114 | N/C |
| 7 | N/C | 43 | 0V | 79 | 0V | 115 | N/C |
| 8 | V1 | 44 | 0V | 80 | 0V | 116 | N/C |
| 9 | 0V | 45 | 0V | 81 | 0V | 117 | N/C |
| 10 | 0V | 46 | 0V | 82 | 0V | 118 | N/C |
| 11 | 0V | 47 | 0V | 83 | 0V | 119 | N/C |
| 12 | 0V | 48 | 0V | 84 | 0V | 120 | 0V |
| 13 | 0V | 49 | 0V | 85 | 0V | 121 | V1 |
| 14 | 0V | 50 | 0V | 86 | 0V | 122 | N/C |
| 15 | 0V | 51 | 0V | 87 | 0V | 123 | N/C |
| 16 | 0V | 52 | V1 | 88 | 0V | 124 | N/C |
| 17 | 0V | 53 | V1 | 89 | V1 | 125 | N/C |
| 18 | V1 | 54 | V1 | 90 | 0V | 126 | N/C |
| 19 | V1 | 55 | V1 | 91 | V1 | 127 | N/C |
| 20 | V1 | 56 | V1 | 92 | V1 | 128 | N/C |
| 21 | V1 | 57 | V1 | 93 | 0V | 129 | N/C |
| 22 | V1 | 58 | V1 | 94 | 0V | 130 | N/C |
| 23 | V1 | 59 | V1 | 95 | 0V | 131 | N/C |
| 24 | V1 | 60 | V1 | 96 | V1 | 132 | V1 |
| 25 | V1 | 61 | V1 | 97 | 0V | 133 | N/C |
| 26 | V1 | 62 | V1 | 98 | 0V | 134 | 0V |
| 27 | V1 | 63 | V1 | 99 | V1 | 135 | N/C |
| 28 | V1 | 64 | V1 | 100 | N/C | 136 | N/C |
| 29 | V1 | 65 | V1 | 101 | N/C | 137 | N/C |
| 30 | V1 | 66 | V1 | 102 | N/C | 138 | N/C |
| 31 | V1 | 67 | V1 | 103 | N/C | 139 | N/C |
| 32 | V1 | 68 | V1 | 104 | N/C | 140 | N/C |
| 33 | V1 | 69 | V1 | 105 | N/C | 141 | N/C |
| 34 | 0V | 70 | 0V | 106 | N/C | 142 | N/C |
| 35 | 0V | 71 | 0V | 107 | N/C | 143 | 0V |
| 36 | V1 | 72 | 0V | 108 | N/C | 144 | V1 |

VDD max = +5.0V = V1

N/C = not connected

Figure 4(b) Life Test/Burn-in connections
 NOTE: PDA is 5% and based on groups 1 and 7

ii) WTB1:0 = 00 No shift applied giving a shifter output format:

| | | | | | | | | | | | | | | | |
|------------|----|-------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Number | 31 | 30 | 29 | 28 | 27 | 26 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Weighting | S | 2^0 | 2^{-1} | 2^{-2} | 2^{-3} | 2^{-4} | 2^{-22} | 2^{-23} | 2^{-24} | 2^{-25} | 2^{-26} | 2^{-27} | 2^{-28} | 2^{-29} | 2^{-30} |

The effective weighting of the shift bit is -2^1 .

iii) WTB1:0 = 01 Shift complex product one place to the right giving a shifter output format:

| | | | | | | | | | | | | | | | |
|------------|----|-------|-------|----------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Weighting | S | 2^1 | 2^0 | 2^{-1} | 2^{-2} | 2^{-3} | 2^{-4} | 2^{-5} | 2^{-23} | 2^{-24} | 2^{-25} | 2^{-26} | 2^{-27} | 2^{-28} | 2^{-29} |

The effective weighting of the sign bit is -2^2 .

iv) WTB1:0 = 10 Shift complex product two places to the right giving a shifter output format:

| | | | | | | | | | | | | | | | |
|------------|----|-------|-------|-------|----------|----------|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit Number | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Weighting | S | 2^2 | 2^1 | 2^0 | 2^{-1} | 2^{-2} | 2^{-3} | 2^{-4} | 2^{-22} | 2^{-23} | 2^{-24} | 2^{-25} | 2^{-26} | 2^{-27} | 2^{-28} |

The effective weighting of the sign bit is -2^3 .

Overflow

If the left shift option is selected and the Adder/Subtractor contain a 32 bit word, then an invalid result will be passed to the output. An invalid output arising from this combination of events will be flagged by the SFTA0 flag output. The SFTA0 Flag will go high if either the real or imaginary result is invalid.

Output Select

The output from the Shifters is passed to the Output Select Mux, which is controlled via the OSEL inputs. These inputs are not registered and hence allow the output combination to be changed within each cycle. The full complex 64 bit result from the multiplier may therefore be output within a single cycle. The OSEL control selects four different output combinations as as summarised in Table 4.

| | | | |
|-------|-------|-----|-----|
| OSEL1 | OSEL0 | PR | PI |
| 0 | 0 | MSR | MSI |
| 0 | 1 | LSR | LSI |
| 1 | 0 | MSR | LSR |
| 1 | 1 | MSI | LSI |

Table 3 - Output Selection

(Where MSR and LSR are the most and least significant 16 bit words of the Real Shifter output, MSI and LSI are the most and least significant 16 bit words of the imaginary Shifter output).

The output select options allow two different modes for extracting the full 32 bit result from the PDSP16116. The first mode treats the two 16 bit outputs as real and imaginary ports allowing the real and imaginary results to be output in two halves on the real and imaginary output ports. The second mode treats the two 16 bit outputs as one 32 bit output and allows the real and imaginary results to be output as 32 bit words.

PIN DESCRIPTIONS

XR, XI, YR, YI

Data inputs 16 bits: Data is loaded into the input registers from these ports on the rising edge of CLK. The data format is Twos Complement Fractional, where the MSB (sign bit) is bit 15. In normal mode the weighting of the MSB is -2^0 ie -1.

PR, PI

Data outputs 16 bits: Data is clocked into the output registers and passed to the PR and PI outputs on the rising edge of CLK. The data format is Twos Complement Fractional. The field of the internal result selected for output via PR and PI is controlled by signals OSEL1:0 (see Table 4).

CLK

Common Clock to all internal register.

CEX, CEY

Clock enables for X and Y input ports: When low these inputs enable the CLK signal to the X or Y input registers allowing new data to be clocked into the Multiplier.

CONX, CONY

If either of these inputs are high on the rising edge of CLK, then the data in the associated input has its imaginary component inverted (multiplied by -1), see Table 3. CONX and CONY affect data input on the same clock rising edge.

ROUND

The ROUND control is used to round the most significant 16 bits of the Adder/Subtractor result prior to being passed to the output register. The rounding operation takes place one cycle after the ROUND input is taken high. The ROUND input is not latched and is intended to be tied high or low depending upon the application.

MBFP

Mode select: When high, Block Floating Point (BFP) mode is selected. This allows the device to maintain the dynamic range of the data using a series of word tags. This is especially useful in FFT applications. When low, the chip operates in normal mode for more general applications. This pin is intended to be tied high or low, depending on application.

PDSP16116/A/MC

$\overline{\text{SOBFP}}$ (BFP MODE ONLY)

Start of BFP: This input should be held low for the first cycle of the first pass of the BFP calculations (see Fig.7). It serves to reset the internal registers associated with BFP control. When operating in normal mode this input should be tied low.

$\overline{\text{EOPSS}}$ (BFP MODE ONLY)

End of pass: This input should be held low for the last cycle of each pass and for the lay time between passes. It instructs the control logic to update the value of the global weighting register and prepare the BFP circuitry for the next pass. When operating in normal mode this input should be tied low.

AR15:13 (BFP MODE ONLY)

Three Msbs of the real part of the A-word : These are used in the FFT butterfly application to determine the magnitude of the real part of the A-word and, hence, to determine if there will be any change of word growth in the PDSP16318 Complex Accumulator. When operating in normal mode, these inputs are not used and may be tied low.

AI15:13 (BFP MODE ONLY)

Three Msbs of the imaginary part of the A-word : used in the same fashion as AR.

SFTR2:0 (BFP MODE ONLY)

Accumulator result shift control. These pins should be linked directly to the S2:0 pins on the PDSP16318 Complex Accumulator. They control the accumulator's barrel shifter (see Table 5). The purpose of this shift is to minimise sign extension in the multiplier or accumulator ALU's. When operating in normal mode, these output are superfluous.

| SFTR2:0 | FUNCTION |
|---------|--------------------|
| 0 0 0 | Reserved |
| 0 0 1 | Reserved |
| 0 1 0 | Reserved |
| 0 1 1 | Shift right by one |
| 1 0 0 | No shift |
| 1 0 1 | Shift left by one |
| 1 1 0 | Shift left by two |
| 1 1 1 | Reserved |

Table 5 - Accumulator Shifts (BFP mode)

GWR4:0 (BFP MODE ONLY)

Contents of the global weighting register: This stores the weighting of the largest word present with respect to the weighting of the original input words. Hence, if the contents of the GWR are 00010, this indicates that the largest word currently being processed has its binary point two bits to the right of the original data at the start of the BFP calculations. The contents of this register are updated at the end of each pass, according to the largest value of WTOUT occurring during that pass. (i.e. If WTOUT = 11, then GWR will be increased by 2). The GWR is presented in two's complement format. These outputs are superfluous in normal mode.

WTOUT1:0 (BFP MODE ONLY)

Word tag output. This tag records the weighting of the output words from the current cycle relative to the current global weighting register (see Table 6). It should be stored along with the A' and B' words as it will form the input word tags, WTA and WTB, for each complex word during the next pass. These outputs are superfluous in normal mode.

| WTOUT1:0 | Weighting of the output relative to the current global weighting register |
|----------|---|
| 0 0 | One less |
| 0 1 | The same |
| 1 0 | One more |
| 1 1 | Two more |

Table 6 - Word Tag Weightings

WTA1:0 (BFP MODE ONLY)

Word tag from the A-word. This word records the weighting of the A-word relative to the global weighting register on the previous pass. Although the A-word itself is not processed in the PDSP16116, this information is required by the control logic for the radix-2 butterfly FFT application. These inputs should be tied low in normal mode.

WTB1:0 (BFP & NORMAL MODES)

In BFP mode, this is the word tag from the B-word. This is operated in the same manner as WTA but for the B-word. The value of the word tags are used to ensure that the binary weighting of the A word and the product of the complex multiplier are the same at the inputs to the complex accumulator. Depending on which word is the larger, the weighting adjustment is performed using either the internal shifter or an external shifter controlled by SFTA. The word tags are also used to maintain the weighting of the final result to within plus two and minus one binary points relative to the new GWR. (On the first pass all word tags will be ignored).

In normal mode, these inputs perform a different function. They directly control the internal shifter at the output port as shown in Table 7.

| WTB1:0 | FUNCTION |
|--------|---|
| 11 | shift complex product one place to the left |
| 00 | no shift applied |
| 01 | shift complex product one place to the right |
| 10 | shift complex product two places to the right |

Table 7 - Normal Mode Shift Control

SFTA1:0 (BFP & NORMAL MODES)

In BFP mode, these signals act as as the A-word shift control. They allow shifting from one to four places to the right, see Table 8. Depending on the relative weightings of the A-words and the complex product, the A-word may have to be shifted to the right to ensure compatible weightings at the inputs to the PDSP16318 complex accumulator. (The two words must have the same weighting if they are to be added).

In normal mode, SFTA0 performs a different a different function. If WTB1:0 is set to implement a left shift, then overflow will occur if the data is fully 32 bits wide. This pin is used to flag such an overflow. SFTA1 is not used in normal mode.

| WTB1:0 | FUNCTION |
|--------|------------------------------------|
| 0 0 | Shift A-word 1 places to the right |
| 0 1 | Shift A-word 2 places to the right |
| 1 0 | Shift A-word 3 places to the right |
| 1 1 | Shift A-word 4 places to the right |

Table 8 - External A-word shift control

OSEL1:0

The outputs from the device are selected by the OSEL0 & OSEL1 instruction bits. These controls allow selection of the output combination during the current cycle. (They are not registered). These are four possible output configurations that allow either complex outputs of the most or least significant bytes, or real or imaginary outputs of the full 32 bit word (see Table 4). OSEL0 and OSEL1 should both be tied low when in BFP mode.

BFP MODE FFT APPLICATION

The PDSP16116 may be used as the main arithmetic unit of the butterfly processor which will allow the following FFT benchmarks:

- 1024 point complex radix-2 transform in 517us
- 512 point complex radix-2 transform in 235us
- 256 point complex radix-2 transform in 106us

In addition, with pin MBFP tied high, the BFP circuitry within the PDSP16116 can be used to adaptively rescale data throughout the course of the FFT so as to give high-resolution results.

The BFP system on the PDSP16116 can be used with any variation of the Radix-2 Decimation-In-Time FFT - e.g. the

Constant Geometry algorithm, the In-Place algorithm etc. An N-point Radix-2 DIT FFT is split into log(N) passes. Each pass consists of N/2 'butterflies', each performing the operation:

$$A' = A + B.W$$

$$B' = A - B.W$$

Where W is the complex coefficient and A & B are the complex data.

Fig.4 illustrates how a single PDSP16116 may be combined with two PDSP1601's and two PDSP16318's to form a complete BFP butterfly processor. The PDSP16318's are used to perform the complex addition and subtraction of the butterfly operation, while the PDSP1601's are used to match the data path of the A-word to the pipelining and shifting operations within the PDSP16116.

For more information on the theory and construction of this butterfly processor, refer to application note AN59.

BFP MODE OPERATION

The BFP mode on the PDSP16116 is intended for use in the FFT application described above. i.e. it is intended to prevent data degradation during the course of an FFT calculation. The operation of the PDSP16116 based BFP butterfly processor (see Fig.4) is described below.

The Block Floating Point System

A block floating point system is essentially an ordinary integer arithmetic system with some clever logic bolted on. The object of the extra logic is to lend the system some of the enormous dynamic range afforded by a true floating point system without suffering the corresponding loss in performance.

The initial data used by the FFT should all have the same binary arithmetic weighting. i.e. the binary point should occupy the same position in every data word, as is normal in integer arithmetic. However, during the course of the FFT, a variety of weightings are used in the data words to increase the dynamic range available. This situation is similar to that within a true floating point system, though the range of numbers representable is more limited. In the BFP system used in the PDSP16116, there are, within any one pass of the FFT, four possible positions of the binary point within the integer words. To record the position of its binary point, each word has a 2-bit word tag associated with it. By way of example, in a particular pass we may have the following four positions of binary point available, each denoted by a certain value of word tag:

| | |
|----------------------|---------------|
| XX.XXXXXXXXXXXXXX | word tag = 00 |
| XXX.XXXXXXXXXXXXXX | word tag = 01 |
| XXXX.XXXXXXXXXXXXXX | word tag = 10 |
| XXXXX.XXXXXXXXXXXXXX | word tag = 11 |

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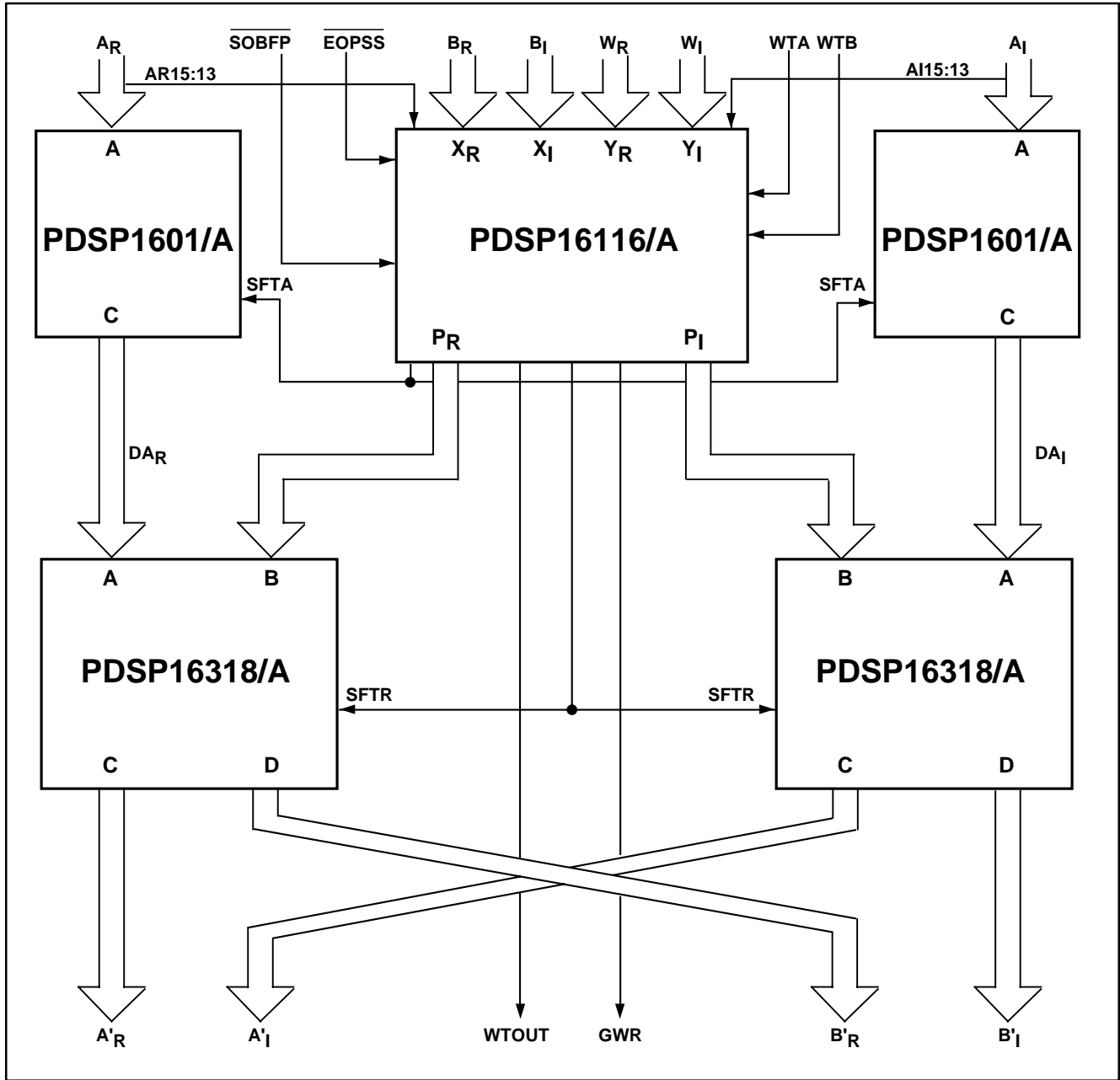


Figure 5 - FFT Butterfly Processor

At the end of each constituent pass of the FFT, the positions of the binary point supported may change to reflect the trend of data increase or decreases in magnitude. Hence, in the pass following that of the above example, the four positions of binary point supported may be change to:

- XX.XXXXXXXXXXXXX word tag = 00
- XXX.XXXXXXXXXXXXX word tag = 01
- XXXX.XXXXXXXXXXXXX word tag = 10
- XXXXX.XXXXXXXXXXXXX word tag = 11

Thus we can determine the position of the binary point relative to its initial position by modifying the value of GWR by WTOUT for a given word as shown in Table 6. As an example, if GWR=01001 and WTOUT=10 then the binary point has moved 10 places to the right of its original position.

This variation in the range of binary points supported from pass to pass (i.e. the movement of the binary point relative to its position in the original data) is recorded in the GWR.

The butterfly operation

The butterfly operation is the arithmetic operation which is repeated many times to produce an FFT. The PDSP16116A based butterfly processor performs this operation in a low power high accuracy chip set.

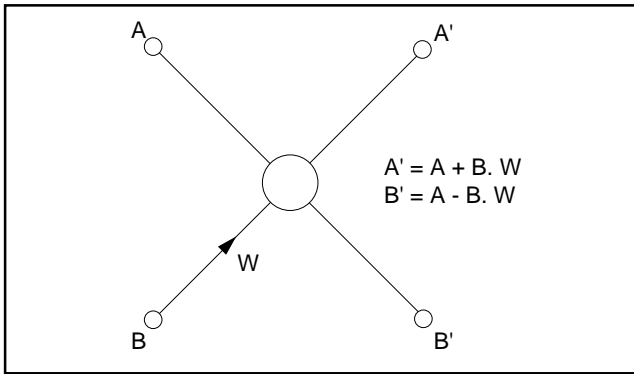


Figure 6 - Butterfly Operation

A new butterfly operation is commenced each cycle, requiring a new set of data for , B, W, WTA and WTB. Five cycles later, the corresponding results A' and B' are produced along with their associated WTOUT. In between, the signals SFTA and SFTR are produced and acted upon by the shifters in the PDSP1601/A and PDSP16318/A. The timing of the data and control signals is shown in Fig.6.

The results (A' and B') of each butterfly calculation in a pass must be stored away to be used later as the input data (A and B) in the next pass. Each result must be stored together with its associated word tag, WTOUT. Although WTOUT is common to both A' and B', it must be stored separately with each word as the words are used on different cycles during the next pass. At the inputs, the word tag associated with the A word is known as WTA and the word tag associated with the B word is known as WTB. Hence, the WTOUTs from one pass will become the WTAs and WTBs for the following pass. It should be noted that the first pass is unique in that word tags need not be input into the butterfly as all data initially has the same weighting. Hence, during the first pass alone, the inputs WTA and WTB are ignored.

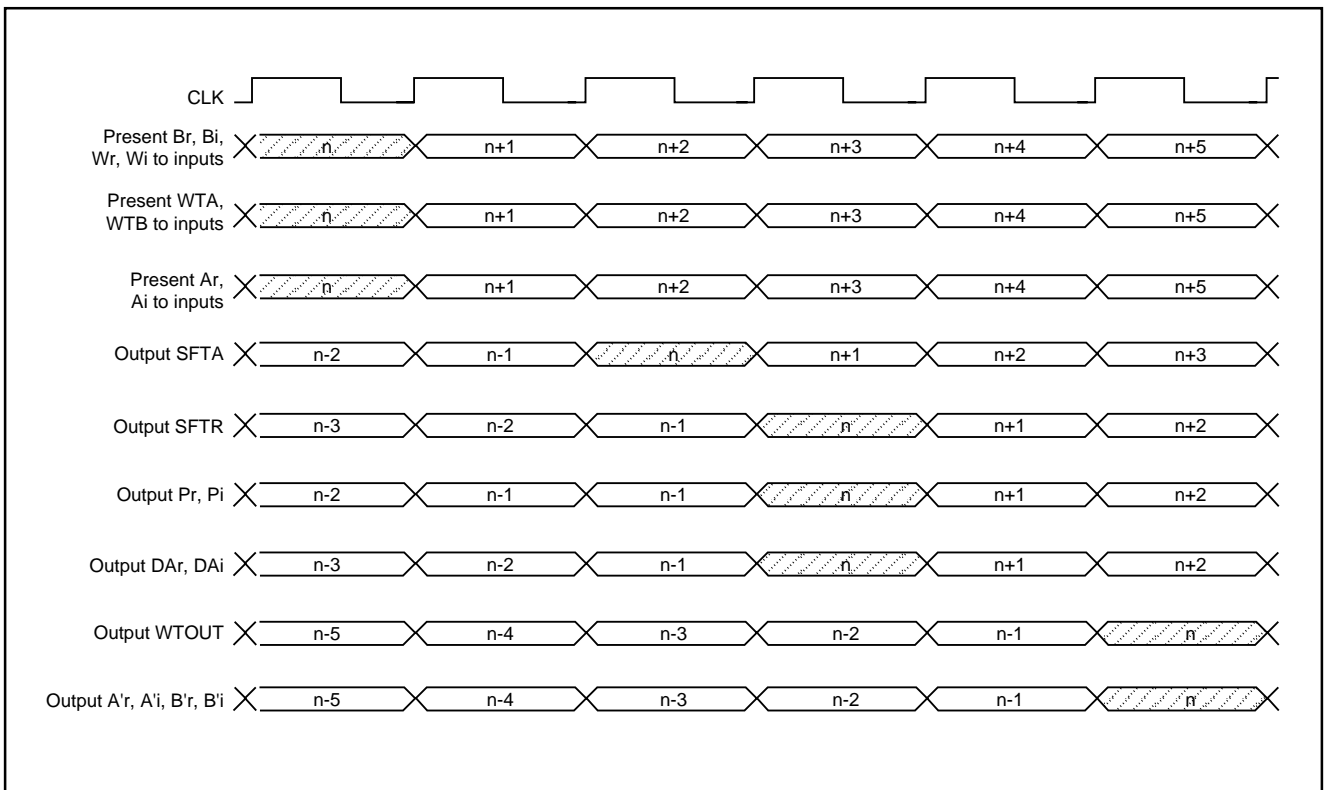


Figure 7 Butterfly Data and Control Signals

PDSP16116/A/MC

Control of the FFT

To enable the block floating point hardware to keep track of the data, the following signals are provided :

- SOBFP - start of the FFT
- EOPSS - end of current pass

These inform the PDSP16116/A when an FFT is starting and when each pass is complete. Fig.7 shows how these signals should be used and a commentary is provided below.

To commence the FFT, the signal EOPSS should be set high (where it will remain for the duration of the pass). SOBFP should be pulled low during the initial cycle when the first data words A and B are presented to the inputs of the butterfly processor. The following cycle SOBFP must be pulled high

where it should remain for the duration of the FFT. New data is presented to the processor each successive cycle until the end of the first pass of the FFT. On the last cycle of the pass, the signal EOPSS should be pulled low and remain low for a minimum of five cycles *, the time required to clear the pipeline of the butterfly processor so that all the results from one pass are obtained before commencing the following pass. On the initial cycle of each new pass, the signal EOPSS should be pulled high and it should remain high until the final cycle of that pass, when it is pulled low again.

* Should a longer pause be required between passes - to arrange the data for the next pass, for example, then EOPSS may be kept low as long as necessary - the next pass cannot commence until it is brought high again.

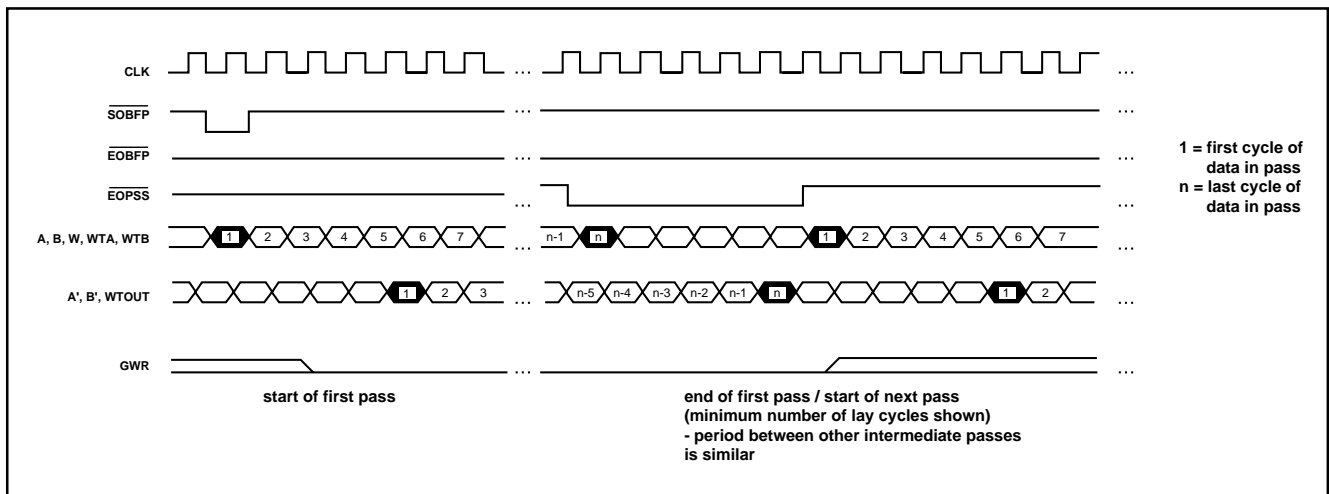


Figure 8 - Use of the BFP Control Signals

FFT Output Normalisation

When an FFT system outputs a series of FFT results for display, storage or transmission, it is essential that all results are compatible, i.e. with the binary point in the same position. However, in order to preserve the dynamic range of the data in the FFT calculation, the PDSP1601/A employs a range of different weightings. Therefore, data must be re-formatted at the end of the FFT to be pre-determined common weighting. This can be done by comparing the exponent of given data word with the pre-determined universal exponent and then shifting the data word by the difference. The PDSP1601/A, with its multifunction 16 bit barrel shifter, is ideally suited to this task.

What value should the Universal Exponent take? Well, according to theory, the largest possible data result from an FFT is N times the largest input data. This means that the binary point can move a maximum of $\log_2(N)$ places to the right. Hence, if we choose the Universal Exponent to be $\log_2(N)$ this should give us sufficient range to represent all data points faithfully.

In practice, data output may never approach the theoretical maximum. Hence, it may be worthwhile to try various Universal Exponents and choose the one best suited to the particular application.

Data is output from the butterfly processor with a two-part exponent: the 5-bit GWR applicable to all data words from a given FFT and a 2-bit WTOUT associated with each individual data word. To find the complete exponent for a given word, the GWR for that FFT must be modified by its WTOUT as shown in Table 6. The result is the number of places the binary point has shifted to the right during the course of the FFT.

This value must be compared with the Universal Exponent to determine the shift required. This is done by subtracting it from the Universal Exponent. The number of places to be shifted is equal to the difference between the two exponents. The shift can be implemented in a PDSP1601/A. The shift value is fed into the SV port.

As FFT data consists of real and imaginary parts, either two PDSP1601As must be used (controlled by the same logic) or a single PDSP1601/A could be used handling real and imaginary data on alternate cycles (using the same instructions for both cycles).

N.B.

It is easier to simply add the word tag to the exponent for the purpose of determining the shift required, instead of modifying it according to Table.6. To compensate for this, the Universal Exponent may be increased by one.

An example of an output normalisation circuit is shown in Fig.8. Only 4 bit data paths are used in calculating the shift. This means that we must be able to trap very small values negative of GWR and force a 15-bit right shift in such cases.

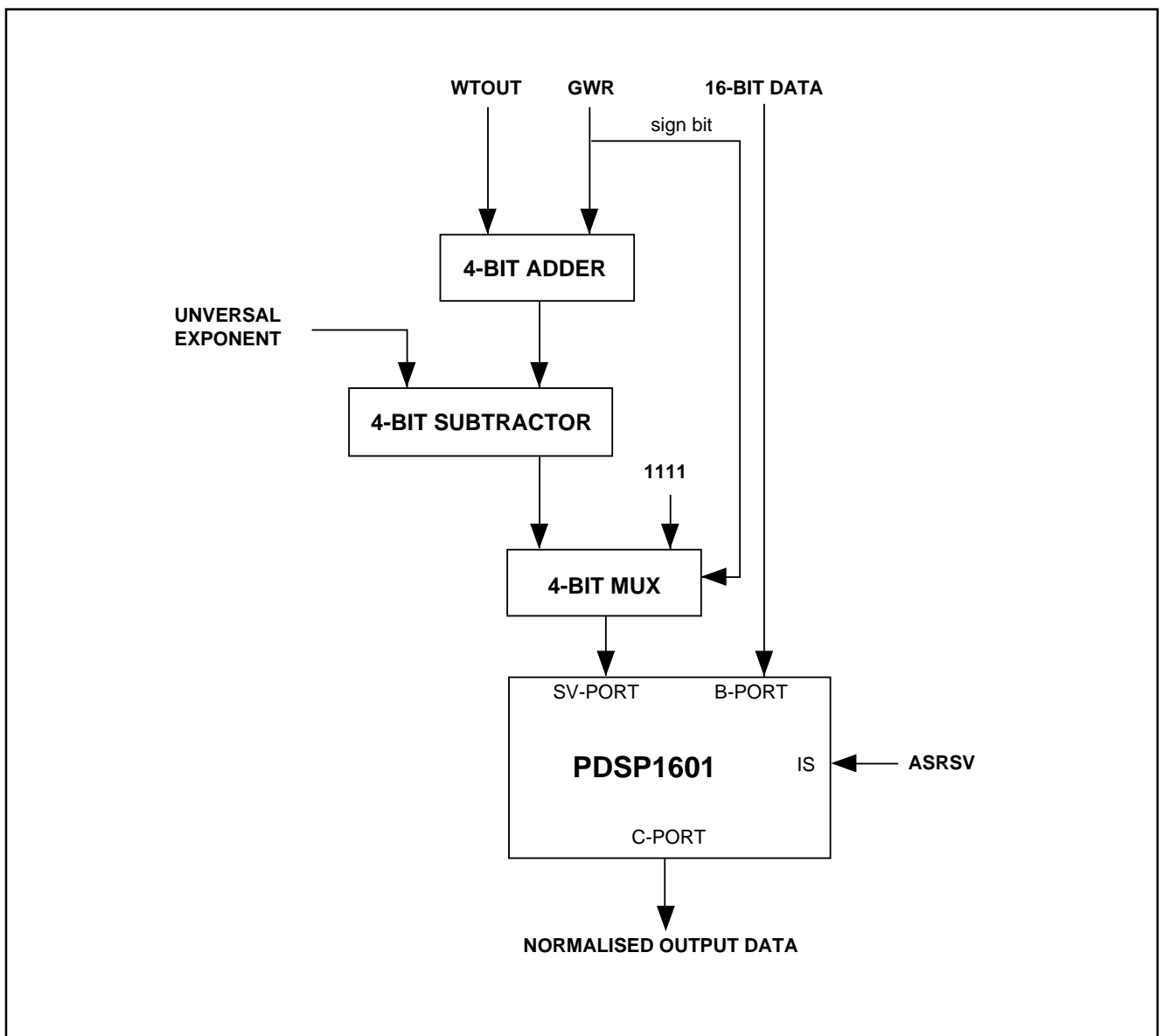


Fig.9 Output Normalisation Circuitry

PDSP16116/A/MC

ABSOLUTE MAXIMUM RATINGS (Note 1)

| | |
|--|--------------------------|
| Supply voltage V_{CC} | -0.5V to 7.0V |
| Input voltage V_{IN} | -0.5V to $V_{CC} + 0.5V$ |
| Output voltage V_{OUT} | -0.5V to $V_{CC} + 0.5V$ |
| Clamp diode current per I_k (see note 2) | 18mA |
| Static discharge voltage (HBM) | 500V |
| Storage temperature range T_s | -65°C to +150°C |
| Ambient temperature with power applied T_{AMB} | |
| Military | -55°C to +125°C |
| Industrial | -40°C to +85°C |
| Junction temperature | 150°C |
| Package power dissipation | 1000mW |
| Thermal resistances | |
| Junction to case θ_{JC} | 12°C/W |
| Junction to case θ_{JA} | 29°C/W |

NOTES

- Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
- Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
- Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):

Industrial: $T_{AMB} = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0V \pm 10\%$, $GND = 0V$

Military: $T_{AMB} = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0V \pm 10\%$, $GND = 0V$

Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|------------------------|----------|-------|------|------|---------------|-------------------------|
| | | Min. | Typ. | Min. | | |
| Output high voltage | V_{OH} | 2.4 | | - | V | $I_{OH} = 8\text{mA}$ |
| Output low voltage | V_{OL} | - | | 0.4 | V | $I_{OL} = -8\text{mA}$ |
| Input high voltage | V_{IH} | 3.0 | | - | V | CLK input only |
| Input high voltage | V_{IH} | 2.2 | | - | V | All other inputs |
| Input low voltage | V_{IL} | - | | 0.8 | V | $GND < V_{IN} < V_{CC}$ |
| Input leakage current | I_{IN} | -10 | | +10 | μA | |
| Input capacitance | C_{IN} | | 10 | | pF | $GND < V_{IN} < V_{CC}$ |
| Output leakage current | I_{OZ} | -50 | | +50 | μA | $V_{CC} = \text{Max}$ |
| Output S/C current | I_{OS} | 10 | | 300 | mA | |

Switching Characteristics

| Characteristic | PDSP16116 | | PDSP16116A | | Units | Conditions |
|--|-----------|------|------------|------|-------|------------------|
| | Min. | Max. | Min. | Max. | | |
| CLK rising edge to P-PORTS | 5 | 45 | 5 | 23 | ns | 2 x LSTTL + 20pF |
| CLK rising edge to WTOUT1:0 | 5 | 30 | 5 | 20 | ns | 2 x LSTTL + 20pF |
| CLK rising edge to GWR4:0 | 5 | 30 | 5 | 20 | ns | 2 x LSTTL + 20pF |
| CLK rising edge to SFTA1:0 | 5 | 60 | 5 | 30 | ns | 2 x LSTTL + 20pF |
| CLK rising edge to SFTR2:0 | 5 | 50 | 5 | 28 | ns | 2 x LSTTL + 20pF |
| Setup \overline{CEX} or \overline{CEY} to CLK rising edge | 11 | - | 8 | - | ns | |
| Hold \overline{CEX} or \overline{CEY} to CLK rising edge | - | 0 | - | 0 | ns | |
| Setup X or Y port inputs to CLK rising edge | 11 | - | 8 | - | ns | |
| Hold X or Y port inputs to CLK rising edge | - | 2 | - | 0 | ns | |
| Setup WTA1:0, WTB1:0, \overline{SOBFP} or \overline{EOPSS} inputs to CLK rising edge | 14 | - | 8 | - | ns | |
| Hold WTA1:0, WTB1:0, \overline{SOBFP} or \overline{EOPSS} inputs to CLK rising edge | - | 0 | - | 0 | ns | |
| Setup CONX or CONY inputs to CLK rising edge | 14 | - | 8 | - | ns | |
| Hold CONX or CONY inputs to CLK rising edge | - | 0 | - | 0 | ns | |
| Setup AR15:13 or AI15:13 to CLK rising edge | 14 | - | - | - | ns | |
| Hold AR15:13 or AI15:13 to CLK rising edge | - | 0 | - | 0 | ns | |
| OPSEL to valid P-PORTS | - | 35 | - | 20 | ns | 2 x LSTTL + 20pF |
| \overline{OER} or \overline{OEI} rising PR-PORT or PI-PORT high to Z | - | 35 | - | 25 | ns | see Fig.9 |
| \overline{OER} or \overline{OEI} rising PR-PORT or PI-PORT low to Z | - | 45 | - | 25 | ns | see Fig.9 |
| \overline{OER} or \overline{OEI} falling PR-PORT or PI-PORT Z to high | - | 22 | - | 18 | ns | see Fig.9 |
| \overline{OER} or \overline{OEI} falling PR-PORT or PI-PORT Z to low | - | 24 | - | 18 | ns | see Fig.9 |
| Clock period | 100 | - | 50 | - | ns | |
| Clock high time | 30 | - | 12 | - | ns | |
| Clock low time | 20 | - | 12 | - | ns | |
| Vcc Current (CMOS input levels) | - | 60 | - | 80 | mA | see Note 4 |
| Vcc Current (TTL input levels) | - | 100 | - | 130 | mA | see Note 4 |

NOTE 4 :- V_{CC} = Max Outputs unloaded, clock freq = Max

| Test | Waveform - measurement level |
|---|------------------------------|
| Delay from output high to output high impedance | |
| Delay from output low to output high impedance | |
| Delay from output high impedance to output low | |
| Delay from output high impedance to output high | |

V_H - Voltage reached when output driven high
 V_L - Voltage reached when output driven low

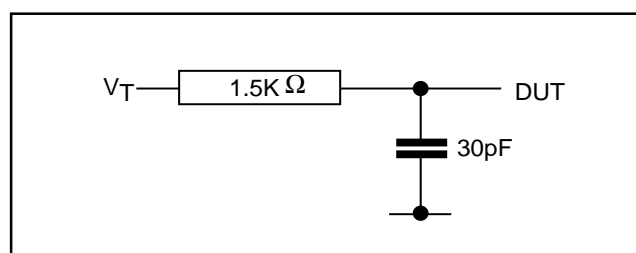


Fig.10 Three state delay measurement load



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