ZARLINK SEMICONDUCTOR

SL2100

Single chip synthesised broadband converter

Datasheet

DS5365 ISSUE 1.2 November 2001

Ordering Information

SL2100B/KG/NP2S (tubes)
SL2100B/KG/NP2T (tape and reel)

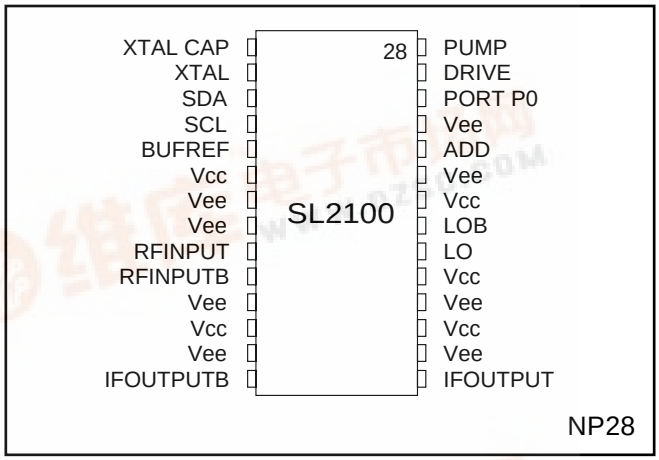


Figure 1 - Pin allocation

Features

- Single chip synthesised broadband solution
- Compatible with both up converter and downconverter requirements in double conversion tuner applications
- Compatible with digital and analogue system requirements
- CSO < -62 dBc, CTB < -64 dBc
- Extremely low phase noise balanced local oscillator, with I^2C bus controlled band switching and with very low fundamental and harmonic radiation
- Integral fast mode compliant I^2C bus controlled PLL frequency synthesiser designed for high comparison frequencies and low phase noise performance
- Buffered crystal output for pipelining system reference frequency
- Full ESD protection. (Normal ESD handling procedures should be observed)

Applications

- Double conversion tuners
- Digital Terrestrial tuners
- Cable Modems
- Data transmit systems
- Data communications systems
- MATV

Description

The SL2100 is a fully integrated single chip broadband mixer oscillator with on-board low phase noise I^2C bus controlled PLL frequency synthesiser. It is intended primarily for application in double conversion tuners as both the up and down converter and is compatible with HIIF frequencies up to 1.4 GHz and all standard tuner IF output frequencies.

The device contains all elements necessary, with the exception of local oscillator tuning network, loop filter and crystal reference to fabricate a complete synthesised block converter, compatible with digital and analogue requirements.

Quick Reference Data

All data applies with the following conditions unless otherwise stated;

a) nominal loads as follows;
   1220 MHz output load as in figure (3)
   44 MHz output load as in figure (4)
b) input signal per carrier of 62 dbuV

Characteristic		Units
RF input operating range	50 - 1400	MHz
Input noise figure, SSB,		
50-860 MHz	6.5 - 8.5	dB
860 - 1400	8.5 - 12	dB
Conversion gain	12	dB
CTB (fully loaded matrix)	c -68	dBc
CSO (fully loaded matrix)	c -65	dBc
P1dB input referred	110	dBuV
Local oscillator phase noise as upconverter		
SSB @ 10 kHz offset	c -90	dBc/Hz
SSB @ 100 kHz offset	c -112	dBc/Hz
Local oscillator phase noise as downconverter		
SSB @ 10 kHz offset	c -93	dBc/Hz
SSB @ 100 kHz offset	c -115	dBc/Hz
Local oscillator phase noise floor	-136	dBc/Hz
LO reradiation from RF input		
fundamental	TBC	dBuV
second harmonic		dBuV
third harmonic		dBuV
PLL spurs on converted output with input @ 60 dBuV	c -70	dBc
PLL maximum comparison frequency	4	MHz
PLL phase noise at phase detector	-152	dBc/Hz

• dBm assumes a 75 Ω characteristic impedance, and 0 dBm = 109 dBuV

Functional Description

The SL2100 is a bipolar, broadband wide dynamic range mixer oscillator with on-board I^2C bus controlled PLL frequency synthesiser, optimised for application in double conversion tuner systems as both the up and down converter. It also has application in any system where a wide dynamic range broadband synthesised frequency converter is required.

The SL2100 is a single chip solution containing all necessary active circuitry and simply requires an external tuneable resonant network for the local oscillator sustaining network. The pin assignment is contained in figure (1) and the block diagram in figure (2).

Converter section

In normal application the RF input is interfaced through appropriate impedance matching and an AGC front end to the device input. The RF input preamplifier of the device is designed for low noise figure, within the operating region of 50 to 1400 MHz and for high intermodulation distortion intercept so offering good signal to noise plus composite distortion spurious performance when loaded with a multi carrier system. The preamplifier also provides gain to the mixer section and back isolation from the local oscillator section. The typical RF input impedance and matching network for broadband upconversion are contained in figures (6) and (7) respectively and for narrow band downconversion in figures (8) and (9) respectively. The input referred two tone intermodulation test condition spectrum is shown in figure (10). The typical input NF is contained in figure (11) and the typical gain in figure (12).

The output of the preamplifier is fed to the mixer section which is optimised for low radiation application. In this stage the RF signal is mixed with the local oscillator frequency, which is generated by the on-board oscillator. The oscillator block uses an external tuneable network and is optimised for low phase noise. The typical application as an upconverter is shown in figure (13) and the typical phase noise performance in figure (14). The typical application as a downconverter is shown in figure (15), and the phase noise performance in figure (17). This block interfaces direct with the internal PLL to allow for frequency synthesis of the local oscillator.

Finally the output of the mixer provides an open collector differential output drive. The device allows for selection of an IF in the range 30-1400 MHz so covering standard HIIFs between 1 and 1.4 GHz and all conventional tuner output IFs. When used as a broadband upconverter to a HIIF the output should be differentially loaded, for example with a differential SAW filter, to maximise intermodulation performance. A nominal load is shown in figure (3), which will typically be terminated with a differential 200 Ω load. When used as a narrowband downconverter the output should be differentially loaded, either with a discrete differential to single ended converter as in figure (4), shown tuned to 44 MHz IF, or direct in to a differential input amplifier or SAWF, in which case external loads to Vcc will be required, an example load for 44 MHz application, with a gain of 16 dB is contained in figure (5).

The typical IF output impedance as upconverter and downconverter are contained in figures (17) and (18) respectively.

In all applications care should be taken to achieve symmetric balance to the IF outputs to maximise intermodulation performance.

The typical key performance data at 5V Vcc and 25 deg C ambient are shown in the section headed 'QUICK REFERENCE DATA'.

PLL frequency Synthesiser

The PLL frequency synthesiser section contains all the elements necessary, with the exception of a reference frequency source and loop filter to control the oscillator, so forming a complete PLL frequency synthesised source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance.

The LO signal from the oscillator drives an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces direct with the 15-bit fully programmable divider. The programmable divider is of MN+A architecture, where the dual modulus prescaler is 16/17, the A counter is 4-bits, and the M counter is 11 bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency. This frequency is derived either from the on-board crystal controlled oscillator or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider which is programmable into 1 of 29 ratios as detailed in

figure (19). The typical application for the crystal oscillator is contained in figure (20)

The output of the phase detector feeds a charge pump and loop amplifier, which when used with an external loop filter and high voltage transistor, integrates the current pulses into the varactor line voltage, used for controlling the oscillator.

The programmable divider output Fpd divided by two and the reference divider output Fcomp can be switched to port P0 by programming the device into test mode. The test modes are described in figure (21).

The crystal reference frequency can be switched to BUFREF output by bit RE as described in figure (22)

Programming

The SL2100 is controlled by an I^2C data bus and is compatible with both standard and fast mode formats.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by I^2C bus format. The device can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. Tables 1 and 2 in figure (23) illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one device in an I^2C bus system. Figure (23), table 3 shows how the address is selected by applying a voltage to the 'ADD' input. When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

Write mode

With reference to figure (23), table 1, bytes 2 and 3 contain frequency information bits 2^{14}-2^0 inclusive. Byte 4 controls the synthesiser reference divider ratio, see figure (19) and the charge pump setting, see figure (24). Byte 5 controls the test modes, see figure (21), the buffered crystal reference output select RE, see figure (22) and the output port P0.

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2, and a logic '1' indicating byte 4. Having interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Having received two complete data bytes, additional data bytes can be entered, where byte interpretation follows the same procedure, without re-addressing the device. This procedure continues until a STOP condition is received. The STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

Read mode

When the device is in read mode, the status byte read from the device takes the form shown in figure (23) table 2.

Bit 1 (POR) is the power-on reset indicator, and this is set to a logic '1' if the Vcc supply to the device has dropped below 3V (at 25˚C), e.g. when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to the power up condition.

Bit 2 (FL) indicates whether the synthesiser is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked.

Programmable features

Synthesiser programmable divider	Function as described above
Reference programmable divider	Function as described above.
Charge pump current	The charge pump current can be programmed by bits C1 & C0 within data byte 4, as defined in figure (24).
Test mode	The test modes are defined by bits T2 - T0 as described in figure (21)
General purpose ports, P0	The general purpose port can be programmed by bits P0; Logic '1' = on Logic '0' = off (high impedance)
Buffered crystal reference output select	The buffered crystal reference frequency can be selected by bit RE as described in figure (22)

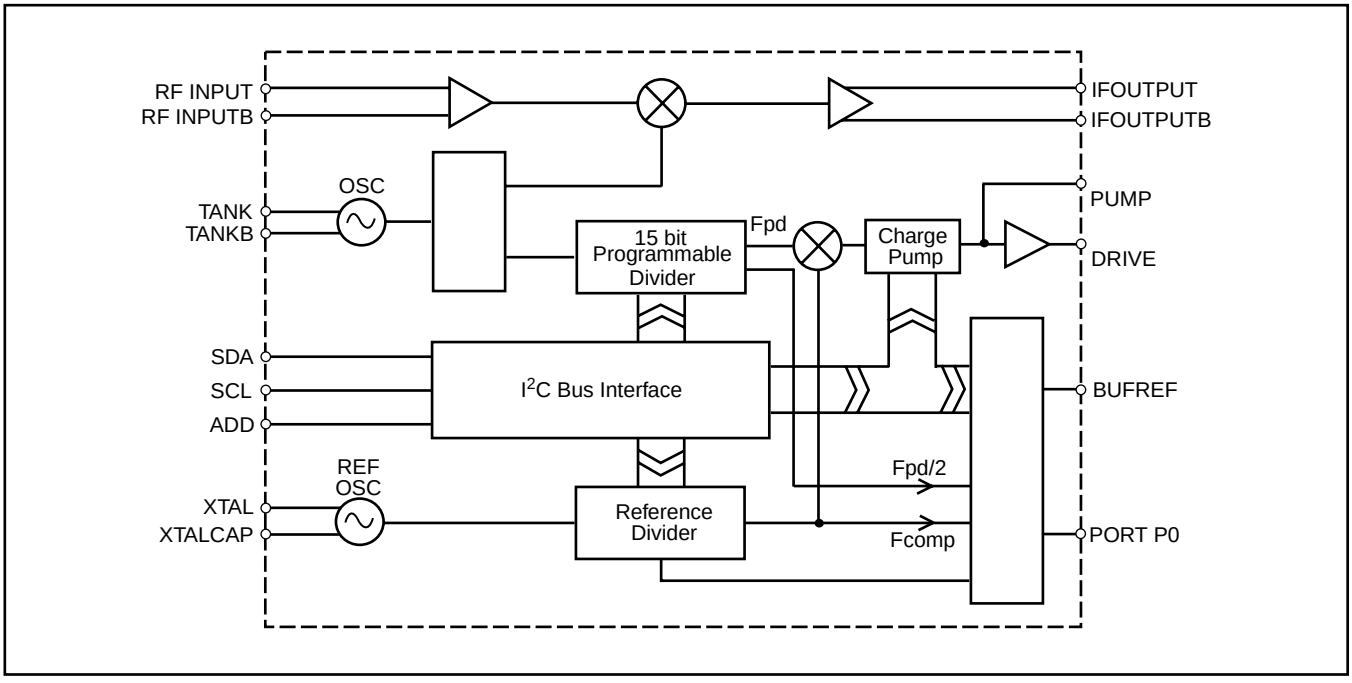


Figure 2 - SL2100 Block Diagram

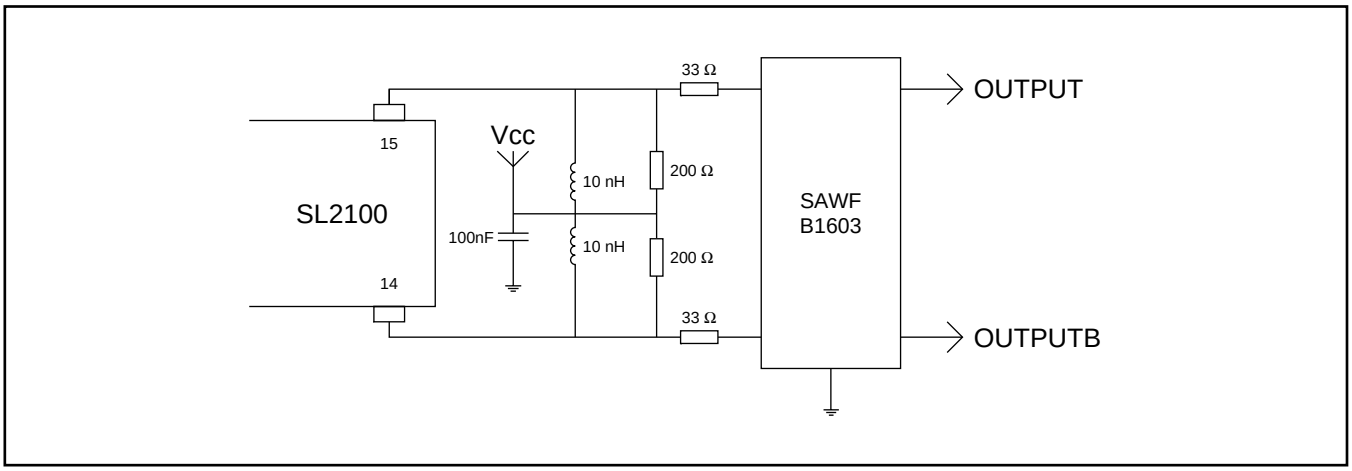


Figure 3 - Nominal output load as upconverter into differential SAWF

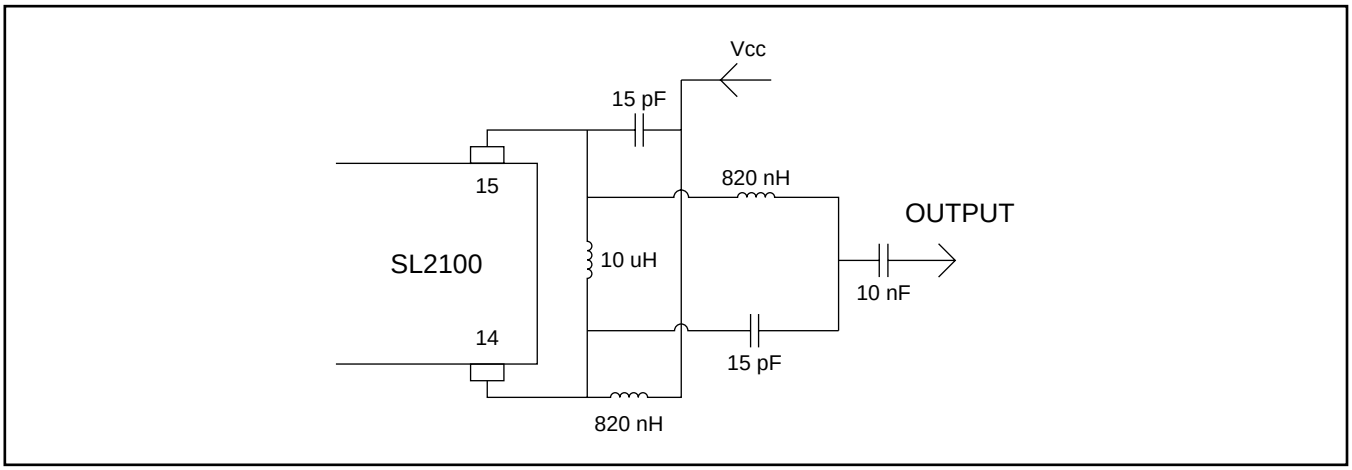


Figure 4 - Nominal output load as downconverter, 44MHz IF

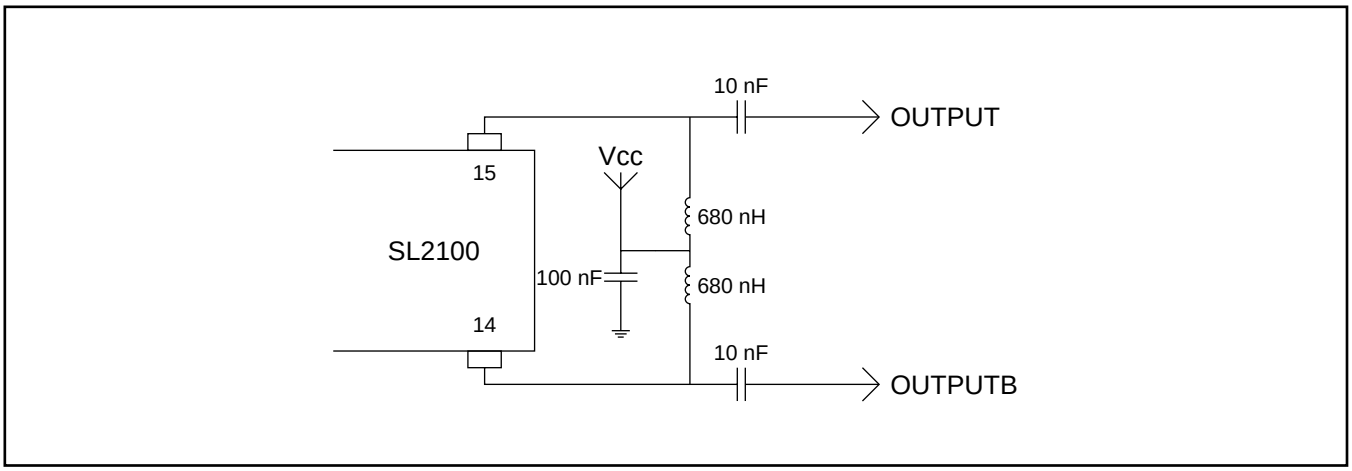


Figure 5 - Output load as downconverter to a differential amplifier

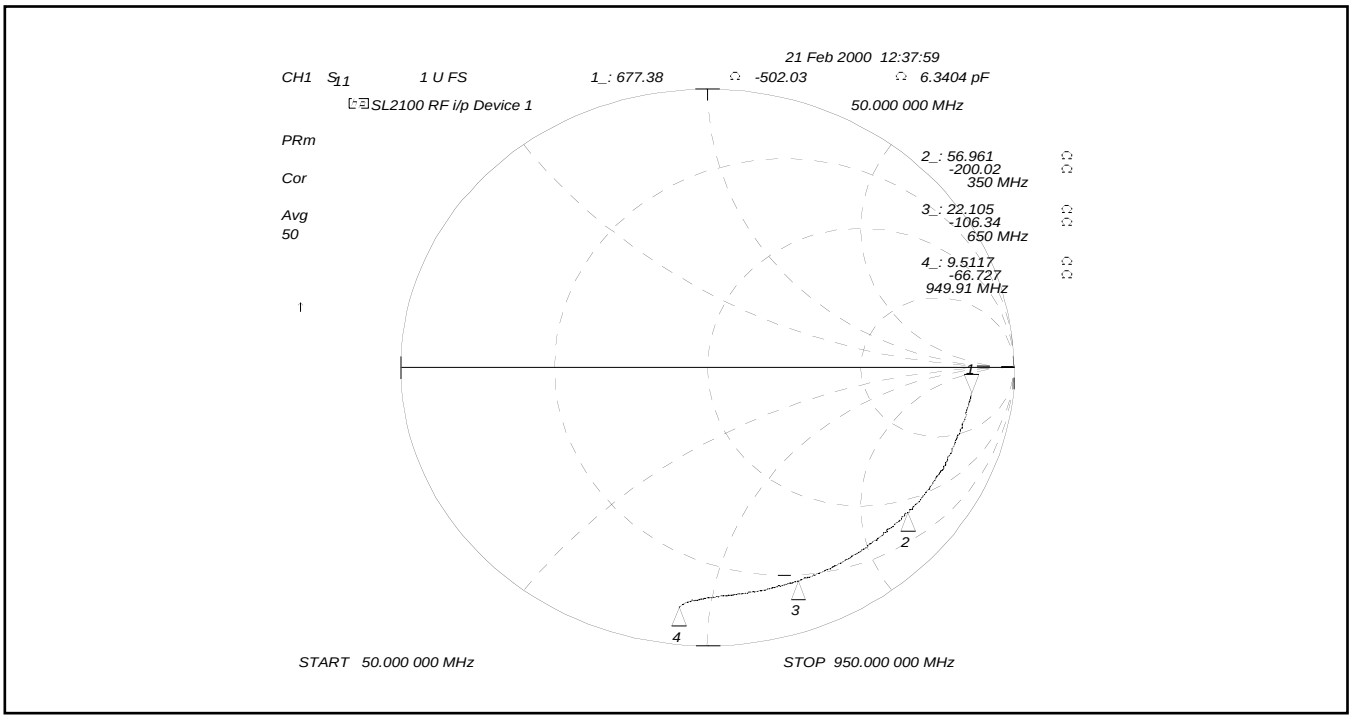


Figure 6 - Typical RF input impedance as broadband upconverter

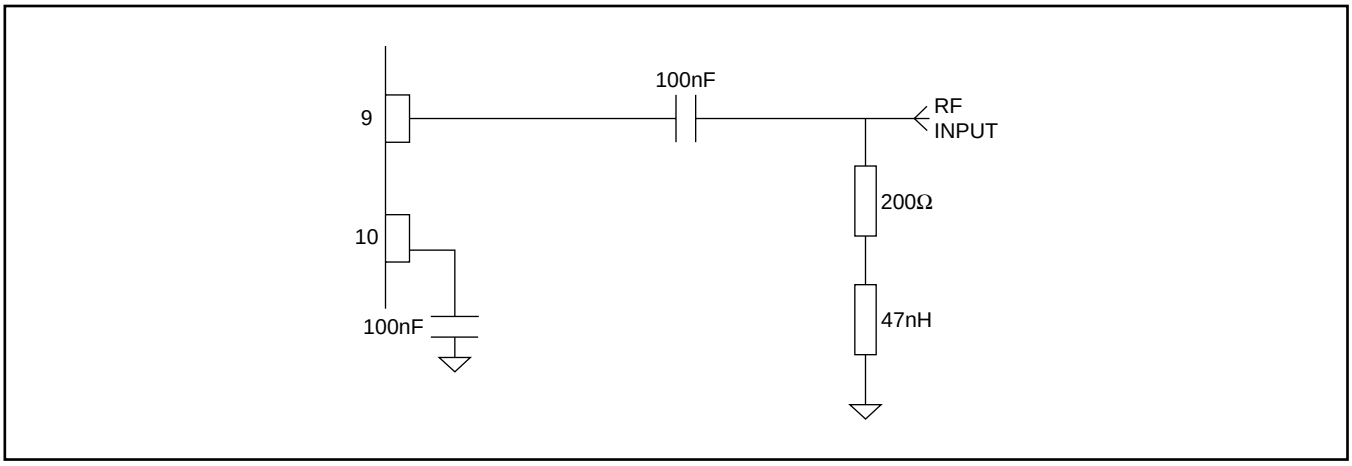


Figure 7 - RF input impedance matching network as 50 -860MHz upconverter

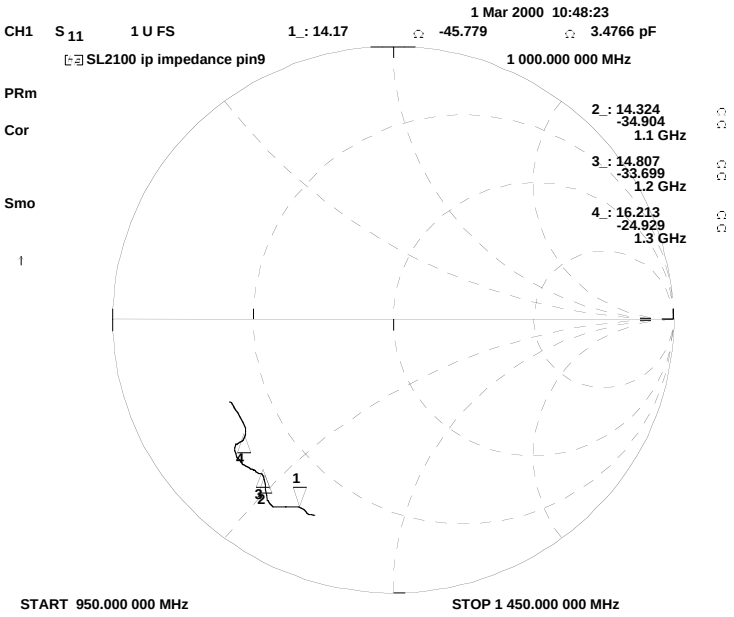


Figure 8 - Typical RF input impedance as narrow band downcoverter

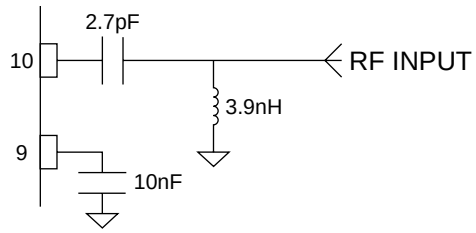


Figure 9 - RF input impedance matching network as 1.22GHz downconverter

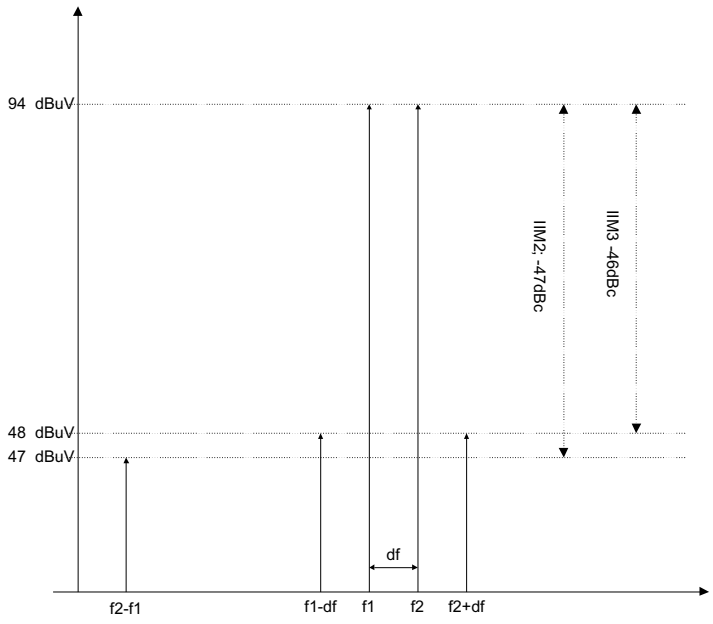


Figure 10 - Two tone intermodulation test condition spectrum, input referred

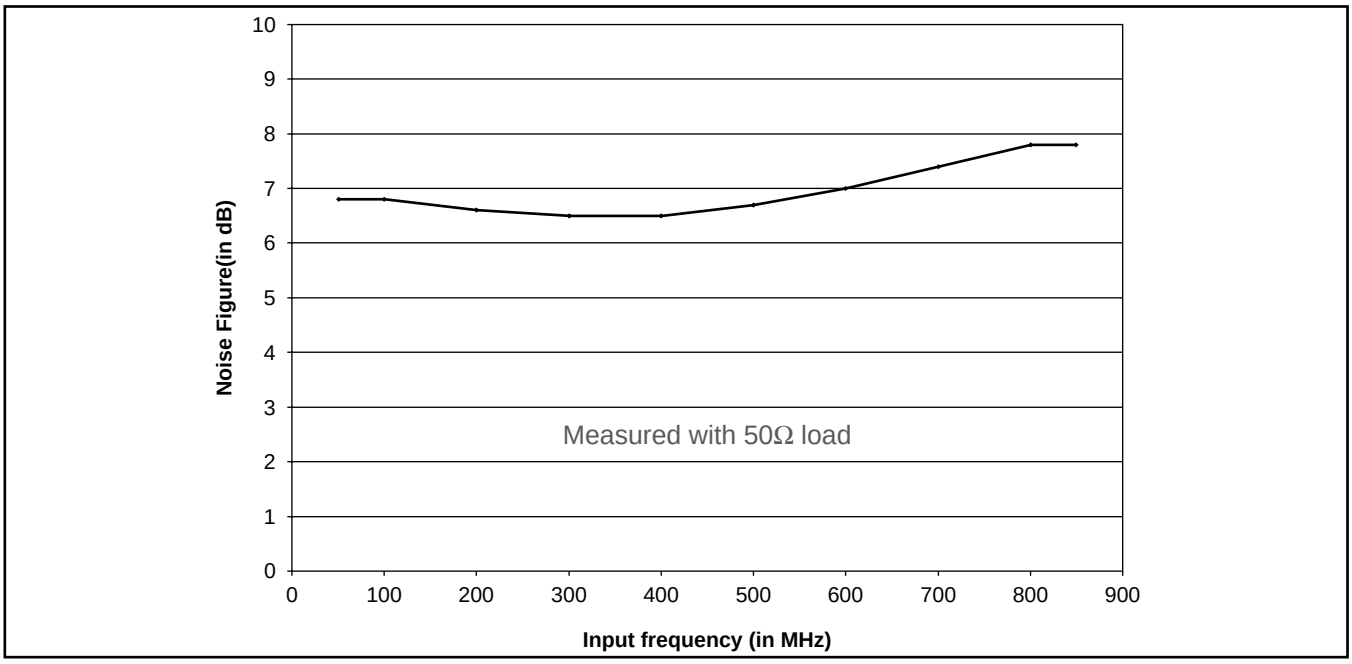


Figure 11 - Input NF

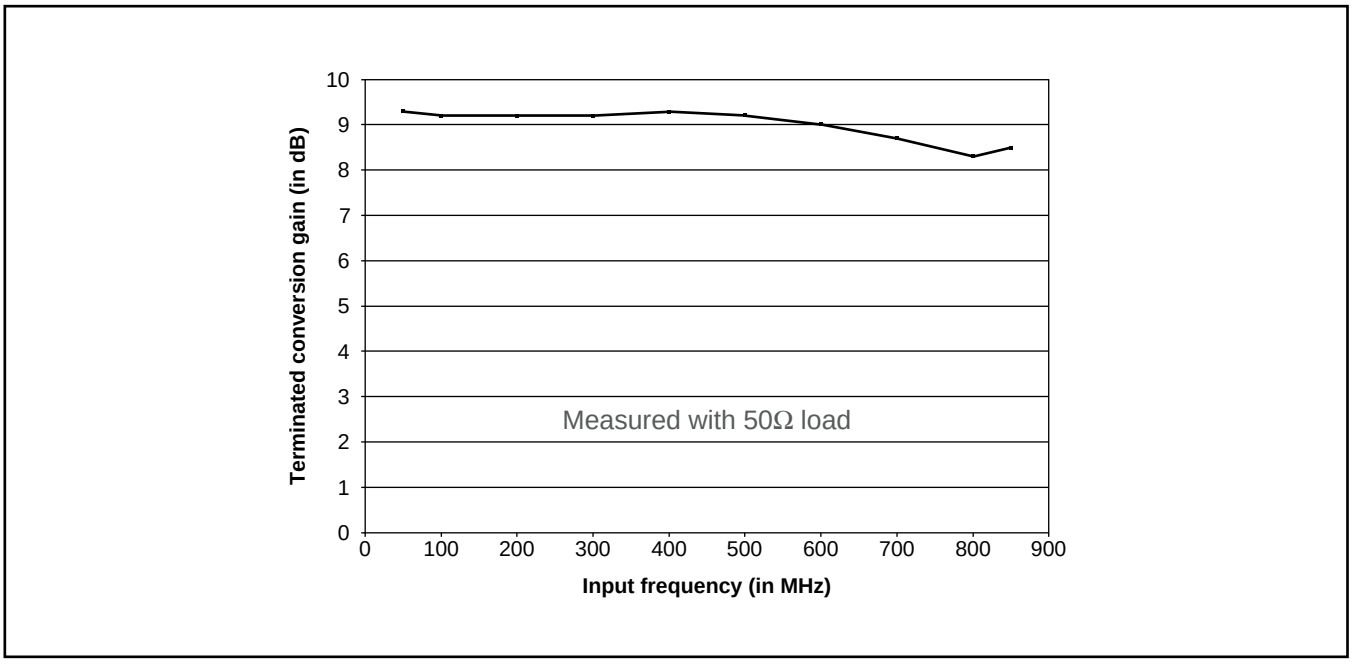


Figure 12 - Conversion Gain as upconverter

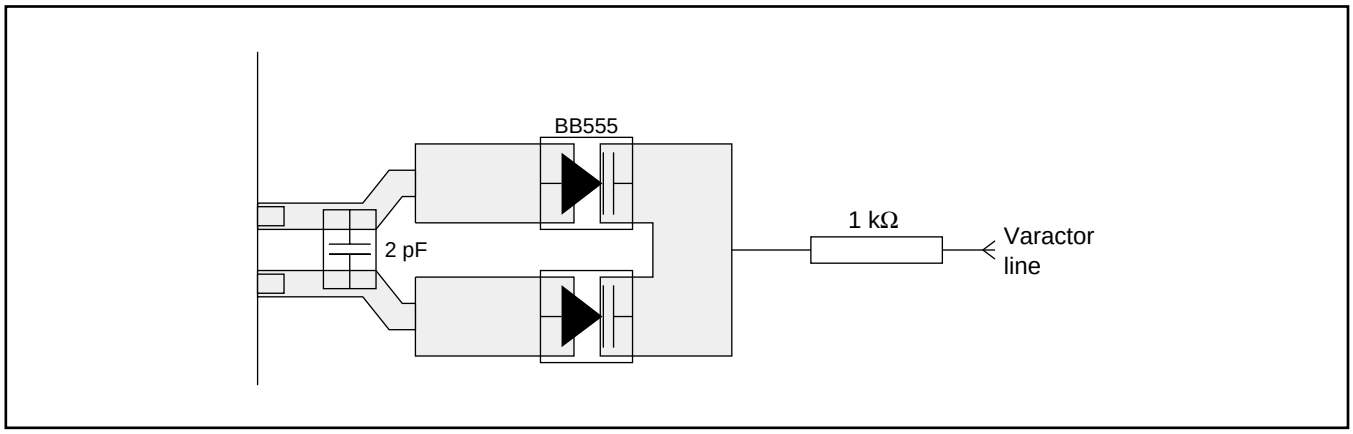


Figure 13 - Upconverter oscillator application

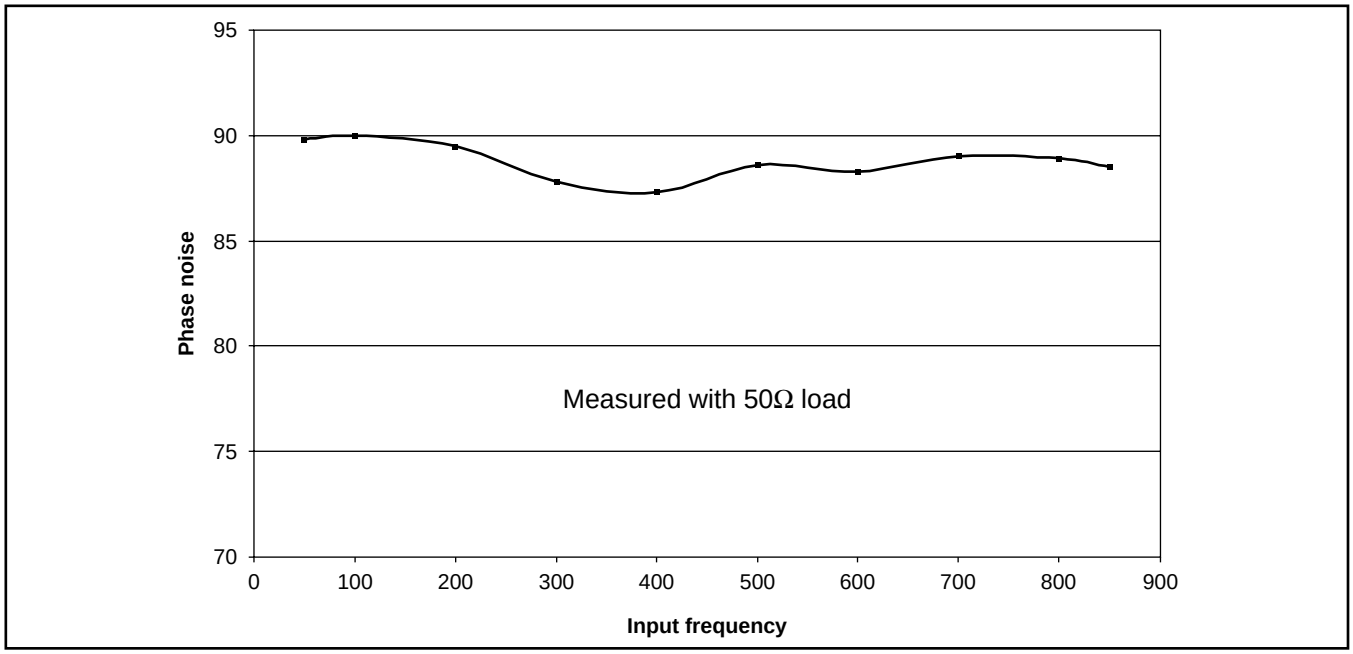


Figure 14 - Oscillator typical phase noise performance

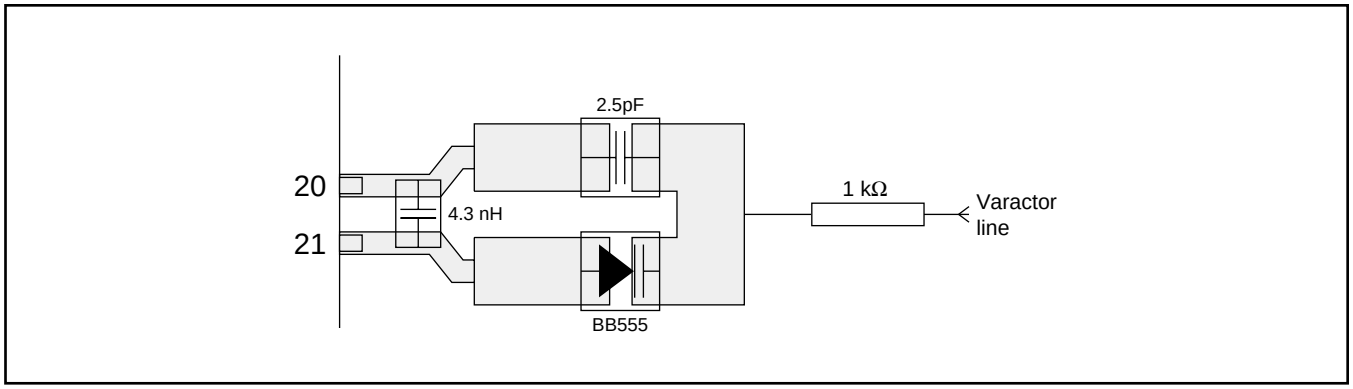


Figure 15 - Downconverter oscillator application

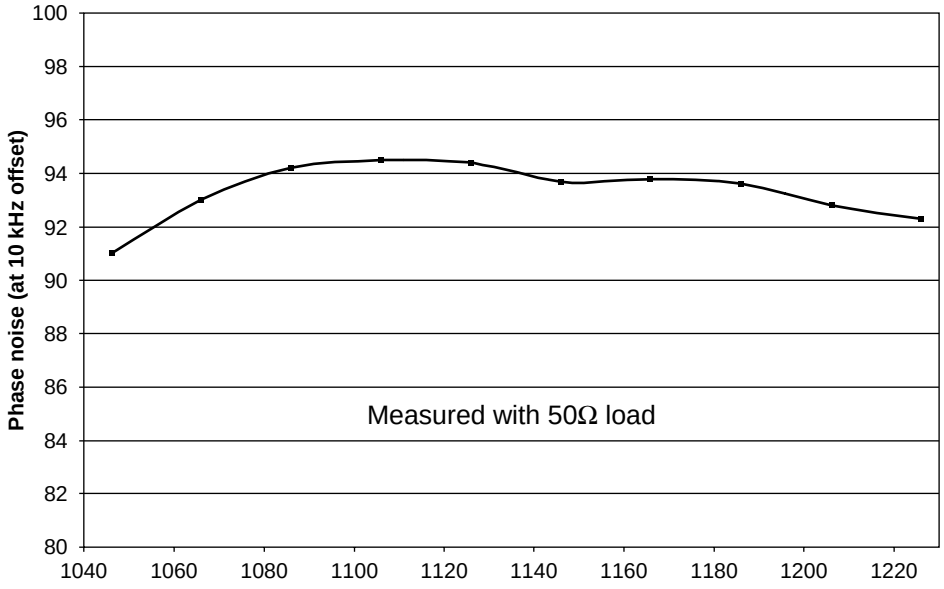


Figure 16 - Typical phase noise performance as downconverter

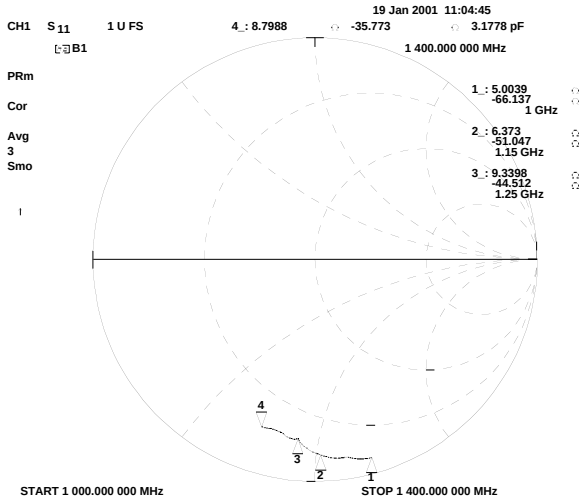
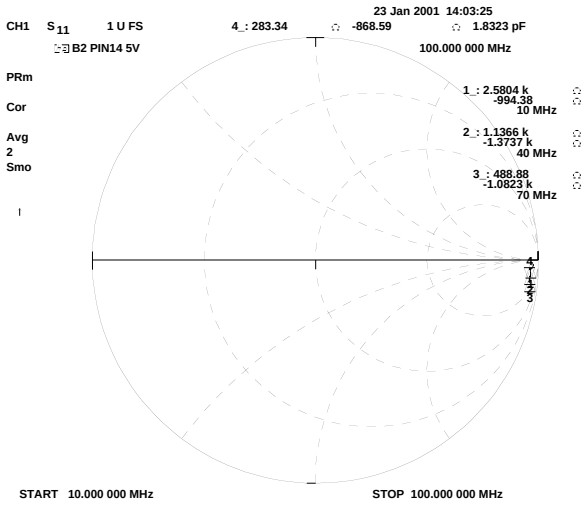


Figure 17 - Typical IF output impedance as upconverter, single-ended



R4	R3	R2	R1	R0	Ratio
0	0	0	0	0	2
0	0	0	0	1	4
0	0	0	1	0	8
0	0	0	1	1	16
0	0	1	0	0	32
0	0	1	0	1	64
0	0	1	1	0	128
0	0	1	1	1	256
0	1	0	0	0	Illegal state
0	1	0	0	1	5
0	1	0	1	0	10
0	1	0	1	1	20
0	1	1	0	0	40
0	1	1	0	1	80
0	1	1	1	0	160
0	1	1	1	1	320
1	0	0	0	0	Illegal state
1	0	0	0	1	6
1	0	0	1	0	12
1	0	0	1	1	24
1	0	1	0	0	48
1	0	1	0	1	96
1	0	1	1	0	192
1	0	1	1	1	384
1	1	0	0	0	Illegal state
1	1	0	0	1	7
1	1	0	1	0	14
1	1	0	1	1	28
1	1	1	0	0	56
1	1	1	0	1	112
1	1	1	1	0	224
1	1	1	1	1	448

Figure 19 - Reference division ratios

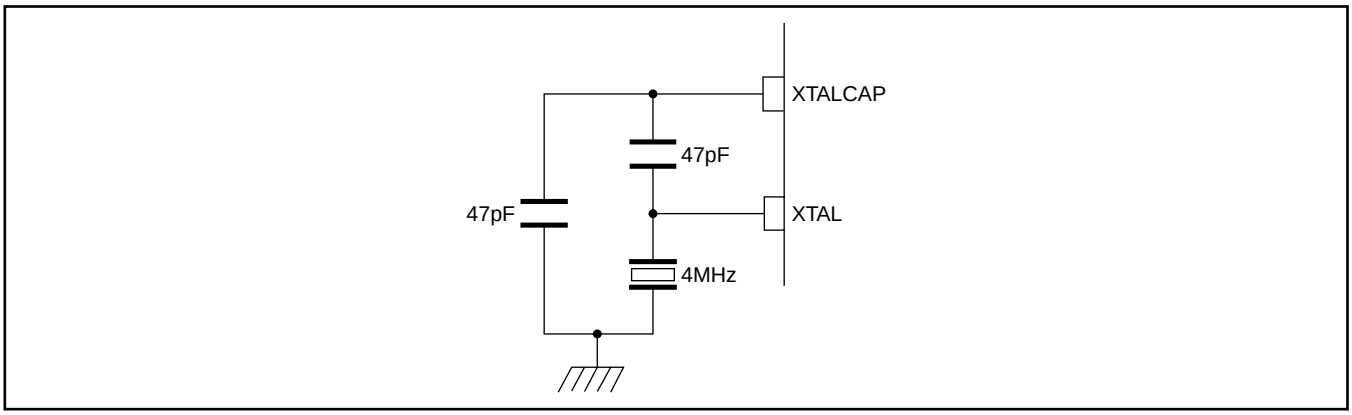


Figure 20 - Crystal oscillator application (typical)

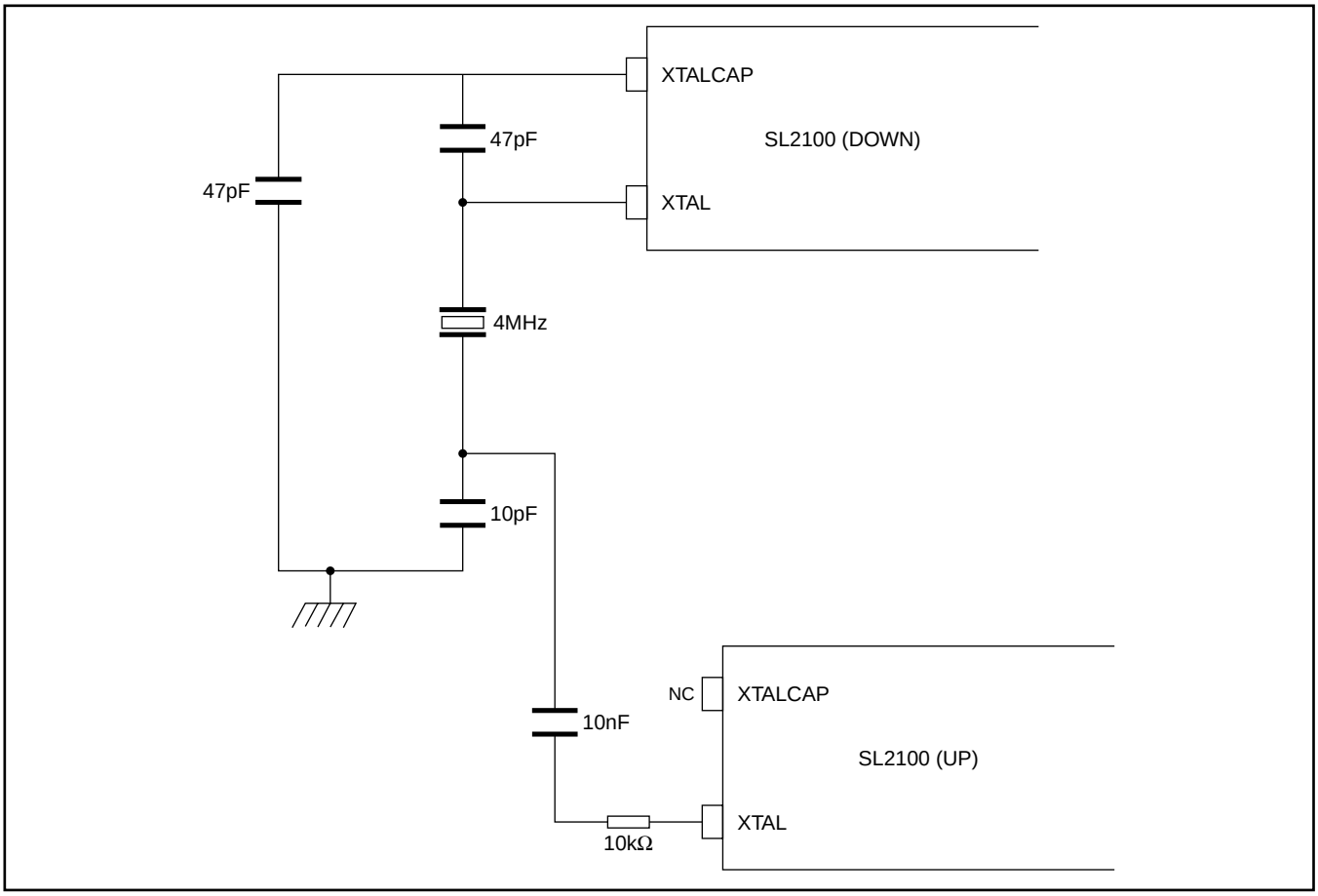


Figure 21 - Crystal oscillator application in dual conversion architecture

T2	T1	T0	Test mode description
0	0	0	Normal operation
0	0	1	Charge pump sink * Status byte FL set to logic '0'
0	1	0	Charge pump source * Status byte FL set to logic '0'
0	1	1	Charge pump disabled * Status byte FL set to logic '1'
1	0	0	Normal operation and Port P0 = Fpd/2
1	0	1	Charge pump sink * Status byte FL set to logic '0' Port P0 = Fcomp
1	1	0	Charge pump source * Status byte FL set to logic '0' Port P0 = Fcomp
1	1	1	Charge pump disabled * Status byte FL set to logic '1' Port P0 = Fcomp

Figure 21 - Test modes

* clocks need to be present on crystal and LO inputs to enable charge pump test modes and to toggle status byte bit FL

RE	BUFREF output
0	disabled, high impedance
1	enabled

Figure 22 - Buffered crystal reference output select

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Control data	1	C1	C0	R4	R3	R2	R1	R0	A	**Byte 4**
Control data	T2	T1	T0	X	X	X	RE	P0	A	**Byte 5**

Table 1 - Write data format (MSB is transmitted first)

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Programmable divider	POR	FL	0	0	0	0	0	0	A	**Byte 2**

Table 2 - Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1,MA0	:	Variable address bits (see Table 3)
2^{14}-2^{0}	:	Programmable division ratio control bits
C1-C0	:	Charge pump current select (see figure (24))
R4-R0	:	Reference division ratio select (see figure (19))
T2-T0	:	Test mode control bits (see figure (21))
P0	:	P0 port output state
POR	:	Power on reset indicator
FL	:	Phase lock flag
X	:	'Don't care'

MA1	MA0	Address input voltage level
0	0	0-0.1Vcc
0	1	Open circuit
1	0	0.4Vcc - 0.6 Vcc #
1	1	0.9 Vcc - Vcc

Table 3 - Address selection

Programmed by connecting a 30 kΩ resistor between pin and Vcc

Figure 23 - Data Formats

C1	C0	Current in µA		
		min	typ	max
0	0	+-98	+-130	+-162
0	1	+-210	+-280	+-350
1	0	+-450	+-600	+-750
1	1	+-975	+-1300	+-1625

Figure 24 - Charge pump current

Electrical Characteristics

Test conditions (unless otherwise stated)

Tamb = -40˚ to 85˚C, Vee= 0V, Vcc=5V+-5%

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	pin	min	typ	max	units	Conditions
Supply current			90	120	mA	IF outputs will be connected to Vcc through the differential load as in figures (3)&(4)
Input frequency range		50		1400	MHz	Operating condition only
Output frequency range		30		1400	MHz	Operating condition only
Composite peak input signal			97		dBuV	Operating condition only
All synthesiser related spurs on IF Output				-60	dBc	Within channel bandwidth of 8 MHz and with input power of 60 dBuV
Upconverter application						
Input frequency range		50		860	MHz	
Input impedance			75		Ω	See figure (6),
Input return loss		6			dB	With input matching network as in figure (7)
Input Noise Figure				9.5	dB	See figure (11), with input matching network as in figure (7)
Conversion gain			9		dB	Differential voltage gain to 200 Ω load on output of SAWF as in figure (3), see figure (12)
Gain variation across operation range		-1		+1	dB	50-860 MHz
Gain variation within channel				0.5	dB	Channel bandwidth 8 MHz within operating frequency range
Through gain			-20		dB	45-1400 MHz
CSO				-62	dBc	Measured with 128 channels at 62 dBuV
CTB				-64	dBc	Measured with 128 channels at 62 dBuV
$IPIP2_{2T}$		137			dBuV	See note (2)
$IPIP3_{2T}$		116			dBuV	See note (2)

Characteristic	pin	min	typ	max	units	Conditions
$IPIM2_{2T}$				-47	dBc	See note (2), see figure (10)
$IPIM3_{2T}$				-46	dBc	See note (2), see figure (10)
LO operating range		1		2.3	GHz	Maximum tuning range 0.9 GHz determined by application
LO phase noise, SSB						Application as in figure (13), see figure (14)
@ 10 kHz offset			-90	-85	dBc/Hz	
@ 100 kHz offset			-110	-106	dBc/Hz	
LO phase noise floor				-136	dBc/Hz	Application as in figure (13)
IF output frequency range		1		1.4	GHz	
LO and harmonic leakage to RF input						To device input
Fundamental			64		dBuV	
2nd harmonic			81		dBuV	
3rd harmonic			49		dBuV	
IF output impedance						See figure (17)
Downconverter application						
Input frequency range		1000		1400	MHz	
Input impedance			75		Ω	See figure (8)
Input return loss		12			dB	With input matching network as in figure (9)
Input Noise Figure				14	dB	Tamb=27˚C, with input matching network as in figure (9)
Conversion gain			12		dB	Differential voltage gain to 50 Ω load on output of impedance transformer as in figure (5)
Gain variation within channel				0.5	dB	Channel bandwidth 8 MHz within operating frequency range
Through gain			-20		dB	45-1400 MHz
$IPIP3_{2T}$		117			dBuV	See note (2)
$IPIM3_{2T}$				-46	dBc	See note (2), see figure (10)
LO operating range		1		2.3	GHz	Maximum tuning range determined by application, see note (4)

Characteristic	pin	min	typ	max	units	Conditions
LO phase noise, SSB						See figure (16)
@ 10 kHz offset			-94	-92	dBc/Hz	Application as in figure (15)
@ 100 kHz offset			-116	-112	dBc/Hz	
LO phase noise floor				-136	dBc/Hz	Application as in figure (13)
IF output frequency range				100	MHz	
IF output impedance						See figure (18)
SYNTHESISER						
SDA, SCL						I^2C 'Fast mode' compliant
Input high voltage		3		5.5	V	
Input low voltage		0		1.5	V	
Input high current				10	uA	Input voltage = Vcc
Input low current				-10	uA	Input voltage = Vee
Leakage current				10	uA	Vcc=Vee
Hysterysis			0.8		V	
SDA output voltage				0.4	V	Isink = 3 mA
				0.6	V	Isink = 6 mA
SCL clock rate				400	kHz	
Charge pump output current						See figure (24), Vpin = 2V
Charge pump output leakage			+-3	+-10	nA	Vpin = 2V
Charge pump drive output current		0.5			mA	Vpin = 0.7V
Crystal frequency		2		20	MHz	See figure (20) for application
Recommended crystal series resistance		10		200	Ω	4 MHz parallel resonant crystal
Oscillator temperature stability				TBC	ppm/°C	
Oscillator supply voltage stability				TBC	ppm/V	

Characteristic	pin	min	typ	max	units	Conditions
External reference input frequency		2		20	MHz	Sinewave coupled through10 nF blocking capacitor
External reference drive level		0.2		0.5	Vpp	Sinewave coupled through 10 nF blocking capacitor
Phase detector comparison frequency				4	MHz	
Equivalent phase noise at phase detector			-152		dBc/Hz	SSB, within loop bandwidth 2 MHz
			-158		dBc/Hz	250 kHz
Local oscillator programmable divider division ratio		240		32767		
Reference division ratio						See figure (19)
Output port						See note (3)
sink current		2			mA	Vport = 0.7
leakage current				10	uA	Vport =Vcc
Buffered REF/COMP output						AC coupled 0.0625-20 MHz,
output amplitude			0.35		Vpp	Enabled by bit RE=1 and default state on power-up
output impedance			250		Ω	
Address select						See figure (23) table (3)
Input high current				1	mA	Vin=Vcc
Input low current				-0.5	mA	Vin=Vee

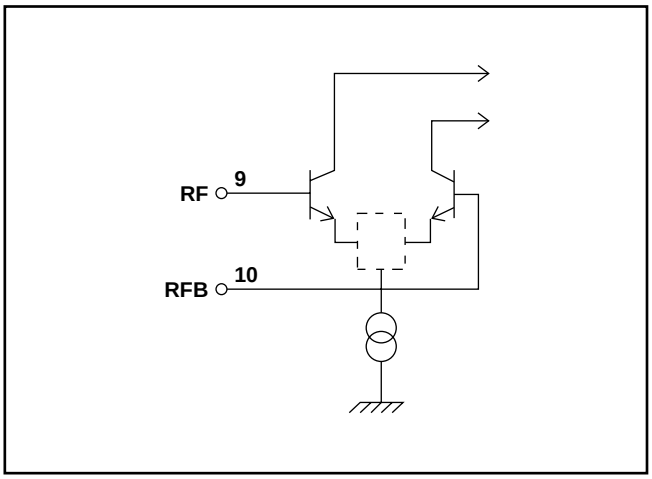
Notes

(1) All power levels are referred to 75 Ω and 0 dBm = 109 dBuV

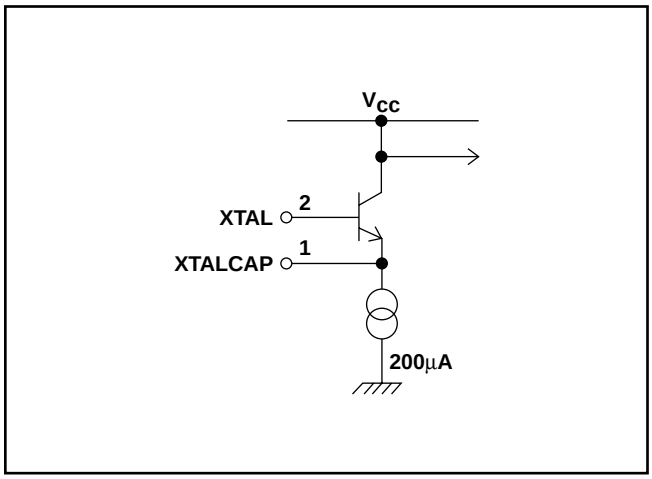
(2) Any two tones within RF operating range at 94 dBuV beating within band, with output load as in figure (3)

(3) Port powers up in high impedance state

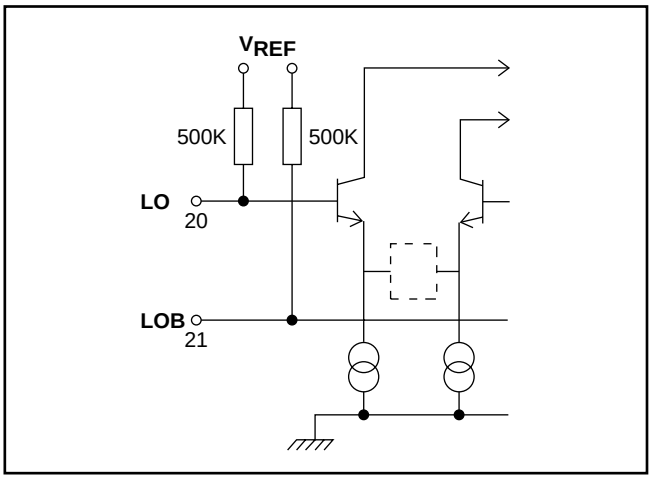
(4) To maximise phase noise the tuning range should be minimised and Q of resonator maximised. The application as in figure (15) has a tuning range of 200 MHz.



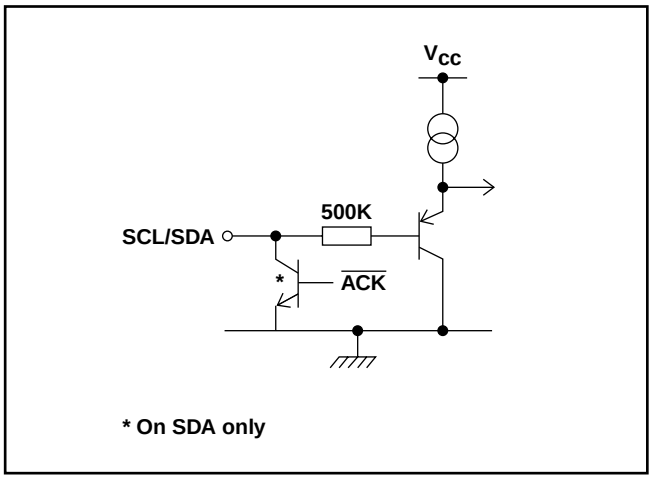
RF Inputs



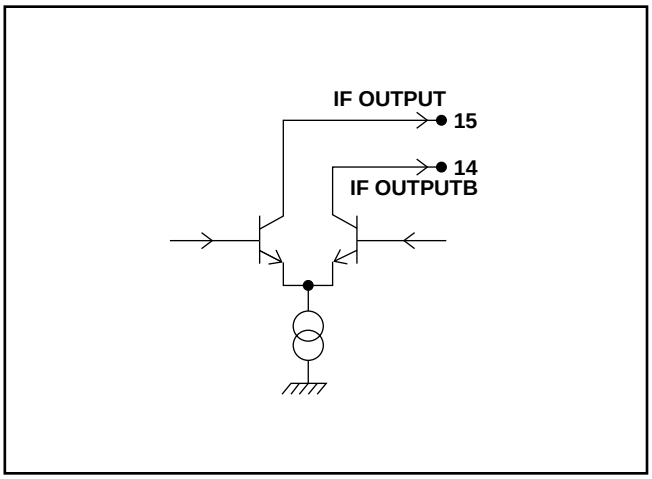
Reference Oscillator



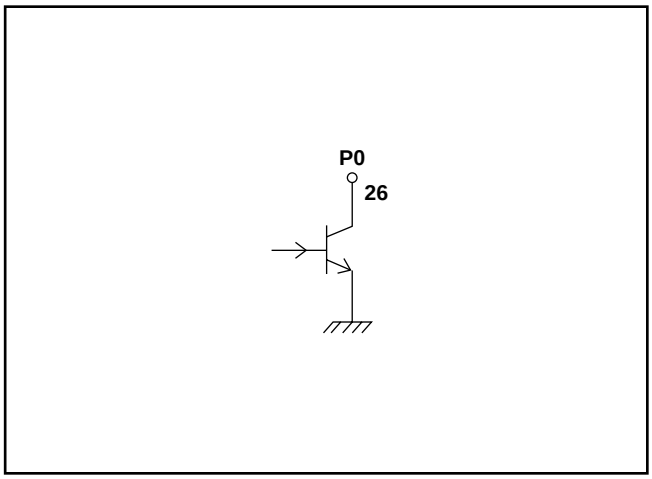
Oscillator Inputs



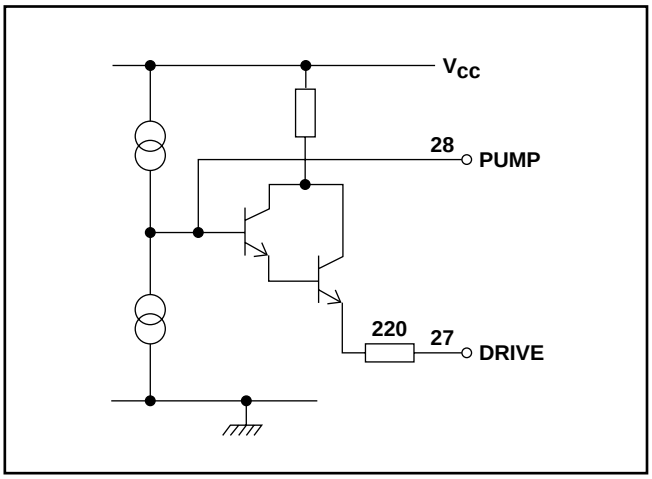
SDA/SCL (pins 3 and 4)



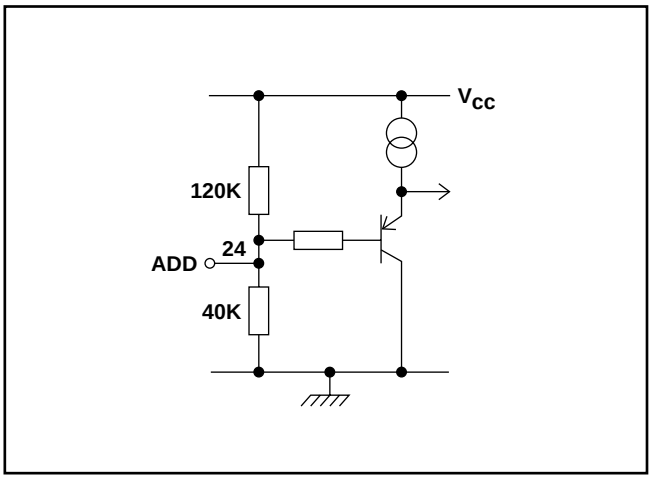
IF Outputs



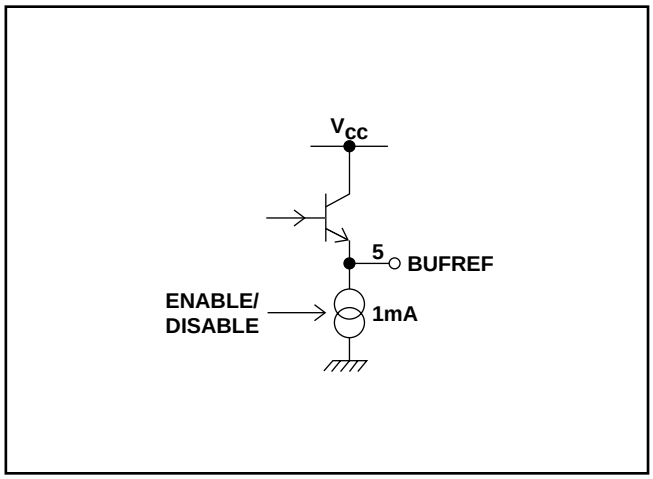
Output port



Loop amplifier



ADD Input

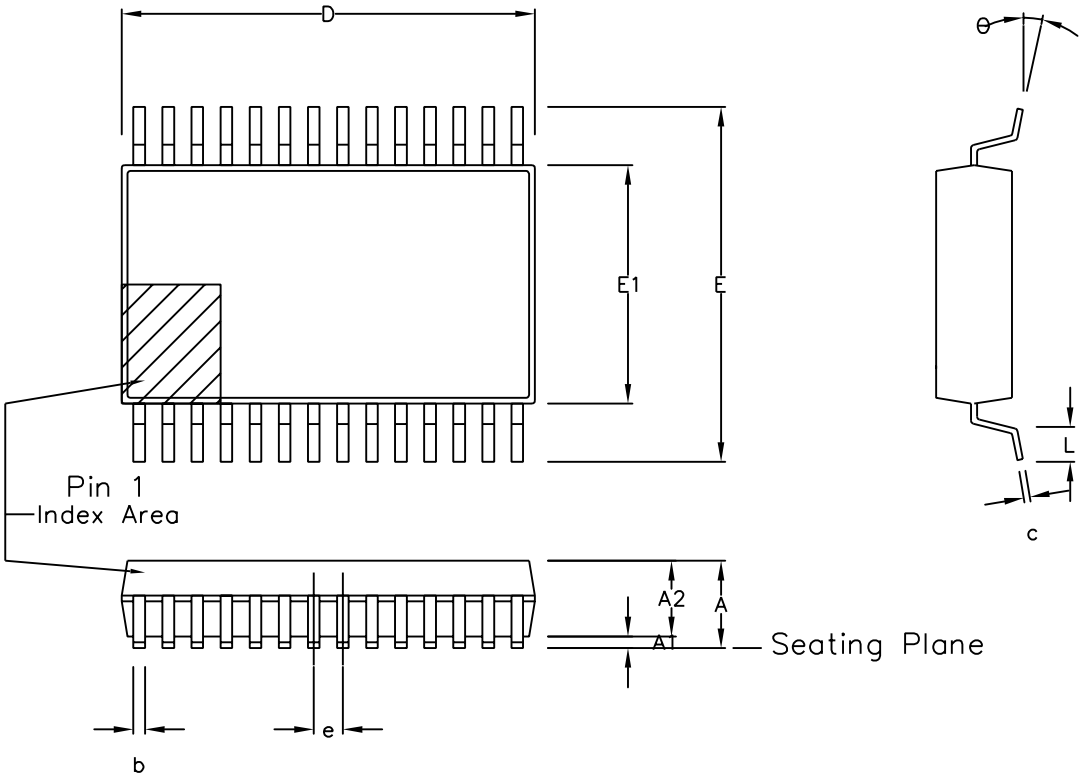


BUFREF ouput

Absolute Maximum Ratings

All voltages are referred to Vee at 0V

Characteristic	min	max	units	conditions
Supply voltage	-0.3	7	V	
RF input voltage		117	dBuV	Differential, ac coupled inputs
All I/O port DC offsets	-0.3	Vcc+0.3	V	
SDA, SCL DC offsets	-0.3	6	V	Vcc = Vee to 5.25V
Storage temperature	-55	150	˚C	
Junction temperature		150	˚C	
Package thermal resistance, chip to case		20	˚C/W	
Package thermal resistance, chip to ambient		85	˚C/W	
Power consumption at 5.25V		630	mW	
ESD protection	2		kV	Mil-std 883B method 3015 cat1



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.07
A1	0.05		0.20		0.002		0.00
A2	1.65		1.85		0.065		0.07
D	9.90		10.50		0.390		0.41
E	7.40		8.20		0.291		0.32
E1	5.00		5.60		0.197		0.22
L	0.55		0.95		0.022		0.03
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.01
c	0.09		0.25		0.004		0.01
θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. E							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Plymouth

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exce 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 m total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 m

ISSUE	1	2	3	
ACN	201935	205232	212478	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
NP / N

Package Code DD

Package Outline for 28 lea
SSOP (5.3mm Body Width)

GPD00296

For more information about all Zarlink products visit our Web Site at

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