ANALOG DEVICES

550kSPS 16-BIT ADC in µSO

Preliminary Technical Data — AD7686*

FEATURES

16 Bits Resolution with No Missing 16-Bit Codes
Throughput:
550 kSPS (Warp mode)
450 kSPS (Normal mode)
380 kSPS (Impulse mode)
INL: ± 3LSB Max (±0.0046 % of Full-Scale)
S/(N+D): 89 dB Typ @ 10 kHz
THD: –95 dB Typ @ 10 kHz
Pseudo-Differential Analog input range:
0V to V_{REF} with V_{REF} up to VDD
No Pipeline Delay
Single Supply Operation 5V and 2.7V with 2.5V/3V/5V logic interface
Multiple ADCs Daisy Chain and Busy Indicator
Serial Interface SPI/QSPI/µWire/DSP compatible
30 mW @ 5V/380ksps, TBD @ 3V Typical Power Dissipation,
80 µW @ 1 kSPS
Stand-by current (acquisition phase): 1 µA Max
µ-SOIC Package (µ-SO8 size)
Pin-to-Pin Compatible with the AD7685, AD7687, AD7688

Battery Powered Equipment
Data Acquisition
Instrumentation
Medical Instruments
Process Control

GENERAL DESCRIPTION

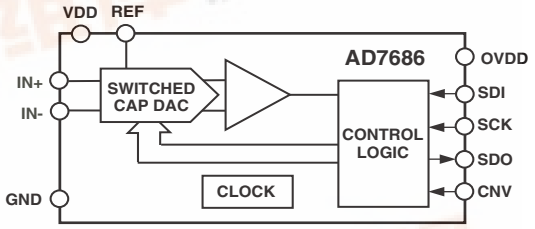
The AD7686 is a 16-bit, 550 kSPS, charge redistribution successive-approximation, Analog-to-Digital Converter which operates from a single power supply. It contains a high-speed 16-Bit sampling ADC without any missing code, an internal conversion clock, error correction circuits, and a flexible serial interface port. The part also contain a low noise, wide bandwidth, very short aperture delay track/hold circuit which can sample an analog input range from 0V to REF. The reference voltage REF is applied externally and can be set up to the supply voltage.

It features a very high sampling rate mode (Warp) and, for asynchronous conversion rate applications, a fast mode (Normal) and, for low power applications, a reduced power mode (Impulse) where the power is scaled with the throughput.

*Patent pending.

REV. PrD

FUNCTIONAL BLOCK DIAGRAM



µSO/SOT23 16 Bit ADC

Type / kSPS	100 kSPS	250 kSPS	380 - 550 kSPS
True Differential		AD7687 AD7684	AD7688
Pseudo Differential		AD7685 AD7683	AD7686
Unipolar	AD7680		

The serial interface features the possibility to "Daisy chain" several ADCs on a single 3 wires bus and provides an optionnal Busy indicator.

The AD7686 is hardware factory calibrated. It is fabricated using CMOS process and is housed in 10-lead µSOIC package with operation specified from –40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Superior INL
The AD7686 has a maximum integral non linearity of 3 LSB with no missing 16-bit code.

2. Fast Throughput.
The AD7686 is a very high speed (550 kSPS in Warp mode and 450 kSPS in Normal mode), charge redistribution, 16-Bit SAR ADC with no pipeline delay.

3. 2.7V or 5V Single Supply Operation
The AD7686 operates from a single supply, dissipates only TBD mW typical (Impulse), and even lower when a reduced throughput is used. It consumes 1 µA maximum during the acquisition phase.

4. Serial Interface with OVDD, Daisy Chain and Busy
2.5V, 3 V or 5 V logic 3-wire serial interface arrangement compatible with SPI and DSP host.

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AD7686–SPECIFICATIONS

(T_A = -40°C to +85°C, V_{REF} = 5V, VDD = 5 V, OVDD = 2.3V to 5.25V, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	IN+ - IN-	0		V_{REF}	V
Absolute Input Voltage	IN+	–0.1		VDD + 0.1	V
	IN-	–0.1		TBD	V
Analog Input CMRR	f_{IN} = TBD kHz		TBD		dB
Leakage Current at 25 °C	550kSPS Throughput		TBD		nA
Input Impedance			See Analog Input Section		
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1.8	µs
Throughput Rate	In Warp Mode	1		550	kSPS
Complete Cycle	In Normal Mode			2.2	µs
Throughput Rate	In Normal Mode	0		450	kSPS
Complete Cycle	In Impulse Mode			2.6	µs
Throughput Rate	In Impulse Mode	0		380	kSPS
DC ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		–3		+3	LSB[1]
Transition Noise			0.7		LSB
Gain Error[2], T_{MIN} to T_{MAX}	REF = 5 V			±TBD	% of FSR
Gain Error Temperature Drift			±TBD		ppm/°C
Offset Error[2], T_{MIN} to T_{MAX}			±TBD	±TBD	LSB
Offset Temperature Drift			±TBD		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±TBD		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = TBD kHz	88	89		dB[3]
Spurious Free Dynamic Range	f_{IN} = TBD kHz		95		dB
Total Harmonic Distortion	f_{IN} = TBD kHz		–95	TBD	dB
Signal-to-(Noise+Distortion)	f_{IN} = TBD kHz	88	89		dB
	f_{IN} = TBD kHz,–60 dB Input		29		dB
Intermodulation Distortion					
Second Order Terms			TBD		dB
Third Order Terms			TBD		dB
–3 dB Input Bandwidth			TBD		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			400	ns
REFERENCE					
External Reference Voltage Range		TBD		VDD	V
External Reference Current Drain	550kSPS Throughput		TBD		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}	OVDD = 2.7V to 5.25V	+2.0		OVDD + 0.3	V
	OVDD = 2.3V to 5.25V	+1.7		OVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA
DIGITAL OUTPUTS					
Data Format			Serial 16-Bits Straight Binary		
Pipeline Delay			Conversion Results Available Immediately After Completed Conversion		
V_{OL}	I_{SINK} = 500 µA			0.4	V
V_{OH}	I_{SOURCE} = –500 µA	OVDD – 0.3			V

NOTES

[1]LSB means Least Significant Bit. With the 5 V input range, one LSB is 76.3 µV.

[2]See Definition of Specifications section. These specifications do include full temperature range variation but do not include the error contribution from the external reference.

[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full-scale unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
VDD	Specified Performance	4.75	5	5.25	V
VDD Range		2.7		5.25	V
OVDD		2.7		5.25	V
Operating Current	550 kSPS Throughput[4]				
VDD	VDD = 5V		TBD		mA
OVDD			TBD		µA
Power Dissipation (VDD = 5V)	380 kSPS Throughput[5]		30	TBD	mW
	1 kSPS Throughput[5]		80		µW
	During acquisition phase[5]			TBD	µW
	550 kSPS Throughput[4]		TBD	TBD	mW
TEMPERATURE RANGE[6]					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[4]In Warp mode.
[5]In Impulse mode. With all digital inputs forced to OVDD or GND respectively.
[6]Contact factory for extended temperature range.
Specifications subject to change without notice.

TIMING SPECIFICATIONS (–40°C to +85°C, VDD = 4.75 V to 5.25V, OVDD = 2.7 V to 5.25 V, unless otherwise stated)

	Symbol	Min	Typ	Max	Unit
Refer to Figure 3					
Conversion Time: CNV Rising Edge to Data available (Warp mode/ Normal mode/ Impulse mode)	t_1		0.7/0.9/1.1	1.4/1.8/2.2	µs
Acquisition Time	t_2	400			ns
Time Between Conversions	t_3		1.8/2.2/2.6	Note 1	µs
CNV Pulse width	t_4	5			ns
SCK Period	t_5	20			ns
SCK Low Time	t_6	8			ns
SCK High Time	t_7	8			ns
SCK Falling Edge to Data remains Valid	t_8	5			ns
SCK Falling Edge to Data Valid delay	t_9			15	ns
CNV Low or SDI Low to SDO Valid (D15 MSB)	t_{10}			15	ns
CNV High or SDI High or 16th SCK Falling Edge to SDO High Impedance	t_{11}			15	ns
SDI valid Setup Time	t_{12}	8			ns
SDI valid Hold Time	t_{13}	0			ns

NOTES
[1]In Warp mode, the maximum time between conversion is 1ms; otherwise, there is no required maximum time.
Specifications subject to change without notice.

AD7686–SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs
IN+[2], IN-, REF, ...GND –0.3 V to VDD + 0.3 V
Supply Voltages
VDD, OVDD to GND ..... -0.3 V to 7 V
VDD to OVDD .....±7 V
Digital Inputs to GND ..... –0.3 V to OVDD + 0.3 V
Digital Outputs to GND .... –0.3 V to OVDD + 0.3 V
Internal Power Dissipation[3] ..... 325 mW
Junction Temperature ..... 150°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) ..... 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]See Analog Input section.
[3]Specification is for device in free air: μSOIC-10: θ_{JA} = 200°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7686ARM-REEL7	–40°C to +85°C	μSOIC-10	RM-10
EVAL-AD7686CB[1]		Evaluation Board	
EVAL-CONTROL BRD2[2]		Controller Board	
EVAL-CONTROL BRD3[2]		Controller Board	

NOTES
[1]This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRDx for evaluation/demonstration purposes.
[2]This board allows a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

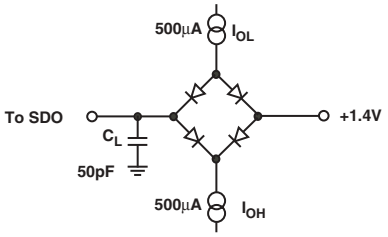


Figure 1. Load Circuit for Digital Interface Timing.

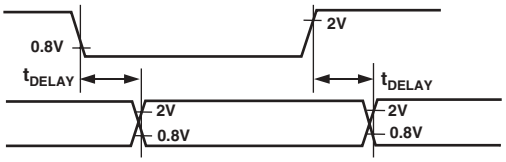
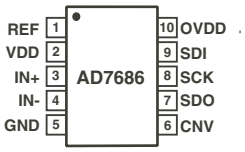


Figure 2. Voltage Reference Levels for Timing.

AD7686 PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7686 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin #	Mnemonic		Function
1	REF	AI	Reference Input Voltage. The REF range is from TBD to VDD. It is referred to the GND ground. This pin should be decoupled closely to the pin with a TBD µFcapacitor.
2	VDD	P	Input Power Supply.
3	IN+	AI	Analog Input. It is referred to IN-. The voltage difference between IN+ and IN- range is 0V to V_{REF}.
4	IN-	AI	Sense Analog Input Ground. To be connected to the analog ground plane or to a remote sense ground.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. It initiates the conversions on its leading edge. The interface mode of the part, Chain or $\overline{CS}$ mode, is selected on its leading edge. In $\overline{CS}$ mode, it can enable the serial output signals when low. In Chain mode, the data should be read while CNV is high.
7	SDO	DO	Serial Data Output. The conversion result or the programming configuration word are ouput on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: The Chain mode is selected if SDI is low on or just before the CNV rising edge. In this Chain mode, SDI could be used as a data input to daisy chain the conversion results from two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. The $\overline{CS}$ mode is selected if SDI is high on or just before the CNV rising edge. In this $\overline{CS}$ mode, either SDI or CNV can enable the serial output signals when low.
10	OVDD	P	Output Interface Digital Power. Nominally at the same supply than the host interface (2.5V, 3V or 5V).

NOTES
AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power

DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY ERROR (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale". The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

DIFFERENTIAL NONLINEARITY ERROR (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

GAIN ERROR
The last transition (from 111 . . . 10 to 111 . . . 11) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (4.999886 V for the 0 V to 5 V range). The gain error is the deviation of the actual level of the last transition from the ideal level after the offset has been adjusted out.

OFFSET ERROR
The first transition should occur at a level 1/2 LSB above analog ground (38.1 μV for the 0 V to 5 V range). The offset error is the deviation of the actual transition from that point.

SPURIOUS FREE DYNAMIC RANGE (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

EFFECTIVE NUMBER OF BITS (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to S/(N+D) by the following formula:

$$ENOB = (S/[N+D]_{dB} - 1.76)/6.02)$$

and is expressed in bits.

TOTAL HARMONIC DISTORTION (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

SIGNAL-TO-NOISE RATIO (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

SIGNAL TO (NOISE + DISTORTION) RATIO (S/[N+D])
S/(N+D) is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

APERTURE DELAY
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the CNV input to when the input signal is held for a conversion.

TRANSIENT RESPONSE
The time required for the AD7686 to achieve its rated accuracy after a full-scale step function is applied to its input.

Modes of Operation

The AD7686 features three modes of operations, Warp, Normal, and Impulse. The suitability of each mode is application dependant.

Warp mode allows the fastest conversion rate up to 550 kSPS. However, in this mode, and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the AD7686 ideal for applications where both high accuracy and fast sample rate are required.

Normal mode is the fastest mode (450 kSPS) without any conversion rate limitations. This mode makes the AD7686 ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

Impulse mode is the lowest power dissipation mode, allowing power saving between conversions. The maximum throughput in this mode is 380 kSPS. When operating at 1 kSPS, for example, it typically consumes only 80 µW. This feature makes the AD7686 ideal for battery-powered applications.

DIGITAL INTERFACE

In spite of its reduced number of pins, the AD7686 offers flexibility in its interface modes:

The AD7686, used in "$\overline{CS}$ mode", is compatible to SPI, QSPI digital hosts and DSPs (e.g.: ADSP-219x). This interface can used either 3 or 4 wires. 3 wires interface using CNV, SCK and SDO signals, minimizes wiring connections useful , for instance, in isolated applications. 4 wires interface using SDI, CNV, SCK and SDO signals allows CNV, used to initiate the conversions, to be independant of the reading timing (SDI). That is useful in, low sampling jitter or simultaneous sampling applications or applications where other SPI devices like analog multiplexers are used.

The AD7686, used in "Chain mode", provides a "daisy chain" feature using the SDI input for cascading multiple ADCs on a single data line.

The AD7686 also offers the possibility, as an option and with both modes, to force a start bit in front of the 16 data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading.

In any mode, the CNV rising edge is used as a sampling edge. It puts the track and hold in hold position and initiates the conversion process. Because the AD7686 has an on board conversion clock, the serial clock SCK is not required for the conversion process. After the conversion is complete, whatever the CNV state is, the part returns automatically in a power-down mode with the track and hold in track position.

$\overline{CS}$ MODE

The $\overline{CS}$ mode is selected if SDI is high on or just before the CNV rising edge. In $\overline{CS}$ mode, the data line SDO is in high impedance while both CNV and SDI are held high.

In this mode, the data can be read by either bringing CNV low while SDI is held high, or bringing SDI low while CNV is held high. When CNV or SDI goes low, the MSB is output on SDO. The remaining data bits are then clocked by subsequent SCK falling edges. SDO is available on both SCK edges. After the 16th SCK falling edge or CNV goes high whichever is the earliest, the SDO returns to high impedance.

Figure 3 shows a detailed timing diagram of this interface mode with a 3 wires connection (SDI tied to VDD).

Figure 4 shows a detailed timing diagram of this interface mode with a 4 wires connection (SDI is used to select the data).

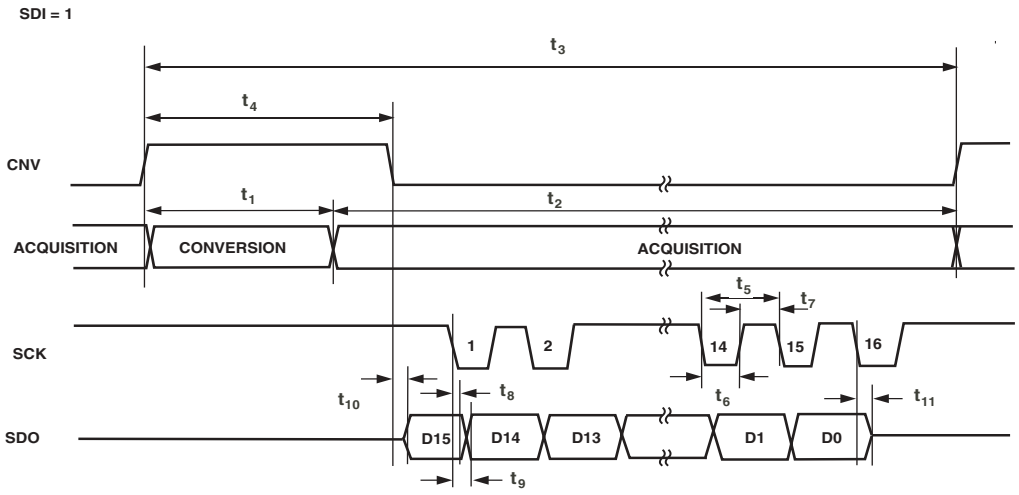


Figure 3. Serial Interface Timing ($\overline{CS}$ mode : SDI High).

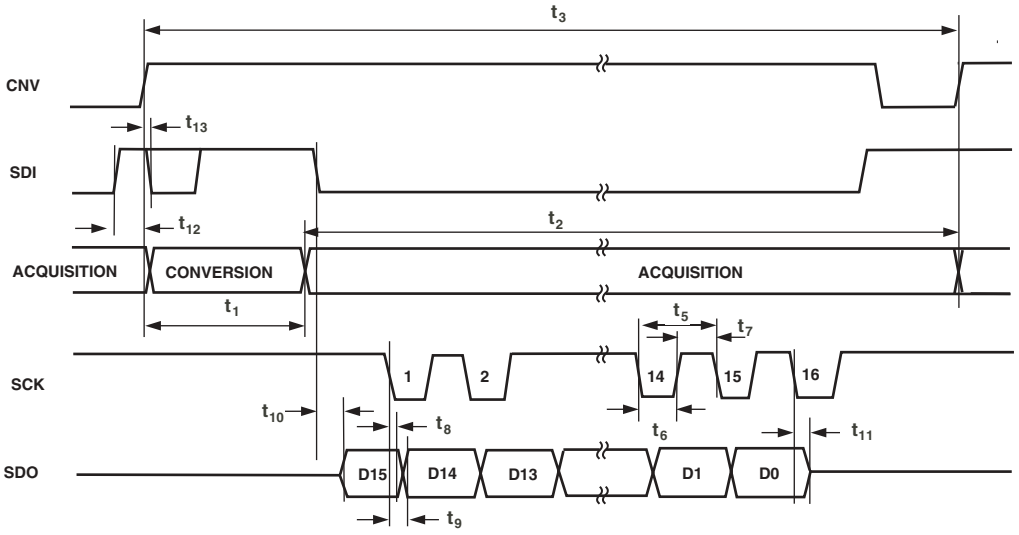


Figure 4. Serial Interface Timing ($\overline{CS}$ mode : SDI used as a $\overline{CS}$ signal).

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

10-Lead μSOIC
(RM-10)