



February 1994  
Revised March 2001

## 74LCX646

### Low Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

#### General Description

The LCX646 consists of registered bus transceiver circuits, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA) (see Functional Description).

The LCX646 is designed for low voltage (2.5V or 3.3V)  $V_{CC}$  applications with capability of interfacing to a 5V signal environment.

The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

#### Features

- 5V tolerant inputs and outputs
- 2.3V – 3.6V  $V_{CC}$  specifications provided
- 7.0 ns  $t_{PD}$  max ( $V_{CC} = 3.3V$ ), 10  $\mu A$   $I_{CC}$  max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- $\pm 24$  mA output drive ( $V_{CC} = 3.0V$ )
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

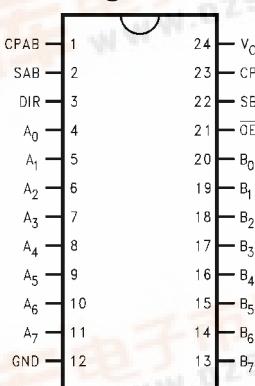
**Note 1:** To ensure the high-impedance state during power up or down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Order Number	Package Number	Package Description
74LCX646WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74LCX646MSA	MSA24	24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX646MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram

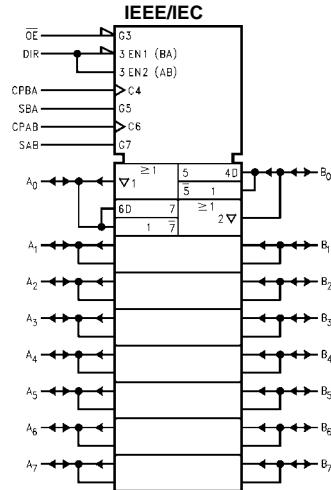
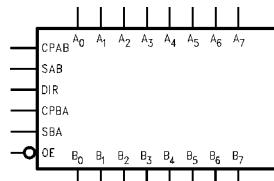


#### Pin Descriptions

Pin Names	Description
$A_0 - A_7$	Data Register A Inputs
$A_0 - A_7$	Data Register A Outputs
$B_0 - B_7$	Data Register B Inputs
$B_0 - B_7$	Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{OE}$	Output Enable Input
DIR	Direction Control Input

74LCX646 Low Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

## Logic Symbols



## Truth Table

(Note 2)

Inputs						Data I/O		Function
OE	DIR	CPAB	CPBA	SAB	SBA	A <sub>0</sub> -A <sub>7</sub>	B <sub>0</sub> -B <sub>7</sub>	
H	X	H or L	H or L	X	X			Isolation
H	X	¬	X	X	X	Input	Input	Clock A <sub>n</sub> Data into A Register
H	X	X	¬	X	X			Clock B <sub>n</sub> Data into B Register
L	H	X	X	L	X			A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode)
L	H	¬	X	L	X	Input	Output	Clock A <sub>n</sub> Data into A Register
L	H	H or L	X	H	X			A Register to B <sub>n</sub> (Stored Mode)
L	H	¬	X	H	X			Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub>
L	L	X	X	X	L			B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode)
L	L	X	¬	X	L	Output	Input	Clock B <sub>n</sub> Data into B Register
L	L	X	H or L	X	H			B Register to A <sub>n</sub> (Stored Mode)
L	L	X	¬	X	H			Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub>

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

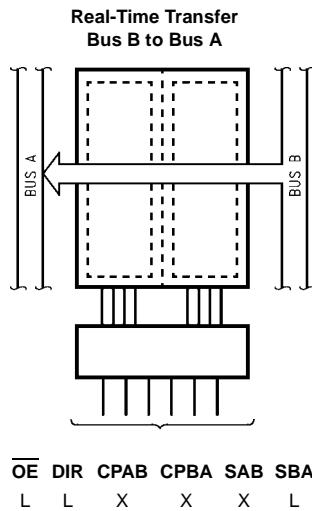
¬ = LOW-to-HIGH Transition

**Note 2:** The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

## Functional Description

In the transceiver mode, data present at the HIGH impedance port may be stored in either the A or B register or both. The select (SAB, SBA) controls can multiplex stored and real-time. The examples shown below demonstrate the four fundamental bus-management functions that can be performed.

The direction control (DIR) determines which bus will receive data when OE is LOW. In the isolation mode (OE HIGH), A data may be stored in one register and/or B data may be stored in the other register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B, may be driven at a time.



**Transfer Storage  
Data to A or B**

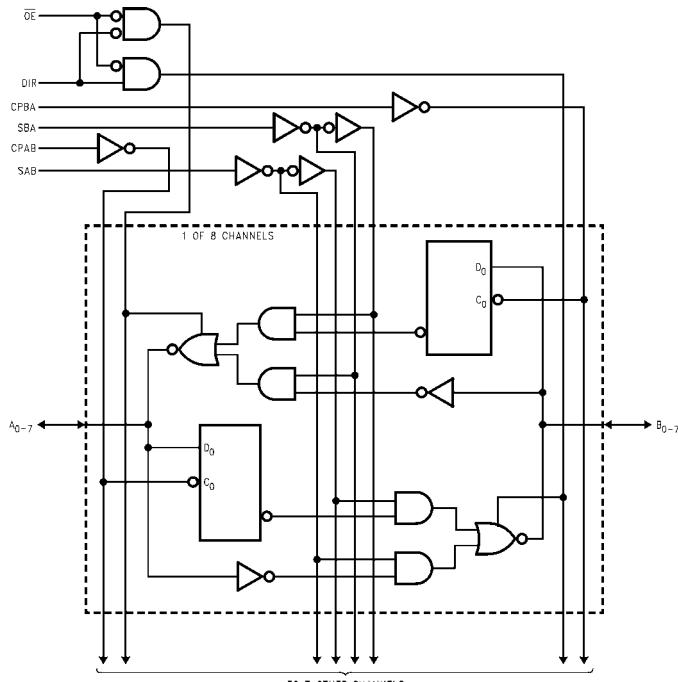
**Storage**

OE	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

**Storage**

OE	DIR	CPAB	CPBA	SAB	SBA
L	H	—	X	L	X
L	L	X	—	X	L
H	X	—	X	X	X
H	X	X	—	X	X

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 3)

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to $V_{CC}$ + 0.5	Output in HIGH or LOW State (Note 4)	
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		°C

### Recommended Operating Conditions (Note 5)

Symbol	Parameter	Operating	Min	Max	Units
		Data Retention	1.5	3.6	V
$V_I$	Input Voltage		0	5.5	V
$V_O$	Output Voltage	HIGH or LOW State	0	$V_{CC}$	V
		3-STATE	0	5.5	
$I_{OH}/I_{OL}$	Output Current	$V_{CC} = 3.0V - 3.6V$		$\pm 24$	mA
		$V_{CC} = 2.7V - 3.0V$		$\pm 12$	
		$V_{CC} = 2.3V - 2.7V$		$\pm 8$	
$T_A$	Free-Air Operating Temperature		-40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V - 2.0V$ , $V_{CC} = 3.0V$		0	10	ns/V

**Note 3:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 4:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 5:** Unused inputs or I/Os must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units
				Min	Max	
$V_{IH}$	HIGH Level Input Voltage		2.3 - 2.7	1.7		V
			2.7 - 3.6	2.0		
$V_{IL}$	LOW Level Input Voltage		2.3 - 2.7		0.7	V
			2.7 - 3.6		0.8	
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -8 mA$	2.3	1.8		
		$I_{OH} = -12 mA$	2.7	2.2		
		$I_{OH} = -18 mA$	3.0	2.4		
		$I_{OH} = -24 mA$	3.0	2.2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.3 - 3.6		0.2	V
		$I_{OL} = 8 mA$	2.3		0.6	
		$I_{OL} = 12 mA$	2.7		0.4	
		$I_{OL} = 16 mA$	3.0		0.4	
		$I_{OL} = 24 mA$	3.0		0.55	
$I_I$	Input Leakage Current	$0 \leq V_I \leq 5.5V$	2.3 - 3.6		$\pm 5.0$	μA
$I_{OZ}$	3-STATE I/O Leakage	$0 \leq V_O \leq 5.5V$ $V_I = V_{IH}$ or $V_{IL}$	2.3 - 3.6		$\pm 5.0$	μA
$I_{OFF}$	Power-Off Leakage Current	$V_I$ or $V_O = 5.5V$	0		10	μA

## DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 – 3.6		10	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V (Note 6)	2.3 – 3.6		±10	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> – 0.6V	2.3 – 3.6		500	μA

Note 6: Outputs disabled or 3-STATE only.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω						Units	
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V			
		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 50 pF		C <sub>L</sub> = 30 pF			
		Min	Max	Min	Max	Min	Max		
t <sub>MAX</sub>	Maximum Clock Frequency	150						MHz	
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Bus to Bus	1.5	7.0	1.5	8.0	1.5	8.4	ns	
		1.5	7.0	1.5	8.0	1.5	8.4		
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation Delay Clock to Bus	1.5	8.5	1.5	9.5	1.5	10.5	ns	
		1.5	8.5	1.5	9.5	1.5	10.5		
t <sub>PZL</sub> t <sub>PZH</sub>	Propagation Delay Select to Bus	1.5	8.5	1.5	9.5	1.5	10.5	ns	
		1.5	8.5	1.5	9.5	1.5	10.5		
t <sub>PZL</sub> t <sub>PHZ</sub>	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns	
		1.5	8.5	1.5	9.5	1.5	10.5		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns	
		1.5	8.5	1.5	9.5	1.5	10.5		
t <sub>S</sub>	Setup Time	2.5		2.5		4.0		ns	
t <sub>H</sub>	Hold Time	1.5		1.5		2.0		ns	
t <sub>W</sub>	Pulse Width	3.3		3.3		4.0		ns	
t <sub>OSHL</sub> t <sub>OSLH</sub>	Output to Output Skew (Note 7)		1.0					ns	
			1.0						

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Units
				Typical		
V <sub>OLP</sub>	Quiet Output Dynamic Peak V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	0.8		V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	0.6		
V <sub>OLV</sub>	Quiet Output Dynamic Valley V <sub>OL</sub>	C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3V, V <sub>IL</sub> = 0V	3.3	-0.8		V
		C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5V, V <sub>IL</sub> = 0V	2.5	-0.6		

## Capacitance

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open, V <sub>I</sub> = 0V or V <sub>CC</sub>	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 3.3V, V <sub>I</sub> = 0V or V <sub>CC</sub> , f = 10 MHz	25	pF

## AC LOADING and WAVEFORMS Generic for LCX Family

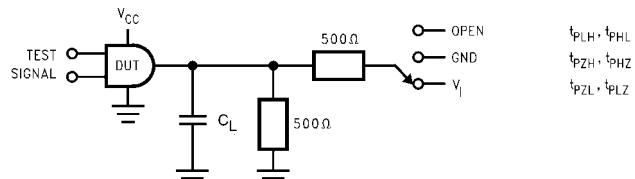
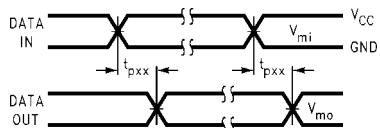
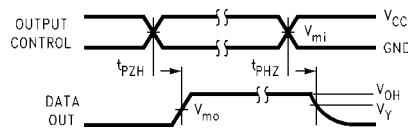


FIGURE 1. AC Test Circuit ( $C_L$  includes probe and jig capacitance)

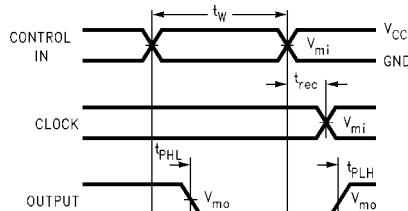
Test	Switch
$t_{PLH}, t_{PHL}$	Open
$t_{PZH}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
$t_{PZL}, t_{PHZ}$	GND



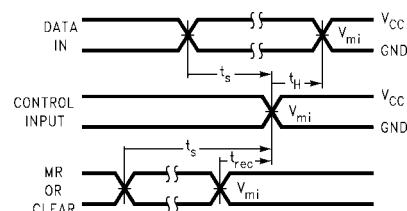
Waveform for Inverting and Non-Inverting Functions



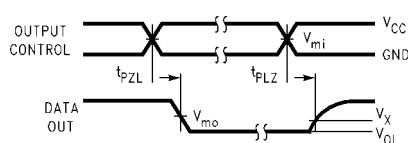
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

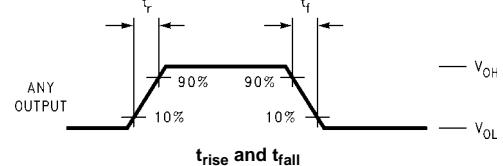
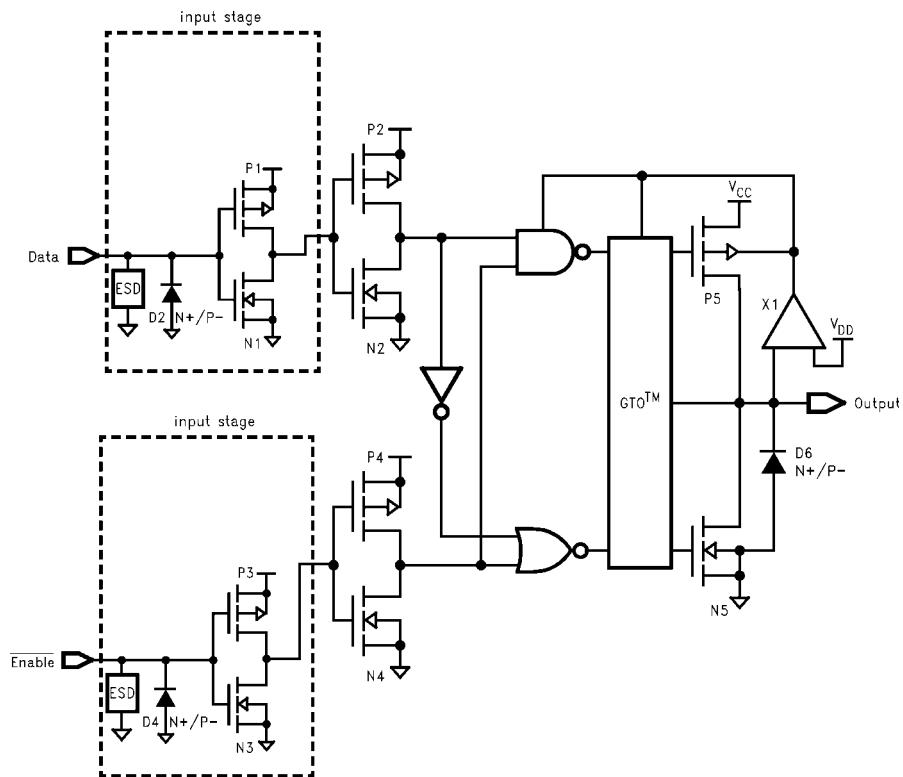


FIGURE 2. Waveforms  
(Input Characteristics;  $f = 1MHz$ ,  $t_r = t_f = 3ns$ )

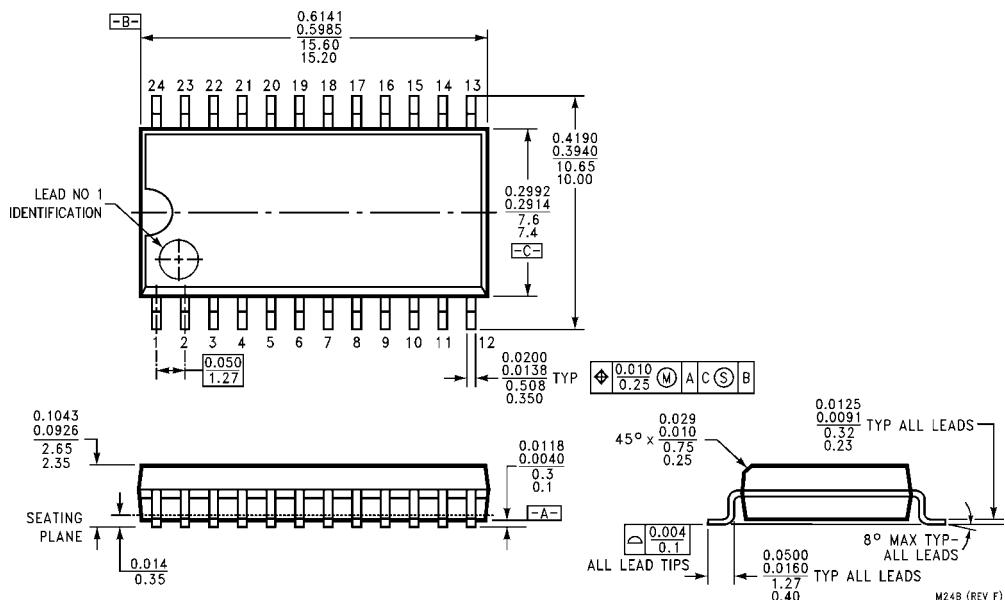
Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.7V$	$2.5V \pm 0.2V$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$
$V_x$	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
$V_y$	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

74LCX646

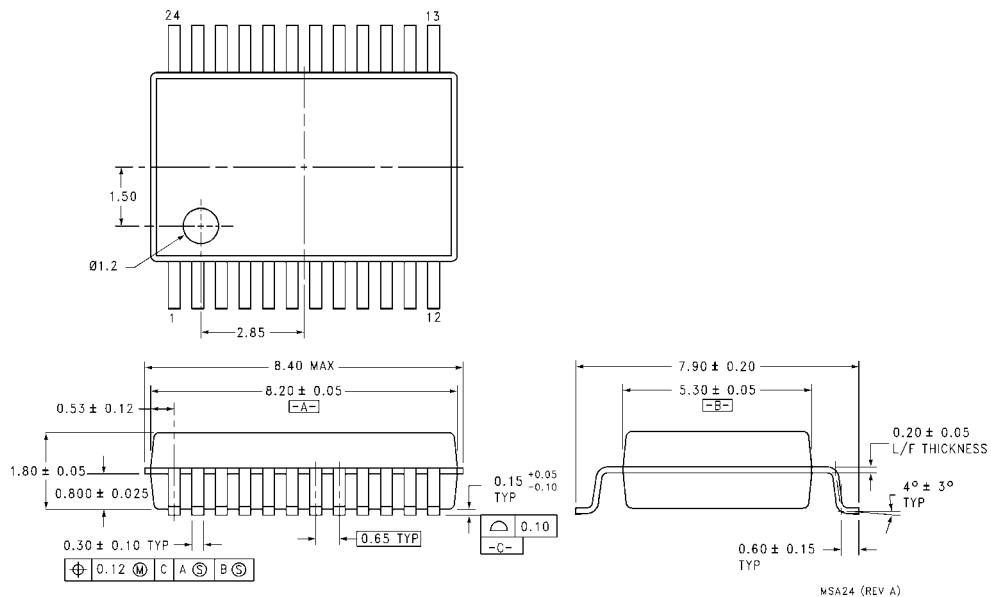
**Schematic Diagram** Generic for LCX Family



## **Physical Dimensions** inches (millimeters) unless otherwise noted

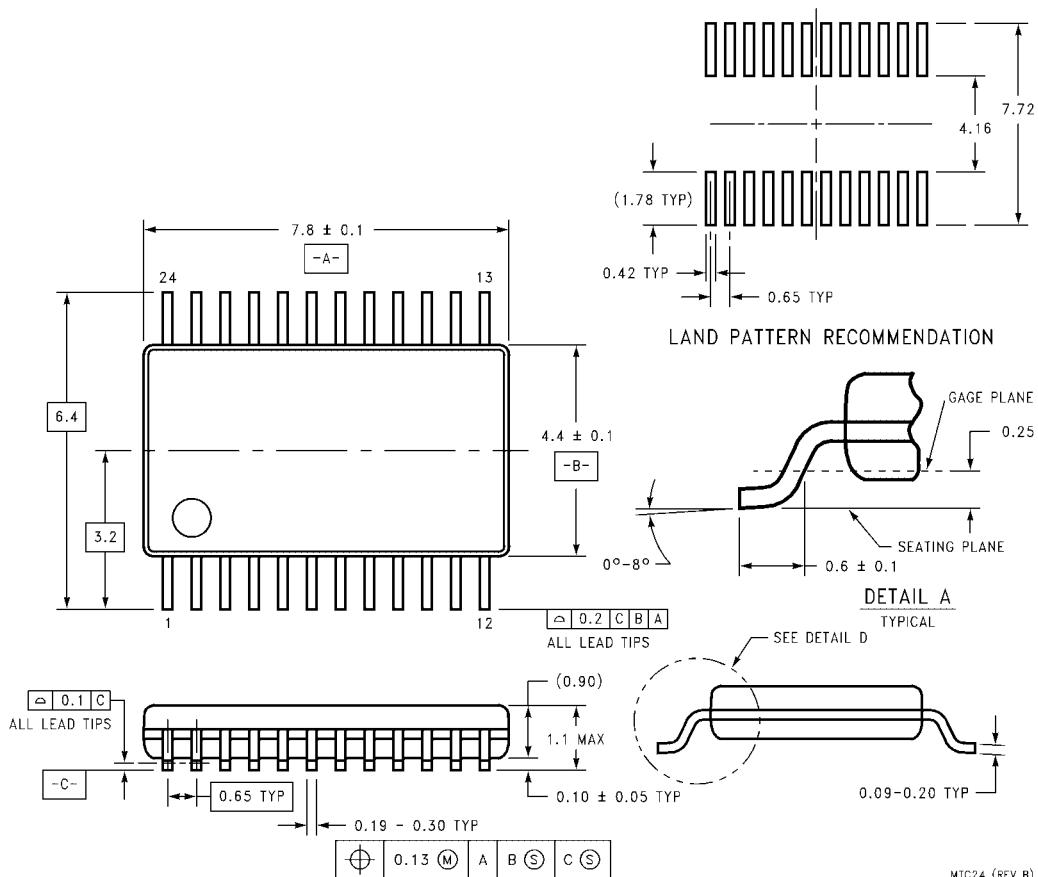


**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**



**24-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA24**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC24

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