# 2.5 V to 5.5 V, Parallel Interface Octal Voltage Output 8-/10-/12-Bit DACs

## Preliminary Technical Data — AD5346/AD5347/AD5348*

### FEATURES

AD5346: Octal 8-Bit DAC
AD5347: Octal 10-Bit DAC
AD5348: Octal 12-Bit DAC
Low Power Operation: 1.4 mA (max) @ 3 V
Power-Down to 100 nA @ 3 V, 240 nA @ 5 V
Guaranteed Monotonic by Design Over All Codes
Rail-to-Rail Output Range: 0–$V_{REF}$ or 0–2 $V_{REF}$
Power-On Reset to Zero Volts
Simultaneous Update of DAC Outputs via $\overline{LDAC}$ Pin
Asynchronous $\overline{CLR}$ Facility
Readback
Buffered/Unbuffered Reference Inputs
20ns $\overline{WR}$ time
38-lead TSSOP/6mm x 6mm 40-lead CSP Packaging
Temperature Range: –40°C to +105°C

### APPLICATIONS

Portable Battery-Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Optical Networking
Automatic Test Equipment
Mobile Communications
Programmable Attenuators
Industrial Process Control

### GENERAL DESCRIPTION

The AD5346/AD5347/AD5348 are octal 8-, 10-, and 12-bit DACs, operating from a 2.5 V to 5.5 V supply. These devices incorporate an on-chip output buffer that can drive the output to both supply rails, and also allows a choice of buffered or unbuffered reference input.

The AD5346/AD5347/AD5348 have a parallel interface. $\overline{CS}$ selects the device and data is loaded into the input registers on the rising edge of $\overline{WR}$. A readback feature allows the internal DAC registers to be read back through the digital port.

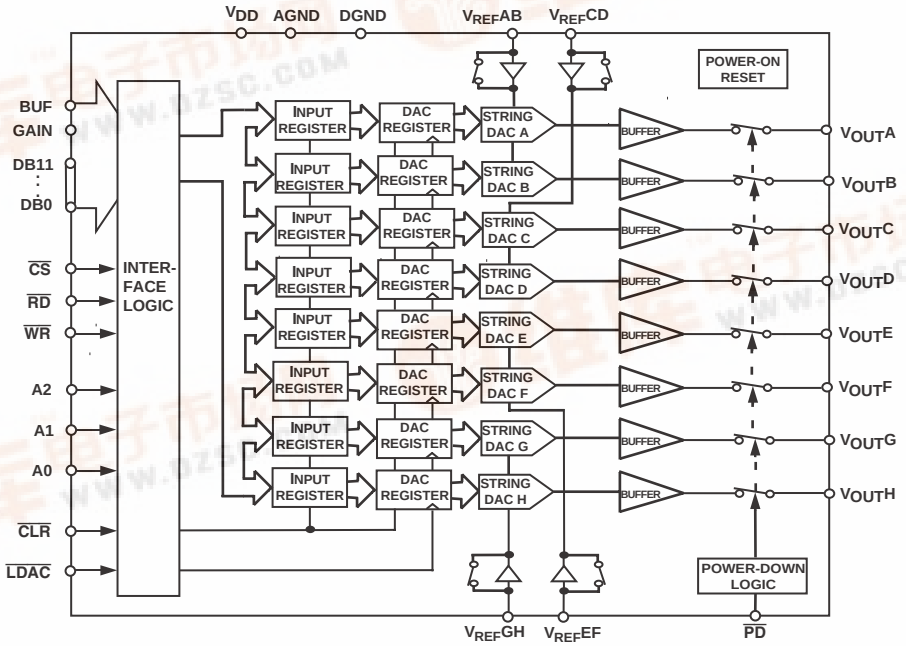
The GAIN pin on these devices allows the output range to be set at 0 V to $V_{REF}$ or 0 V to 2 x $V_{REF}$.

Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the $\overline{LDAC}$ pin.

An asynchronous $\overline{CLR}$ input is also provided, which resets the contents of the Input Register and the DAC Register to all zeros. These devices also incorporate a power-on-reset circuit that ensures that the DAC output powers on to 0 V and remains there until valid data is written to the device.

All three parts are pin-compatible, which allows the user to select the amount of resolution appropriate for their application without redesigning their circuit board.

### AD5348 FUNCTIONAL BLOCK DIAGRAM




*Protected by U.S. Patent Number 5,969,657; other patents pending.

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# AD5346/AD5347/AD5348–SPECIFICATIONS

**($V_{DD}$ = 2.5 V to 5.5 V, $V_{REF}$ = 2 V. $R_L$ = 2 kΩ to GND; $C_L$ =200 pF to GND; all specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)**

| Parameter[1] | B Version[2] Min | Typ | Max | Unit | Conditions/Comments |
|---|---|---|---|---|---|
| DC PERFORMANCE[3,4] | | | | | |
| AD5346 | | | | | |
| Resolution | | 8 | | Bits | |
| Relative Accuracy | | ±0.15 | ±1 | LSB | |
| Differential Nonlinearity | | ±0.02 | ±0.25 | LSB | Guaranteed Monotonic By Design Over All Codes |
| AD5347 | | | | | |
| Resolution | | 10 | | Bits | |
| Relative Accuracy | | ±0.5 | ±4 | LSB | |
| Differential Nonlinearity | | ±0.05 | ±0.5 | LSB | Guaranteed Monotonic By Design Over All Codes |
| AD5348 | | | | | |
| Resolution | | 12 | | Bits | |
| Relative Accuracy | | ±2 | ±16 | LSB | |
| Differential Nonlinearity | | ±0.2 | ±1 | LSB | Guaranteed Monotonic By Design Over All Codes |
| Offset Error | | ±0.4 | ±3 | % of FSR | |
| Gain Error | | ±0.1 | ±1 | % of FSR | |
| Lower Deadband[5] | | 10 | 60 | mV | Lower Deadband Exists Only if Offset Error Is Negative |
| Upper Deadband | | 10 | 60 | mV | $V_{DD}$ = 5 V. Upper Deadband Exists Only if $V_{REF} = V_{DD}$ |
| Offset Error Drift[6] | | –12 | | ppm of FSR/°C | |
| Gain Error Drift[6] | | –5 | | ppm of FSR/°C | |
| DC Power Supply Rejection Ratio[6] | | –60 | | dB | $\Delta V_{DD}$ = ±10% |
| DC Crosstalk[6] | | 200 | | µV | $R_L$ = 2 kΩ to GND, 2 kΩ to $V_{DD}$; $C_L$ = 200 pF to GND; Gain = 1 |
| DAC REFERENCE INPUT[6] | | | | | |
| $V_{REF}$ Input Range | 1 | | $V_{DD}$ | V | Buffered Reference Mode |
| $V_{REF}$ Input Range | 0.25 | | $V_{DD}$ | V | Unbuffered Reference Mode |
| $V_{REF}$ Input Impedance | | >10 | | MΩ | Buffered Reference Mode and Power-Down Mode |
| | | 90 | | kΩ | Gain = 1. Input Impedance = $R_{DAC}$ |
| | | 45 | | kΩ | Gain = 2. Input Impedance = $R_{DAC}$ |
| Reference Feedthrough | | –90 | | dB | Frequency = 10 kHz |
| Channel-to-Channel Isolation | | –75 | | dB | Frequency = 10 kHz |
| OUTPUT CHARACTERISTICS[6] | | | | | |
| Minimum Output Voltage[4,7] | | 0.001 | | V min | Rail-to-Rail Operation |
| Maximum Output Voltage[4,7] | | $V_{DD}$ – 0.001 | | V max | |
| DC Output Impedance | | 0.5 | | Ω | |
| Short Circuit Current | | 25 | | mA | $V_{DD}$ = 5 V |
| | | 16 | | mA | $V_{DD}$ = 3 V |
| Power-Up Time | | 2.5 | | µs | Coming Out of Power-Down Mode. $V_{DD}$ = 5 V |
| | | 5 | | µs | Coming Out of Power-Down Mode. $V_{DD}$ = 3 V |
| LOGIC INPUTS[6] | | | | | |
| Input Current | | | ±1 | µA | |
| $V_{IL}$, Input Low Voltage | | | 0.8 | V | $V_{DD}$ = 5 V ± 10% |
| | | | 0.8 | V | $V_{DD}$ = 3 V ± 10% |
| | | | 0.7 | V | $V_{DD}$ = 2.5 V |
| $V_{IH}$, Input High Voltage | 1.7 | | | V | $V_{DD}$ = 2.5 V to 5.5 V |
| Pin Capacitance | | 3 | | pF | |
| LOGIC OUTPUTS[6] | | | | | |
| $V_{DD}$ = 4.5 V to 5.5 V | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 2 mA |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ –1 | | | V | $I_{SOURCE}$ = 2 mA |
| $V_{DD}$ = 2.5 V to 3.6 V | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 2 mA |
| Output High Voltage, $V_{OH}$ | $V_{DD}$ –0.5 | | | V | $I_{SOURCE}$ = 2 mA |
| POWER REQUIREMENTS | | | | | |
| $V_{DD}$ | 2.5 | | 5.5 | V | |
| $I_{DD}$ (Normal Mode) | | | | | $V_{IH} = V_{DD}$, $V_{IL}$ = GND |
| $V_{DD}$ = 4.5 V to 5.5 V | | 1 | 1.8 | mA | All DACs in Unbuffered Mode. In Buffered Mode, |
| $V_{DD}$ = 2.5 V to 3.6 V | | 0.8 | 1.5 | mA | extra current is typically x µA per DAC where x = 5 µA + $V_{REF}/R_{DAC}$. |
| $I_{DD}$ (Power-Down Mode) | | | | | $V_{IH} = V_{DD}$, $V_{IL}$ = GND |
| $V_{DD}$ = 4.5 V to 5.5 V | | 0.4 | 1 | µA | |
| $V_{DD}$ = 2.5 V to 3.6 V | | 0.12 | 1 | µA | |

NOTES
[1]See Terminology section.
[2]Temperature range: B Version: –40°C to +105°C; typical specifications are at 25°C.
[3]Linearity is tested using a reduced code range: AD5346 (Code 8 to 255); AD5347 (Code 28 to 1023); AD5348 (Code 115 to 4095).
[4]DC specifications tested with outputs unloaded.
[5]This corresponds to x codes. x = Deadband voltage/LSB size.
[6]Guaranteed by design and characterisation, not production tested.
[7]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

## AC CHARACTERISTICS[1]

**($V_{DD}$ = 2.5 V to 5.5 V. $R_L$ = 2 kΩ to GND; $C_L$ = 200 pF to GND. All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)**

| Parameter[2] | B Version[3] Min | Typ | Max | Unit | Conditions/Comments |
|---|---|---|---|---|---|
| Output Voltage Settling Time | | | | | $V_{REF}$ = 2 V. See Figure 20 |
| AD5346 | | 6 | 8 | µs | 1/4 Scale to 3/4 Scale Change (40 H to C0 H) |
| AD5347 | | 7 | 9 | µs | 1/4 Scale to 3/4 Scale Change (100 H to 300 H) |
| AD5348 | | 8 | 10 | µs | 1/4 Scale to 3/4 Scale Change (400 H to C00 H) |
| Slew Rate | | 0.7 | | V/µs | |
| Major Code Transition Glitch Energy | | 8 | | nV-s | 1 LSB Change Around Major Carry |
| Digital Feedthrough | | 0.5 | | nV-s | |
| Digital Crosstalk | | 1 | | nV-s | |
| Analog Crosstalk | | 0.5 | | nV-s | |
| DAC-to-DAC Crosstalk | | 3.5 | | nV-s | |
| Multiplying Bandwidth | | 200 | | kHz | $V_{REF}$ = 2 V ± 0.1 V p-p. Unbuffered Mode |
| Total Harmonic Distortion | | –70 | | dB | $V_{REF}$ = 2.5 V ± 0.1 V p-p. Frequency = 10 kHz; Unbuffered Mode. |

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]See Terminology section.
[3]Temperature range: B Version: –40°C to +105°C; typical specifications are at 25°C.

Specifications subject to change without notice.

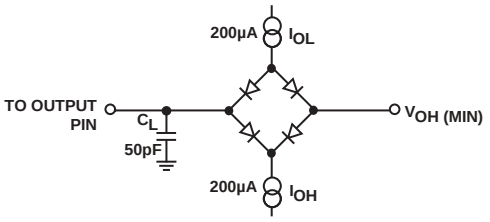



*Figure 1. Load Circuit for Digital Output Timing Specifications*

## TIMING CHARACTERISTICS[1, 2, 3] ($V_{DD}$ = 2.5 V to 5.5 V, All specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Condition/Comments |
|---|---|---|---|
| Data Write Mode (Figure 1) | | | |
| $t_1$ | 0 | ns min | $\overline{CS}$ to $\overline{WR}$ Setup Time |
| $t_2$ | 0 | ns min | $\overline{CS}$ to $\overline{WR}$ Hold Time |
| $t_3$ | 20 | ns min | $\overline{WR}$ Pulsewidth |
| $t_4$ | 5 | ns min | Data, GAIN, BUF Setup Time |
| $t_5$ | 4.5 | ns min | Data, GAIN, BUF Hold Time |
| $t_6$ | 5 | ns min | Synchronous Mode. $\overline{WR}$ Falling to $\overline{LDAC}$ Falling. |
| $t_7$ | 5 | ns min | Synchronous Mode. $\overline{LDAC}$ Falling to $\overline{WR}$ Rising. |
| $t_8$ | 4.5 | ns min | Synchronous Mode. $\overline{WR}$ Rising to LDAC Rising. |
| $t_9$ | 5 | ns min | Asynchronous Mode. $\overline{LDAC}$ Rising to $\overline{WR}$ Rising. |
| $t_{10}$ | 4.5 | ns min | Asynchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Falling. |
| $t_{11}$ | 20 | ns min | $\overline{LDAC}$ Pulsewidth |
| $t_{12}$ | 20 | ns min | $\overline{CLR}$ Pulsewidth |
| $t_{13}$ | 50 | ns min | Time Between $\overline{WR}$ Cycles |
| $t_{14}$ | 20 | ns min | A0, A1, A2 Setup Time |
| $t_{15}$ | 0 | ns min | A0, A1, A2 Hold Time |
| Data Readback Mode (Figure 2) | | | |
| $t_{16}$ | 0 | ns min | A0, A1, A2 to $\overline{CS}$ Setup Time |
| $t_{17}$ | 0 | ns min | A0, A1, A2 to $\overline{CS}$ Hold Time |
| $t_{18}$ | 0 | ns min | CS to falling edge of $\overline{RD}$ |
| $t_{19}$ | 20 | ns min | $\overline{RD}$ Pulsewidth; $V_{DD}$ = 3.6V to 5.5V |
| | 40 | ns min | $\overline{RD}$ Pulsewidth; $V_{DD}$ = 2.5V to 3.6V |
| $t_{20}$ | 0 | ns min | $\overline{CS}$ to $\overline{RD}$ Hold Time |
| $t_{21}$ | 22 | ns max | Data Access time after falling edge of $\overline{RD}$; $V_{DD}$ = 3.6V to 5.5V |
| | 35 | ns max | Data Access time after falling edge of $\overline{RD}$; $V_{DD}$ = 2.5V to 3.6V |
| $t_{22}$ | 5 | ns min | Bus Relinquish Time after rising edge of $\overline{RD}$ |
| | 30 | ns max | |
| $t_{23}$ | 22 | ns max | $\overline{CS}$ falling edge to Data; $V_{DD}$ = 3.6V to 5.5V |
| | 35 | ns max | $\overline{CS}$ falling edge to Data; $V_{DD}$ = 2.5V to 3.6V |

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of $V_{DD}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[3]See Figure 1.

Specifications subject to change without notice.

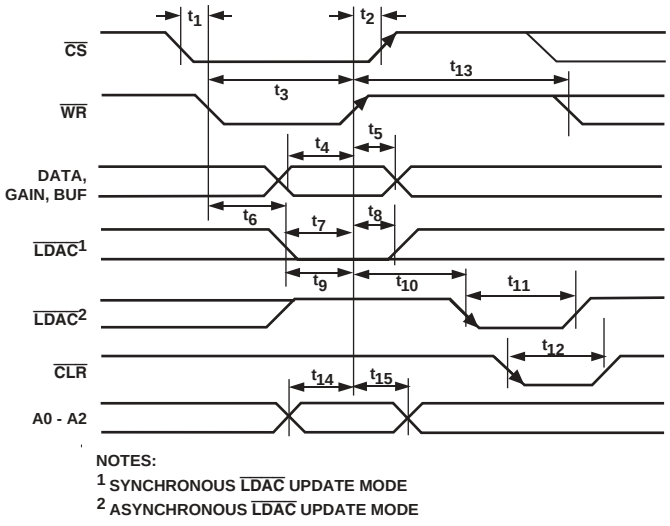



*Figure 2. Parallel Interface Write Timing Diagram*

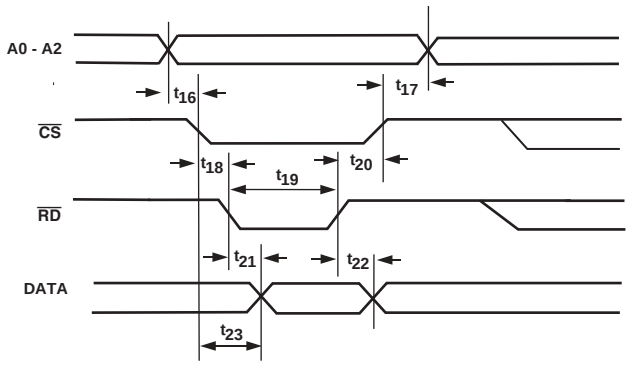



*Figure 3. Parallel Interface Read Timing Diagram*

**ABSOLUTE MAXIMUM RATINGS***
($T_A$ = 25°C unless otherwise noted)

$V_{DD}$ to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . –0.3 V to $V_{DD}$ + 0.3 V
Digital Output Voltage to GND . –0.3 V to $V_{DD}$ + 0.3 V
Reference Input Voltage to GND –0.3 V to $V_{DD}$ + 0.3 V
$V_{OUT}$ to GND . . . . . –0.3 V to $V_{DD}$ + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
38-lead TSSOP Package
Power Dissipation . . . . . ($T_J$ max – $T_A$)/$\theta_{JA}$ mW
$\theta_{JA}$ Thermal Impedance . . . . . 98.3°C/W
$\theta_{JC}$ Thermal Impedance . . . . . 8.9°C/W
40-lead CSP Package
Power Dissipation . . . . . ($T_J$ max – $T_A$)/$\theta_{JA}$ mW
$\theta_{JA}$ Thermal Impedance . . . . . 30°C/W
$\theta_{JC}$ Thermal Impedance . . . . . °C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature . . . . . +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING GUIDE**

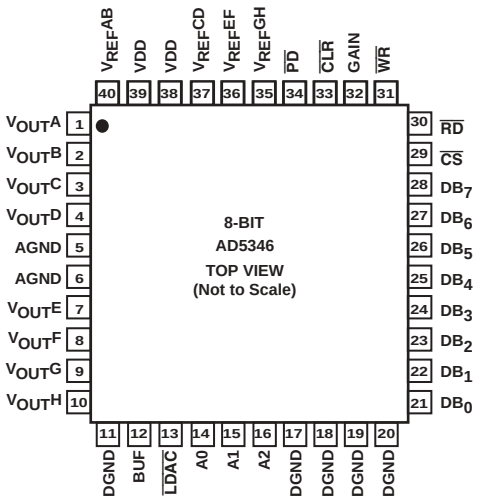
| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD5346BRU | –40°C to +105°C | TSSOP (Thin Shrink Small Outline Package) | RU-38 |
| AD5346BCP | –40°C to +105°C | CSP (Chip Scale Package) | CP-40 |
| AD5347BRU | –40°C to +105°C | TSSOP (Thin Shrink Small Outline Package) | RU-38 |
| AD5347BCP | –40°C to +105°C | CSP (Chip Scale Package) | CP-40 |
| AD5348BRU | –40°C to +105°C | TSSOP (Thin Shrink Small Outline Package) | RU-38 |
| AD5348BCP | –40°C to +105°C | CSP (Chip Scale Package) | CP-40 |

**CAUTION**

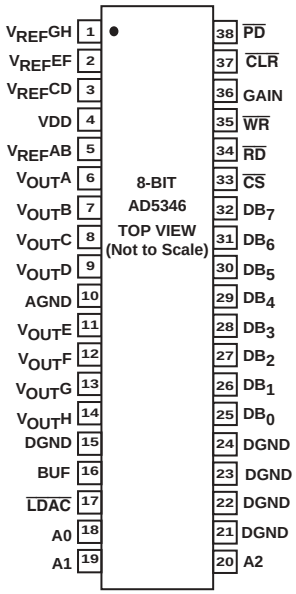
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5346/AD5347/AD5348 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## AD5346 PIN CONFIGURATIONS

**40-lead CSP Package**




**38-lead TSSOP Package**

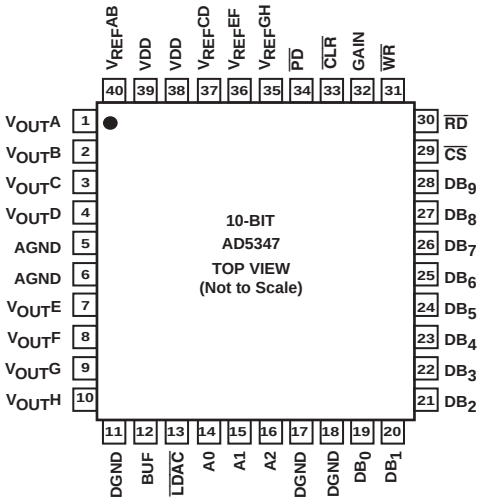



## AD5346 PIN FUNCTION DESCRIPTIONS

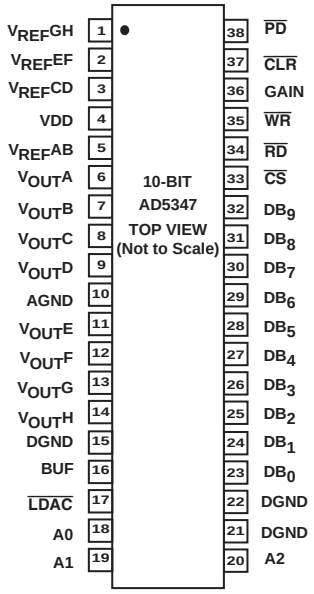
| Pin No. TSSOP | Pin No. CSP | Mnemonic | Function |
|---|---|---|---|
| 1 | 35 | $V_{REF}GH$ | Reference Input for DACs G and H. |
| 2 | 36 | $V_{REF}EF$ | Reference Input for DACs E and F. |
| 3 | 37 | $V_{REF}CD$ | Reference Input for DACs C and D. |
| 4 | 38,39 | $V_{DD}$ | Power Supply Pin(s). This part can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. Both $V_{DD}$ pins on the CSP package must be at the same potential. |
| 5 | 40 | $V_{REF}AB$ | Reference Input for DACs A and B. |
| 6-9, 11-14 | 1-4, 7-10 | $V_{OUT}X$ | Output of DAC X. Buffered Output with Rail-to-Rail Operation. |
| 10 | 5,6 | AGND | Analog Ground. Ground Reference for Analog Circuitry. |
| 15, 21-24 | 11, 17-20 | DGND | Digital Ground. Ground Reference for Digital Circuitry. |
| 16 | 12 | BUF | Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered. |
| 17 | 13 | $\overline{LDAC}$ | Active Low Control Input that Updates the DAC Registers with the Contents of the Input Registers. This allows all DAC outputs to be simultaneously updated. |
| 18 | 14 | A0 | LSB Address Pin for Selecting which DAC is to Be Written to. |
| 19 | 15 | A1 | Address Pin for Selecting which DAC is to Be Written to. |
| 20 | 16 | A2 | MSB Address Pin for Selecting which DAC is to Be Written to. |
| 25-32 | 21-28 | $DB_0$–$DB_7$ | Eight Parallel Data Inputs. $DB_7$ is the MSB of these eight bits. |
| 33 | 29 | $\overline{CS}$ | Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface, or with $\overline{RD}$ to readback data from a DAC. |
| 34 | 30 | $\overline{RD}$ | Active Low Read Input. This is used in conjunction with $\overline{CS}$ to read data back from the internal DACS. |
| 35 | 31 | $\overline{WR}$ | Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface. |
| 36 | 32 | GAIN | Gain Control Pin. This controls whether the output range from the DAC is 0–$V_{REF}$ or 0–2 $V_{REF}$. |
| 37 | 33 | $\overline{CLR}$ | Asynchronous Active Low Control Input that Clears All Input Registers and DAC Registers to Zeros. |
| 38 | 34 | $\overline{PD}$ | Power-Down Pin. This active low control pin puts all DACs into power-down mode. |

## AD5347 PIN CONFIGURATIONS

**40-lead CSP Package**




**38-lead TSSOP Package**

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| 4 | 38,39 | $V_{DD}$ | Power Supply Pin(s). This part can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. Both $V_{DD}$ pins on the CSP package must be at the same potential. |
| 5 | 40 | $V_{REF}AB$ | Reference Input for DACs A and B. |
| 6-9, 11-14 | 1-4, 7-10 | $V_{OUT}X$ | Output of DAC X. Buffered Output with Rail-to-Rail Operation. |
| 10 | 5,6 | AGND | Analog Ground. Ground Reference for Analog Circuitry. |
| 15, 21-22 | 11, 17-18 | DGND | Digital Ground. Ground Reference for Digital Circuitry. |
| 16 | 12 | BUF | Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered. |
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| 18 | 14 | A0 | LSB Address Pin for Selecting which DAC is to Be Written to. |
| 19 | 15 | A1 | Address Pin for Selecting which DAC is to Be Written to. |
| 23-32 | 19-28 | $DB_0$–$DB_9$ | Ten Parallel Data Inputs. $DB_9$ is the MSB of these ten bits. |
| 33 | 29 | $\overline{CS}$ | Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface, or with $\overline{RD}$ to readback data from a DAC. |
| 34 | 30 | $\overline{RD}$ | Active Low Read Input. This is used in conjunction with $\overline{CS}$ to read data back from the internal DACS. |
| 35 | 31 | $\overline{WR}$ | Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface. |
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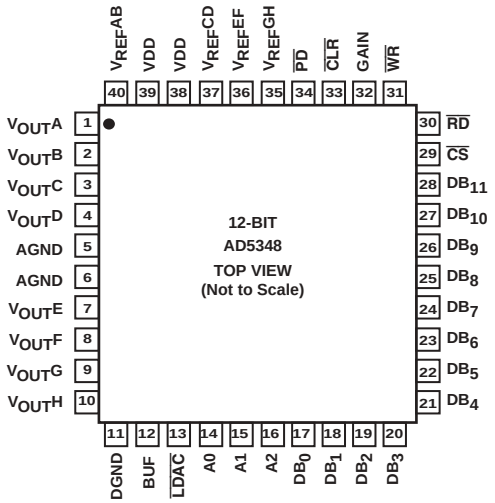
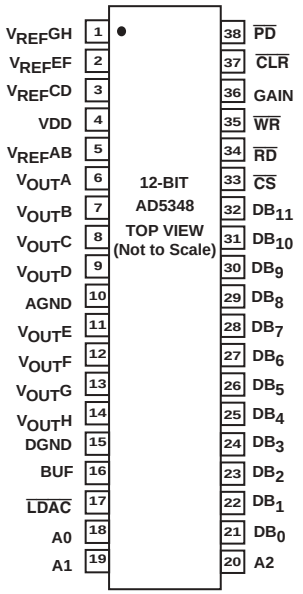



**38-lead TSSOP Package**

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| 5 | 40 | $V_{REF}AB$ | Reference Input for DACs A and B. |
| 6-9, 11-14 | 1-4, 7-10 | $V_{OUT}X$ | Output of DAC X. Buffered Output with Rail-to-Rail Operation. |
| 10 | 5,6 | AGND | Analog Ground. Ground Reference for Analog Circuitry. |
| 15 | 11 | DGND | Digital Ground. Ground Reference for Digital Circuitry. |
| 16 | 12 | BUF | Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered. |
| 17 | 13 | $\overline{LDAC}$ | Active Low Control Input that Updates the DAC Registers with the Contents of the Input Registers. This allows all DAC outputs to be simultaneously updated. |
| 18 | 14 | A0 | LSB Address Pin for Selecting which DAC is to Be Written to. |
| 19 | 15 | A1 | Address Pin for Selecting which DAC is to Be Written to. |
| 20 | 16 | A2 | MSB Address Pin for Selecting which DAC is to Be Written to. |
| 21-32 | 17-28 | $DB_0$–$DB_{11}$ | Twelve Parallel Data Inputs. $DB_{11}$ is the MSB of these twelve bits. |
| 33 | 29 | $\overline{CS}$ | Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface, or with $\overline{RD}$ to readback data from a DAC. |
| 34 | 30 | $\overline{RD}$ | Active Low Read Input. This is used in conjunction with $\overline{CS}$ to read data back from the internal DACS. |
| 35 | 31 | $\overline{WR}$ | Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface. |
| 36 | 32 | GAIN | Gain Control Pin. This controls whether the output range from the DAC is 0–$V_{REF}$ or 0–2 $V_{REF}$. |
| 37 | 33 | $\overline{CLR}$ | Asynchronous Active Low Control Input that Clears All Input Registers and DAC Registers to Zeros. |
| 38 | 34 | $\overline{PD}$ | Power-Down Pin. This active low control pin puts all DACs into power-down mode. |

## TERMINOLOGY

### RELATIVE ACCURACY

For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. Typical INL versus Code plot can be seen in TPC's 1, 2, and 3.

### DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL versus Code plot can be seen in TPC's 4, 5, and 6.

### OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

If the offset voltage is positive, the output voltage will still be positive at zero input code. This is shown in Figure 5. Because the DACs operate from a single supply, a negative offset cannot appear at the output of the buffer amplifier. Instead, there will be a code close to zero at which the amplifier output saturates (amplifier footroom). Below this code there will be a deadband over which the output voltage will not change. This is illustrated in Figure 6.

### GAIN ERROR

This is a measure of the span error of the DAC (including any error in the gain of the buffer amplifier). It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range. This is illustrated in Figure 4.

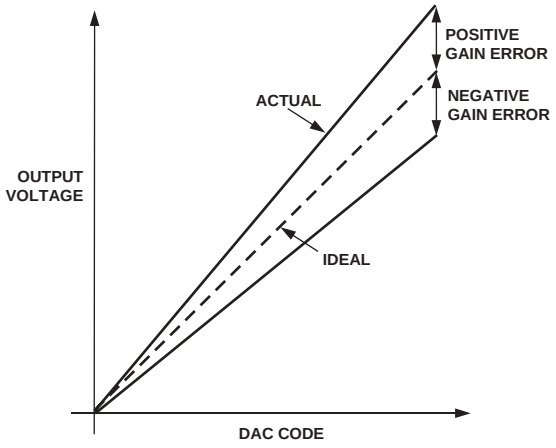



*Figure 4. Gain Error*

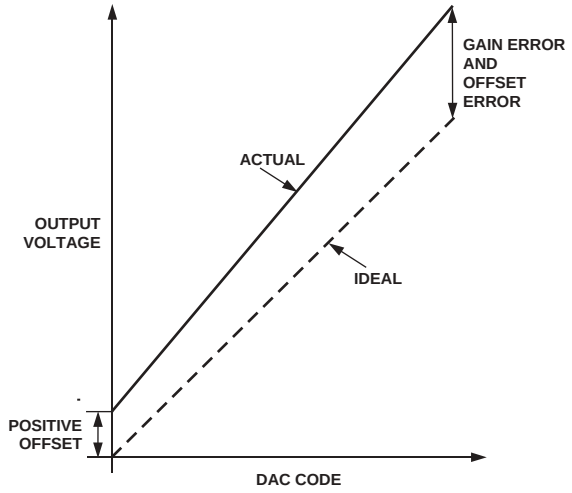



*Figure 5. Positive Offset Error and Gain Error*

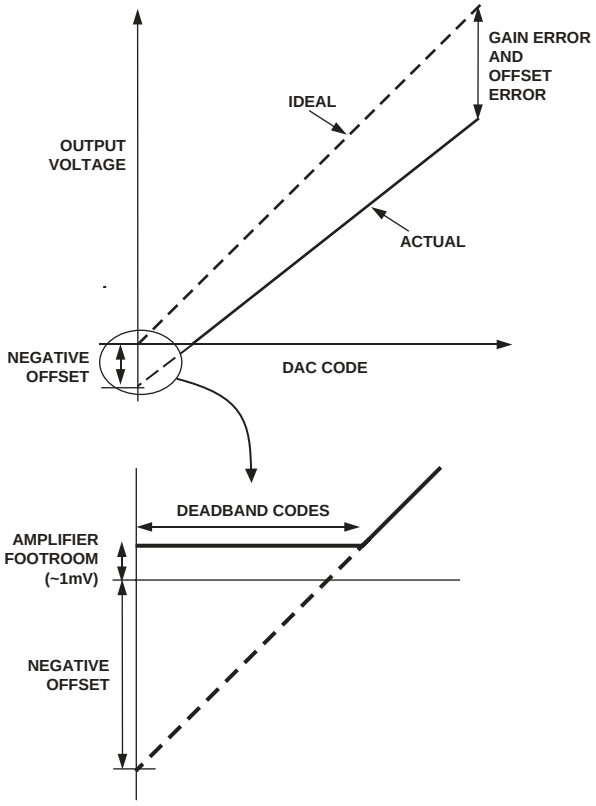



*Figure 6. Negative Offset Error and Gain Error*

**OFFSET ERROR DRIFT**
This is a measure of the change in Offset Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

**GAIN ERROR DRIFT**
This is a measure of the change in Gain Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

**DC POWER-SUPPLY REJECTION RATIO (PSRR)**
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for full-scale output of the DAC. It is measured in dBs. $V_{REF}$ is held at 2 V and $V_{DD}$ is varied ±10%.

**DC CROSSTALK**
This is the dc change in the output level of one DAC at mid-scale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in μV.

**REFERENCE FEEDTHROUGH**
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{\text{LDAC}}$ is high). It is expressed in dBs.

**CHANNEL-TO-CHANNEL ISOLATION**
This is a ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference inputs of the other DACs. It is measured by grounding one $V_{REF}$ pin and applying a 10 kHz, 4 V peak-to-peak sine wave to the other $V_{REF}$ pins. It is expressed in dBs.

**MAJOR-CODE TRANSITION GLITCH ENERGY**
Major-Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the DAC changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

**DIGITAL FEEDTHROUGH**
Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device but is measured when the DAC is not being written to ($\overline{\text{CS}}$ held high). It is specified in nV-secs and is measured with a full-scale change on the digital input pins, i.e. from all 0s to all 1s and vice versa.

**DIGITAL CROSSTALK**
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV secs.

**ANALOG CROSSTALK**
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV secs.

**DAC-TO-DAC CROSSTALK**
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with the $\overline{\text{LDAC}}$ pin set low and monitoring the output of another DAC. The energy of the glitch is expressed in nV secs.

**MULTIPLYING BANDWIDTH**
The amplifiers within the DAC have a finite bandwidth. The Multiplying Bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The Multiplying Bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

**TOTAL HARMONIC DISTORTION**
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

## FUNCTIONAL DESCRIPTION

The AD5346/AD5347/AD5348 are octal resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits, respectively. They are written to using a parallel interface. They operate from single supplies of 2.5 V to 5.5 V and the output buffer amplifiers offer rail-to-rail output swing. The gain of the buffer amplifiers can be set to 1 or 2 to give an output voltage range of 0 to $V_{REF}$ or 0 to 2 $V_{REF}$. The AD5346/AD5347/AD5348 have reference inputs that may be buffered to draw virtually no current from the reference source. The devices have a power-down feature that reduces current consumption to only 100 nA @ 3 V.

### Digital-to-Analog Section

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the $V_{REF}$ pin provides the reference voltage for the DAC. Figure 5 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \times \text{Gain}$$

where:

D = decimal equivalent of the binary code which is loaded to the DAC register:

0–255 for AD5346 (8 Bits)
0–1023 for AD5347 (10 Bits)
0–4095 for AD5348 (12 Bits)

N = DAC resolution

Gain = Output Amplifier Gain (1 or 2)

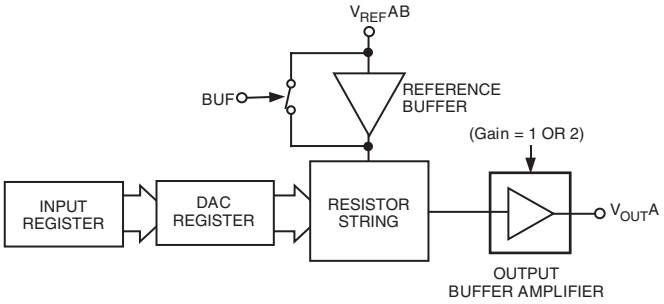



*Figure 7. Single DAC Channel Architecture*

### Resistor String

The resistor string section is shown in Figure 6. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

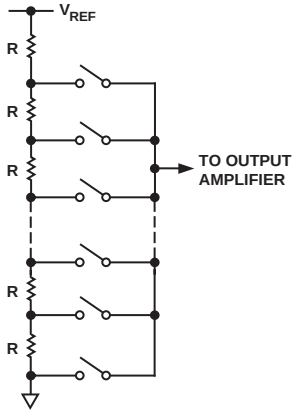



*Figure 8. Resistor String*

### DAC Reference Input

The DACs operate with an external reference. The AD5346/AD5347/AD5348 has a reference input for each pair of DACs. The reference inputs may be configured as buffered or unbuffered. This option is controlled by the BUF pin.

In buffered mode (BUF = 1) the current drawn from an external reference voltage is virtually zero, as the inpedance is at least 10 MΩ. The reference input range is 1 V to $V_{DD}$.

In unbuffered mode (BUF = 0) the user can have a reference voltage as low as 0.25 V and as high as $V_{DD}$ since there is no restriction due to headroom and footroom of the reference amplifier. The impedance is still large at typically 90 kΩ for 0–$V_{REF}$ mode and 45 kΩ for 0–2 $V_{REF}$ mode.

If using an external buffered reference (e.g. REF192) there is no need to use the on-chip buffer.

### Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on $V_{REF}$, GAIN, the load on $V_{OUT}$ and offset error.

If a gain of 1 is selected (GAIN = 0), the output range is 0.001 V to $V_{REF}$.

If a gain of 2 is selected (GAIN = 1), the output range is 0.001 V to 2 $V_{REF}$. However because of clamping the maximum output is limited to $V_{DD}$ – 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or $V_{DD}$, in parallel with 500 pF to GND or $V_{DD}$. The source and sink capabilities of the output amplifier can be seen in TPC 7.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 μs with the output unloaded. See TPC 10.

## PARALLEL INTERFACE

The AD5346, AD5347, and AD5348 load their data as a single 8-, 10-, or 12-bit word.

### Double-Buffered Interface

The AD5346/AD5347/AD5348 DACs all have double-buffered interfaces consisting of an input register and a DAC register. DAC data, BUF and GAIN inputs are written to the input register under control of the Chip Select ($\overline{CS}$) and Write ($\overline{WR}$).

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register may change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it. The gain and buffer control signals are also double-buffered and are only updated when $\overline{LDAC}$ is taken low.

This is useful if the user requires simultaneous updating of all DACs and peripherals. The user may write to all input registers individually and then, by pulsing the $\overline{LDAC}$ input low, all outputs will update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5346/AD5347/AD5348, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated. This removes unnecessary crosstalk.

**Clear Input ($\overline{CLR}$)**

$\overline{CLR}$ is an active low, asynchronous clear that resets the input and DAC registers.

**Chip Select Input ($\overline{CS}$)**

$\overline{CS}$ is an active low input that selects the device.

**Write Input ($\overline{WR}$)**

$\overline{WR}$ is an active low input that controls writing of data to the device. Data is latched into the input register on the rising edge of $\overline{WR}$.

**Read Input ($\overline{RD}$)**

$\overline{RD}$ is an active low input that controls when data is readback from the internal DAC registers. Data is latched into the input register on the rising edge of $\overline{RD}$.

**Load DAC Input ($\overline{LDAC}$)**

$\overline{LDAC}$ transfers data from the input register to the DAC register (and hence updates the outputs). Use of the $\overline{LDAC}$ function enables double buffering of the DAC data, GAIN data and BUF. There are two $\overline{LDAC}$ modes:

***Synchronous Mode:*** In this mode the DAC register is updated after new data is read in on the rising edge of the $\overline{WR}$ input. $\overline{LDAC}$ can be tied permanently low or pulsed as in Figure 1.

***Asynchronous Mode:*** In this mode the outputs are not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low the DAC register is updated with the contents of the input register.

## POWER-ON RESET

The AD5346/AD5347/AD5348 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal operation
- Reference Input Buffered
- 0 – $V_{REF}$ output range
- Output voltage set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

## POWER-DOWN MODE

The AD5346/AD5347/AD5348 have low power consumption, dissipating typically 1.5 mW with a 3 V supply and 3 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, which is selected by taking pin $\overline{PD}$ low.

When the $\overline{PD}$ pin is high, the DACs work normally with a typical power consumption of 1 mA at 5 V (0.8 mA at 3 V). In power-down mode, however, the supply current falls to 240 nA at 5 V (100 nA at 3 V) when the DACs are powered down. Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the outputs are three-state while the part is in power-down mode, and provides a defined input condition for whatever is connected to the outputs of the DAC amplifiers. The output stage is illustrated in Figure 7.

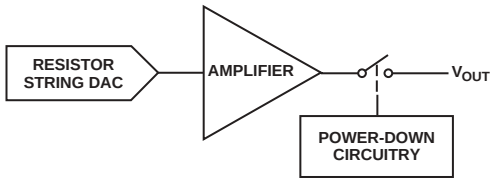



*Figure 9. Output Stage During Power-Down*

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for $V_{DD}$ = 5 V and 5 µs when $V_{DD}$ = 3 V. This is the time from a rising edge on the $\overline{PD}$ pin to when the output voltage deviates from its power-down voltage. See TPC 15 .

**Table I. AD5346/AD5347/AD5348 Truth Table**

| $\overline{CLR}$ | $\overline{LDAC}$ | $\overline{CS}$ | $\overline{WR}$ | $\overline{RD}$ | A2 | A1 | A0 | Function |
|---|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | X | X | X | X | X | No Data Transfer |
| 1 | 1 | X | 1 | 1 | X | X | X | No Data Transfer |
| 0 | X | X | X | X | X | X | X | Clear All Registers |
| 1 | 1 | 0 | 0→1 | 1 | 0 | 0 | 0 | Load DAC A Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 0 | 0 | 1 | Load DAC B Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 0 | 1 | 0 | Load DAC C Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 0 | 1 | 1 | Load DAC D Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 1 | 0 | 0 | Load DAC E Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 1 | 0 | 1 | Load DAC F Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 1 | 1 | 0 | Load DAC G Input Register |
| 1 | 1 | 0 | 0→1 | 1 | 1 | 1 | 1 | Load DAC H Input Register |
| 1 | X | 0 | 1 | 0→1 | 0 | 0 | 0 | Readback DAC Register A |
| 1 | X | 0 | 1 | 0→1 | 0 | 0 | 1 | Readback DAC Register B |
| 1 | X | 0 | 1 | 0→1 | 0 | 1 | 0 | Readback DAC Register C |
| 1 | X | 0 | 1 | 0→1 | 0 | 1 | 1 | Readback DAC Register D |
| 1 | X | 0 | 1 | 0→1 | 1 | 0 | 0 | Readback DAC Register E |
| 1 | X | 0 | 1 | 0→1 | 1 | 0 | 1 | Readback DAC Register F |
| 1 | X | 0 | 1 | 0→1 | 1 | 1 | 0 | Readback DAC Register G |
| 1 | X | 0 | 1 | 0→1 | 1 | 1 | 1 | Readback DAC Register H |
| 1 | 0 | X | X | 1 | X | X | X | Update DAC Registers |
| X | X | X | 0 | 0 | X | X | X | Invalid Operation |

X = don't care.

.

## SUGGESTED DATABUS FORMATS

In many applications the GAIN and BUF are hard-wired. However, if more flexibility is required, they can be included in a data bus. This enables the user to software program GAIN, giving the option of doubling the resolution in the lower half of the DAC range. In a bused system GAIN and BUF may be treated as data inputs since it is written to the device during a write operation and takes effect when $\overline{LDAC}$ is taken low. This means that the reference buffers and the output amplifier gain of multiple DAC devices can be controlled using common GAIN and BUF lines.

The AD5347 and AD5348 databus must be at least 10, and 12 bits wide respectively, and are best suited to a 16-bit databus system.

Examples of data formats for putting GAIN and BUF on a 16-bit databus are shown in Figure 8. Note that any unused bits above the actual DAC data may be used for GAIN and BUF.

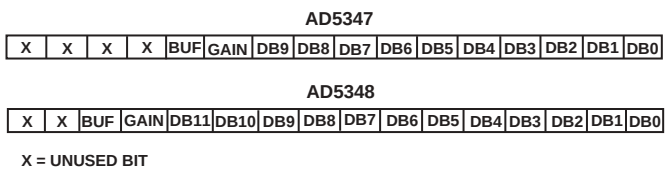



*Figure 10. AD5347/AD5348 Data Format for Word Load with GAIN and BUF Data on 16-Bit Bus*

## APPLICATIONS INFORMATION

### Typical Application Circuits

The AD5346/AD5347/AD5348 can be used with a wide range of reference voltages, especially if the reference inputs are configured as unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of 0.25 V to $V_{DD}$. More typically, these devices may be used with a fixed, precision reference voltage. Figure 11 shows a typical setup for the devices when using an external reference connected to the reference inputs. Suitable references for 5 V operation are the AD780, ADR381 and REF192 (2.5 V references). For 2.5 V operation, suitable external references would be the AD589 and the AD1580 (1.2 V bandgap references).

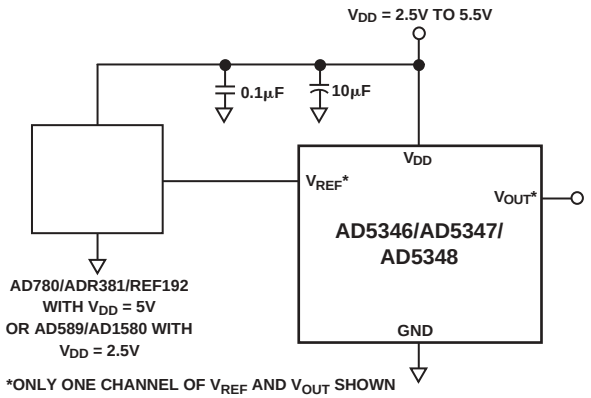



*Figure 11. AD5346/AD5347/AD5348 Using an External Reference*

**Driving $V_{DD}$ from the Reference Voltage**

If an output range of zero to $V_{DD}$ is required, the simplest solution is to connect the reference inputs to $V_{DD}$. As this supply may not be very accurate, and may be noisy, the devices may be powered from the reference voltage, for example using a 5 V reference such as the ADM663 or ADM666, as shown in Figure 12.

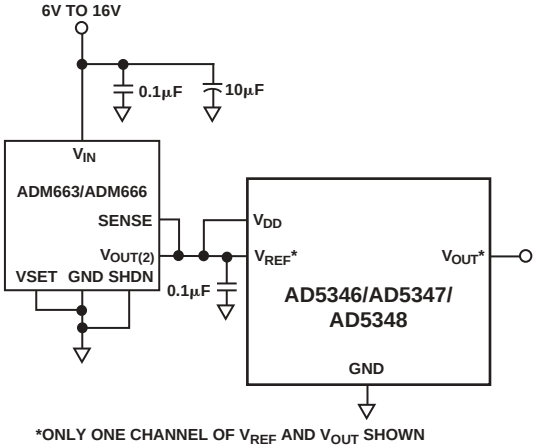



*Figure 12. Using an ADM663/ADM666 as Power and Reference to the AD5346/AD5347/AD5348*

**Bipolar Operation Using the AD5346/AD5347/AD5348**

The AD5346/AD5347/AD5348 have been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 13. This circuit will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820, the AD8519 or an OP196 as the output amplifier.

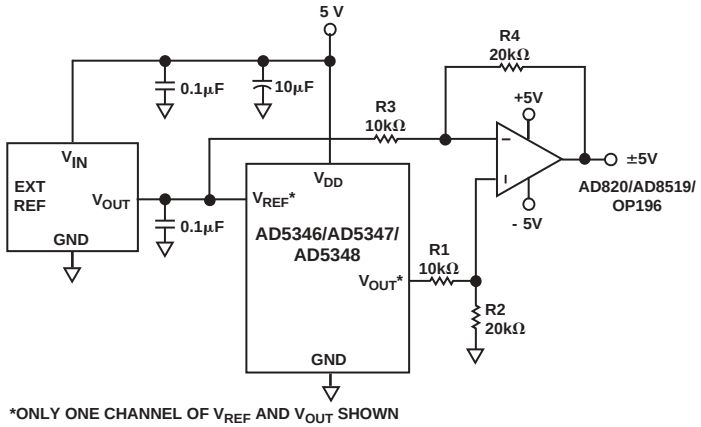



*Figure 13. Bipolar operation with the AD5346/AD5347/AD5348*

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = [(REFIN \times D/2^N) \times (R1 + R2)/R1 - REFIN \times (R2/R1)]$$

where:

D is the decimal equivalent of the code loaded to the DAC.

N is the DAC resolution.

REFIN is the reference voltage input.

With REFIN = 5 V, R1 = R2 = 10 kΩ:

$$V_{OUT} = (10 \times D/2^N) - 5\ V$$

**Decoding Multiple AD5346/AD5347/AD5348**

The $\overline{CS}$ pin on these devices can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same data and $\overline{WR}$ pulses, but only the $\overline{CS}$ to one of the DACs will be active at any one time, so data will only be written to the DAC whose $\overline{CS}$ is low.

The 74HC139 is used as a 2- to 4-line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 14 shows a diagram of a typical setup for decoding multiple devices in a system. Once data has been written sequentially to all DACs in a system, all the DACs can be updated simultaneously using a common $\overline{LDAC}$ line. A common $\overline{CLR}$ line can also be used to reset all DAC outputs to zero.

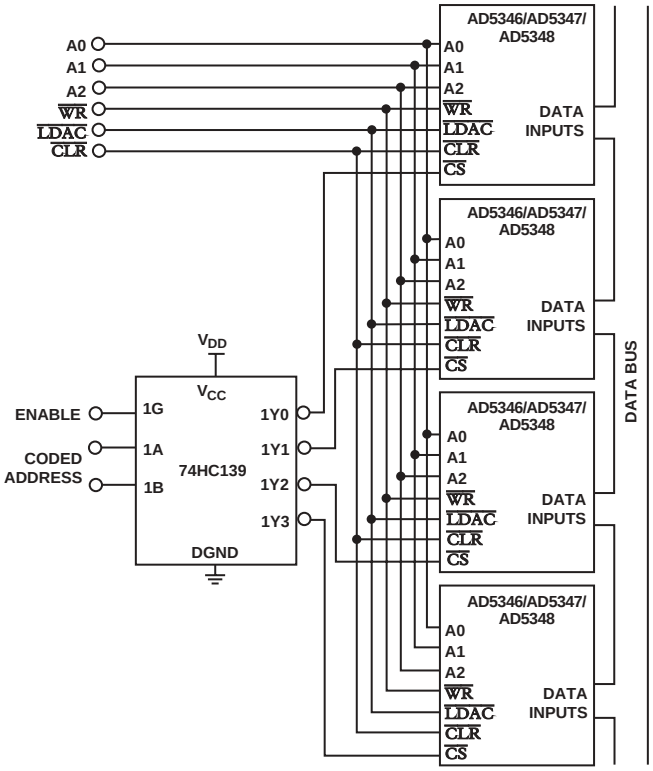



*Figure 14. Decoding Multiple DAC Devices*

**AD5334/AD5335/AD5336/AD5344 as a Digitally Programmable Window Detector**

A digitally programmable upper/lower limit detector using two of the DACs in the AD5346/AD5347/AD5348 is shown in Figure 15. Any pair of DACs in the device may be used, but for simplicity the description will refer to DACs A and B.

The upper and lower limits for the test are loaded to DACs A and B which, in turn, set the limits on the CMP04. If a signal at the $V_{IN}$ input is not within the programmed window, an LED will indicate the fail condition.

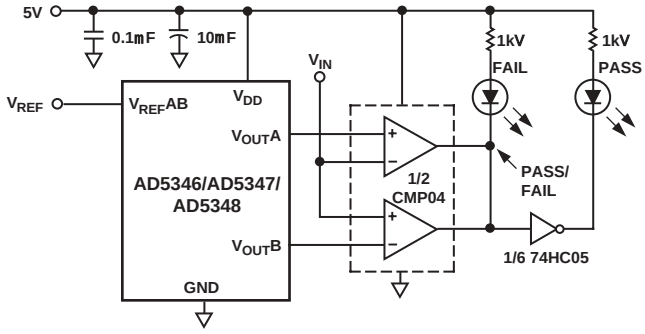



*Figure 15. Programmable Window Detector*

**Programmable Current Source**

Figure 16 shows the AD5346/AD5347/AD5348 used as the control element of a programmable current source. In this example, the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the 470 Ω adjustment potentiometer, which gives an adjustment of about ±5%. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum $V_{SOURCE}$ of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both having rail-to-rail operation on their outputs. The current for any digital input code and resistor value can be calculated as follows:

$$I = G \times V_{REF} \times \frac{D}{(2^N \times R)} \text{ mA}$$

Where:

*G* is the gain of the buffer amplifier (1 or 2)
*D* is the digital input code
*N* is the DAC resolution (8, 10, or 12 bits)
R is the sum of the resistor plus adjustment potentiometer in kΩ

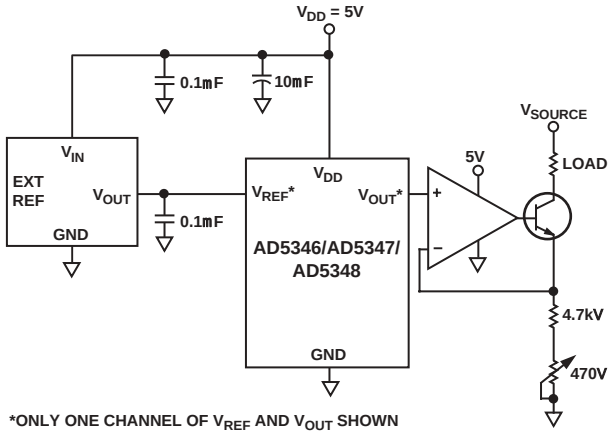



*Figure 16. Programmable Current Source*

**Coarse and Fine Adjustment Using the AD5346/AD5347/AD5348**

Two of the DACs in the AD5346/AD5347/AD5348 can be paired together to form a coarse and fine adjustment function, as shown in Figure 17. As with the window comparator previously described, the description will refer to DACs A and B.

DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 will change the relative effect of the coarse and fine adjustments. With the resistor values shown the output amplifier has unity gain for the DAC A output, so the output range is zero to ($V_{REF}$ – 1 LSB). For DAC B the amplifier has a gain of 7.6 x $10^{-3}$, giving DAC B a range equal to 2 LSBs of DAC A.

The circuit is shown with a 2.5 V reference, but reference voltages up to $V_{DD}$ may be used. The op amps indicated will allow a rail-to-rail output swing.

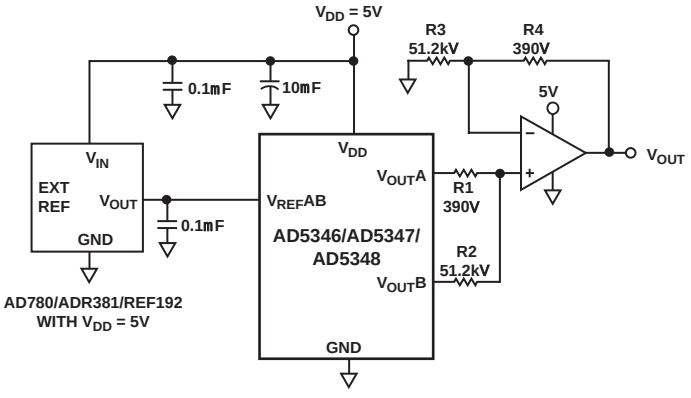



*Figure 17. Coarse and Fine Adjustment*

**Power Supply Bypassing and Grounding**

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance.

The printed circuit board on which the AD5346/AD5347/AD5348 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined in one place. If the AD5346/AD5347/AD5348 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD5346/AD5347/AD5348. If the AD5346/AD5347/AD5348 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD5346/AD5347/AD5348.

The AD5346/AD5347/AD5348 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on the supply located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

**Table III. Overview of AD53xx Parallel Devices**

| Part No. | Resolution | DNL | $V_{REF}$ Pins | Settling Time | Additional Pin Functions | | | | Package | Pins |
|---|---|---|---|---|---|---|---|---|---|---|
| **SINGLES** | | | | | **BUF** | **GAIN** | **HBEN** | **CLR** | | |
| AD5330 | 8 | ±0.25 | 1 | 6 µs | 3 | 3 | | 3 | TSSOP | 20 |
| AD5331 | 10 | ±0.5 | 1 | 7 µs | | 3 | | 3 | TSSOP | 20 |
| AD5340 | 12 | ±1.0 | 1 | 8 µs | 3 | 3 | | 3 | TSSOP | 24 |
| AD5341 | 12 | ±1.0 | 1 | 8 µs | 3 | 3 | 3 | 3 | TSSOP | 20 |
| **DUALS** | | | | | | | | | | |
| AD5332 | 8 | ±0.25 | 2 | 6 µs | | | | 3 | TSSOP | 20 |
| AD5333 | 10 | ±0.5 | 2 | 7 µs | 3 | 3 | | 3 | TSSOP | 24 |
| AD5342 | 12 | ±1.0 | 2 | 8 µs | 3 | 3 | | 3 | TSSOP | 28 |
| AD5343 | 12 | ±1.0 | 1 | 8 µs | | | 3 | 3 | TSSOP | 20 |
| **QUADS** | | | | | | | | | | |
| AD5334 | 8 | ±0.25 | 2 | 6 µs | | 3 | | 3 | TSSOP | 24 |
| AD5335 | 10 | ±0.5 | 2 | 7 µs | | | 3 | 3 | TSSOP | 24 |
| AD5336 | 10 | ±0.5 | 4 | 7 µs | | 3 | | 3 | TSSOP | 28 |
| AD5344 | 12 | ±1.0 | 4 | 8 µs | | | | | TSSOP | 28 |
| **OCTALS** | | | | | | | | | | |
| AD5346 | 8 | ±0.25 | 4 | 6 µs | 3 | 3 | | 3 | TSSOP, CSP | 38, 40 |
| AD5347 | 10 | ±0.5 | 4 | 7 µs | 3 | 3 | | 3 | TSSOP, CSP | 38, 40 |
| AD4348 | 12 | ±1.0 | 4 | 8 µs | 3 | 3 | | 3 | TSSOP, CSP | 38, 40 |

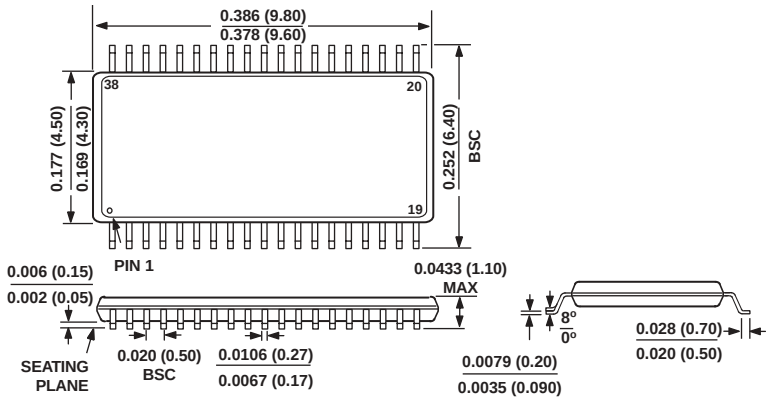
**Table IV. Overview of AD53xx Serial Devices**

| Part No. | Resolution | DNL | VREF Pins | Settling Time | Interface | Package | Pins |
|---|---|---|---|---|---|---|---|
| **SINGLES** | | | | | | | |
| AD5300 | 8 | ±0.25 | 0 (Vref = VDD) | 4 µs | SPI | SOT-23, MicroSOIC | 6, 8 |
| AD5310 | 10 | ±0.5 | 0 (Vref = VDD) | 6 µs | SPI | SOT-23, MicroSOIC | 6, 8 |
| AD5320 | 12 | ±1.0 | 0 (Vref = VDD) | 8 µs | SPI | SOT-23, MicroSOIC | 6, 8 |
| AD5301 | 8 | ±0.25 | 0 (Vref = VDD) | 6 µs | 2-Wire | SOT-23, MicroSOIC | 6, 8 |
| AD5311 | 10 | ±0.5 | 0 (Vref = VDD) | 7 µs | 2-Wire | SOT-23, MicroSOIC | 6, 8 |
| AD5321 | 12 | ±1.0 | 0 (Vref = VDD) | 8 µs | 2-Wire | SOT-23, MicroSOIC | 6, 8 |
| **DUALS** | | | | | | | |
| AD5302 | 8 | ±0.25 | 2 | 6 µs | SPI | MicroSOIC | 8 |
| AD5312 | 10 | ±0.5 | 2 | 7 µs | SPI | MicroSOIC | 8 |
| AD5322 | 12 | ±1.0 | 2 | 8 µs | SPI | MicroSOIC | 8 |
| AD5303 | 8 | ±0.25 | 2 | 6 µs | SPI | TSSOP | 16 |
| AD5313 | 10 | ±0.5 | 2 | 7 µs | SPI | TSSOP | 16 |
| AD5323 | 12 | ±1.0 | 2 | 8 µs | SPI | TSSOP | 16 |
| **QUADS** | | | | | | | |
| AD5304 | 8 | ±0.25 | 1 | 6 µs | SPI | MicroSOIC | 10 |
| AD5314 | 10 | ±0.5 | 1 | 7 µs | SPI | MicroSOIC | 10 |
| AD5324 | 12 | ±1.0 | 1 | 8 µs | SPI | MicroSOIC | 10 |
| AD5305 | 8 | ±0.25 | 1 | 6 µs | 2-Wire | MicroSOIC | 10 |
| AD5315 | 10 | ±0.5 | 1 | 7 µs | 2-Wire | MicroSOIC | 10 |
| AD5325 | 12 | ±1.0 | 1 | 8 µs | 2-Wire | MicroSOIC | 10 |
| AD5306 | 8 | ±0.25 | 4 | 6 µs | 2-Wire | TSSOP | 16 |
| AD5316 | 10 | ±0.5 | 4 | 7 µs | 2-Wire | TSSOP | 16 |
| AD5326 | 12 | ±1.0 | 4 | 8 µs | 2-Wire | TSSOP | 16 |
| AD5307 | 8 | ±0.25 | 2 | 6 µs | SPI | TSSOP | 16 |
| AD5317 | 10 | ±0.5 | 2 | 7 µs | SPI | TSSOP | 16 |
| AD5327 | 12 | ±1.0 | 2 | 8 µs | SPI | TSSOP | 16 |
| **OCTALS** | | | | | | | |
| AD5308 | 8 | ±0.25 | 2 | 6 µs | SPI | TSSOP | 16 |
| AD5318 | 10 | ±0.5 | 2 | 7 µs | SPI | TSSOP | 16 |
| AD5328 | 12 | ±1.0 | 2 | 8 µs | SPI | TSSOP | 16 |

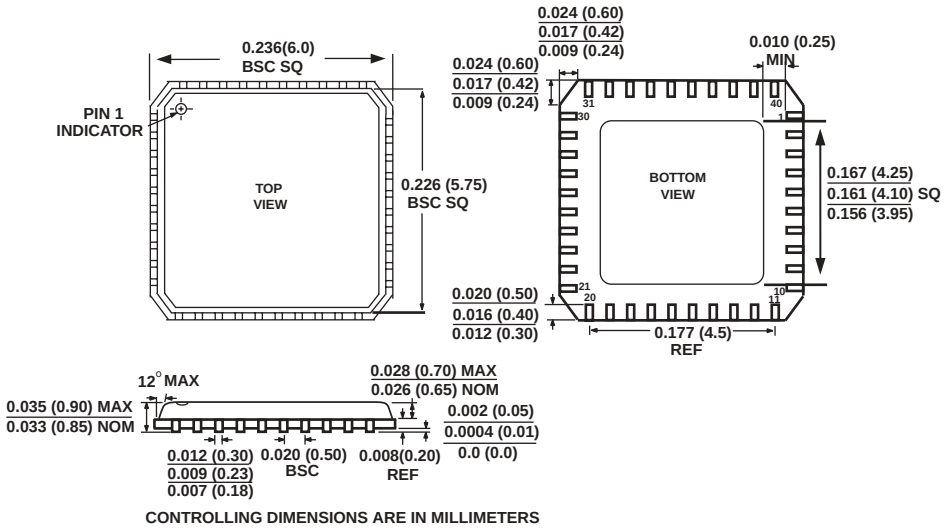
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 38-Lead Thin Shrink Small Outline Package TSSOP (RU-38)




### 40-Lead Chip Scale Package CSP (CP-40)




CONTROLLING DIMENSIONS ARE IN MILLIMETERS