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SEMICONDUCTOR™

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## CD4016BC Quad Bilateral Switch

### General Description

The CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BC.

### Features

- Wide supply voltage range: 3V to 15V
- Wide range of digital and analog switching:  $\pm 7.5 V_{PEAK}$
- "ON" Resistance for 15V operation: 400 $\Omega$  (typ)
- Matched "ON" Resistance over 15V signal input:  
 $\Delta R_{ON} = 10\Omega$  (typ)
- High degree of linearity:  
0.4% distortion (typ)  
@  $f_{IS} = 1 \text{ kHz}$ ,  $V_{IS} = 5 V_{P-P}$ ,  
 $V_{DD} - V_{SS} = 10V$ ,  $R_L = 10 \text{ k}\Omega$
- Extremely low "OFF" switch leakage:  
0.1 nA (typ.)  
@  $V_{DD} - V_{SS} = 10V$   
 $T_A = 25^\circ\text{C}$

- Extremely high control input impedance:  $10^{12}\Omega$  (typ)
- Low crosstalk between switches:  
-50 dB (typ.)  
@  $f_{IS} = 0.9 \text{ MHz}$ ,  $R_L = 1 \text{ k}\Omega$
- Frequency response, switch "ON": 40 MHz (typ)

### Applications

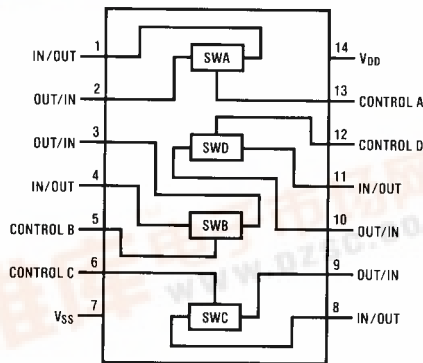
- Analog signal switching/multiplexing  
Signal gating  
Squelch control  
Chopper  
Modulator/Demodulator  
Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

### Ordering Code:

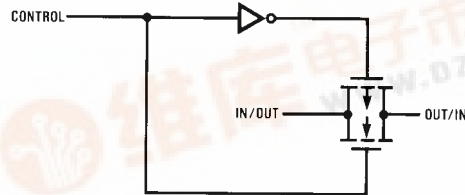
Order Number	Package Number	Package Description
CD4016BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4016BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

### Connection Diagram



### Schematic Diagram



CD4016BC Quad Bilateral Switch



**Absolute Maximum Ratings** (Note 1)

(Note 2)

$V_{DD}$ Supply Voltage	-0.5V to +18V
$V_{IN}$ Input Voltage	-0.5V to $V_{DD} + 0.5V$
$T_S$ Storage Temperature Range	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

$V_{DD}$ Supply Voltage	3V to 15V
$V_{IN}$ Input Voltage	0V to $V_{DD}$
$T_A$ Operating Temperature Range	-55°C to +125°C

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**DC Electrical Characteristics** (Note 2)

Symbol	Parameter	Conditions	-55°C		25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		0.25		0.01	0.25		7.5	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		0.5		0.01	0.5		15	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		1.0		0.01	1.0		30	$\mu A$
<b>Signal Inputs and Outputs</b>										
$R_{ON}$	"ON" Resistance	$R_L = 10k\Omega$ to $(V_{DD} - V_{SS})/2$ $V_C = V_{DD}, V_{IS} = V_{SS}$ or $V_{DD}$ $V_{DD} = 10V$		600		250	660		960	$\Omega$
		$V_{DD} = 15V$		360		200	400		600	$\Omega$
		$R_L = 10k\Omega$ to $(V_{DD} - V_{SS})/2$ $V_C = V_{DD}$ $V_{DD} = 10V, V_{IS} = 4.75$ to $5.25V$ $V_{DD} = 15V, V_{IS} = 7.25$ to $7.75V$		1870		850	2000		2600	$\Omega$
				775		400	850		1230	$\Omega$
$\Delta R_{ON}$	$\Delta$ "ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L = 10k\Omega$ to $(V_{DD} - V_{SS})/2$ $V_C = V_{DD}, V_{IS} = V_{SS}$ to $V_{DD}$ $V_{DD} = 10V$ $V_{DD} = 15V$				15 10				$\Omega$ $\Omega$
$I_{IS}$	Input or Output Leakage Switch "OFF"	$V_C = 0, V_{DD} = 15V$ $V_{IS} = 0V$ or $15V,$ $V_{OS} = 15V$ or $0V$		$\pm 50$		$\pm 0.1$	$\pm 50$		$\pm 500$	nA
<b>Control Inputs</b>										
$V_{ILC}$	LOW Level Input Voltage	$V_{IS} = V_{SS}$ and $V_{DD}$ $V_{OS} = V_{DD}$ and $V_{SS}$ $I_{IS} = \pm 10 \mu A$ $V_{DD} = 5V$		0.9			0.7		0.5	V
		$V_{DD} = 10V$		0.9			0.7		0.5	V
		$V_{DD} = 15V$		0.9			0.7		0.5	V
$V_{IHC}$	HIGH Level Input Voltage	$V_{DD} = 5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$ (Note 3) and Table 1	11.0		11.0			11.0		V
$I_{IN}$	Input Current	$V_{CC} - V_{SS} = 15V$ $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		$\pm 0.1$		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1.0$	$\mu A$

**Note 3:** If the switch input is held at  $V_{DD}$ ,  $V_{IHC}$  is the control input level that will cause the switch output to meet the standard "B" series  $V_{OH}$  and  $I_{OH}$  output levels. If the analog switch input is connected to  $V_{SS}$ ,  $V_{IHC}$  is the control input level — which allows the switch to sink standard "B" series  $|I_{OH}|$ , HIGH level current, and still maintain a  $V_{OL} \leq$  "B" series. These currents are shown in Table 1.

<b>AC Electrical Characteristics</b> (Note 4)						
$T_A = 25^\circ\text{C}$ , $t_r = t_f = 20\text{ ns}$ and $V_{SS} = 0\text{V}$ unless otherwise specified						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PHL}$ , $t_{PLH}$	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$ , $C_L = 50\text{ pF}$ , (Figure 1) $R_L = 200\text{ k}$ $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		58 27 20	100 50 40	ns ns ns
$t_{PZH}$ , $t_{PZL}$	Propagation Delay Time Control Input to Signal Output HIGH Impedance to Logical Level	$R_L = 1.0\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , (Figure 2, Figure 3) $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		20 18 17	50 40 35	ns ns ns
$t_{PHZ}$ , $t_{PLZ}$	Propagation Delay Time Control Input to Signal Output Logical Level to HIGH Impedance Sine Wave Distortion	$R_L = 1.0\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , (Figure 2, Figure 3) $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$ $V_C = V_{DD} = 5\text{V}$ , $V_{SS} = -5$ $R_L = 10\text{ k}\Omega$ , $V_{IS} = 5\text{ V}_{P-P}$ , $f = 1\text{ kHz}$ , (Figure 4)		15 11 10 0.4	40 25 22	ns ns ns %
	Frequency Response — Switch "ON" (Frequency at $-3\text{ dB}$ )	$V_C = V_{DD} = 5\text{V}$ , $V_{SS} = -5\text{V}$ , $R_L = 1\text{ k}\Omega$ , $V_{IS} = 5\text{ V}_{P-P}$ , $20\text{ Log}_{10} V_{OS}/V_{OS}$ (1 kHz) $-dB$ , (Figure 4)		40		MHz
	Feedthrough — Switch "OFF" (Frequency at $-50\text{ dB}$ )	$V_{DD} = 5\text{V}$ , $V_C = V_{SS} = -5\text{V}$ , $R_L = 1\text{ k}\Omega$ , $V_{IS} = 5\text{ V}_{P-P}$ , $20\text{ Log}_{10} (V_{OS}/V_{IS}) = -50\text{ dB}$ , (Figure 4)		1.25		MHz
	Crosstalk Between Any Two Switches (Frequency at $-50\text{ dB}$ )	$V_{DD} = V_{C(A)} = 5\text{V}$ ; $V_{SS} = V_{C(B)} = -5\text{V}$ , $R_L = 1\text{ k}\Omega$ , $V_{IS(A)} = 5\text{ V}_{P-P}$ , $20\text{ Log}_{10} (V_{OS(B)}/V_{OS(A)}) = -50\text{ dB}$ , (Figure 5)		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10\text{V}$ , $R_L = 10\text{ k}\Omega$ $R_{IN} = 1\text{ k}\Omega$ , $V_{CC} = 10\text{V}$ Square Wave, $C_L = 50\text{ pF}$ (Figure 6)		150		mV <sub>P-P</sub>
	Maximum Control Input	$R_L = 1\text{ k}\Omega$ , $C_L = 50\text{ pF}$ , (Figure 7) $V_{OS(f)} = \frac{1}{2} V_{OS}$ (1 kHz) $V_{DD} = 5\text{V}$ $V_{DD} = 10\text{V}$ $V_{DD} = 15\text{V}$		6.5 8.0 9.0		MHz MHz MHz
$C_{IS}$	Signal Input Capacitance			4		pF
$C_{OS}$	Signal Output Capacitance	$V_{DD} = 10\text{V}$		4		pF
$C_{IOS}$	Feedthrough Capacitance	$V_C = 0\text{V}$		0.2		pF
$C_{IN}$	Control Input Capacitance			5	7.5	pF
<p><b>Note 4:</b> AC Parameters are guaranteed by DC correlated testing.</p> <p><b>Note 5:</b> These devices should not be connected to circuits with the power "ON".</p> <p><b>Note 6:</b> In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in <math>C_L</math> wherever it is specified.</p> <p><b>Note 7:</b> <math>V_{IS}</math> is the voltage at the in/out pin and <math>V_{OS}</math> is the voltage at the out/in pin. <math>V_C</math> is the voltage at the control input.</p>						

AC Test Circuits and Switching Time Waveforms

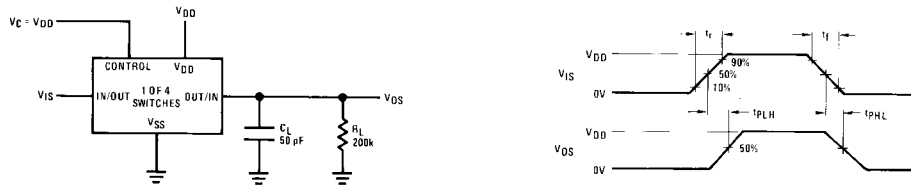


FIGURE 1.  $t_{PLH}$ ,  $t_{PLL}$  Propagation Delay Time Control to Signal Output

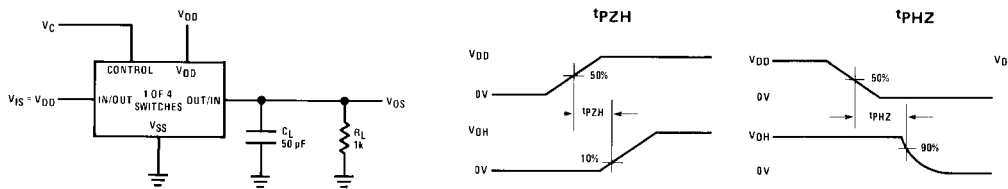


FIGURE 2.  $t_{PZH}$ ,  $t_{PHZ}$  Propagation Delay Time Control to Signal Output

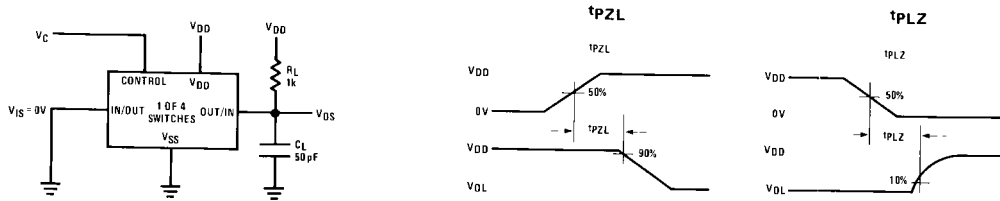
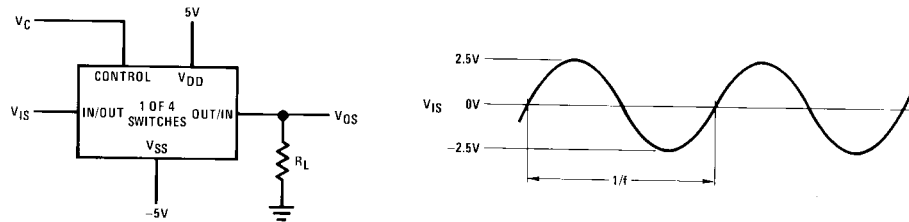


FIGURE 3.  $t_{PZL}$ ,  $t_{PLZ}$  Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$  for distortion and frequency response tests  
 $V_C = V_{SS}$  for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

AC Test Circuits and Switching Time Waveforms (Continued)

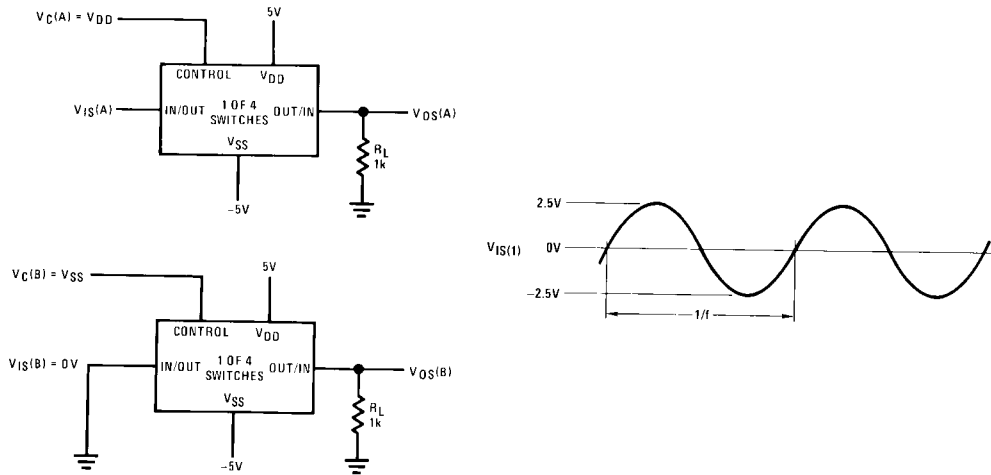


FIGURE 5. Crosstalk Between Any Two Switches

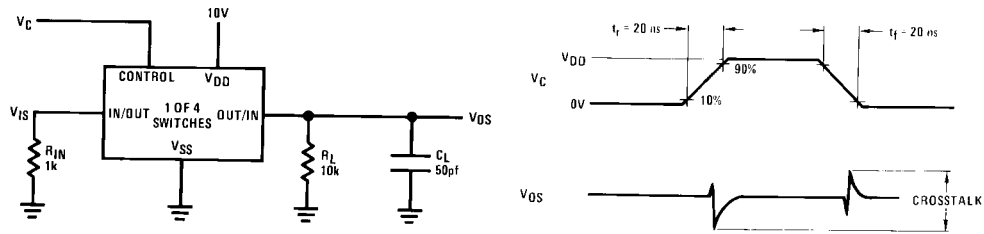


FIGURE 6. Crosstalk — Control to Input Signal Output

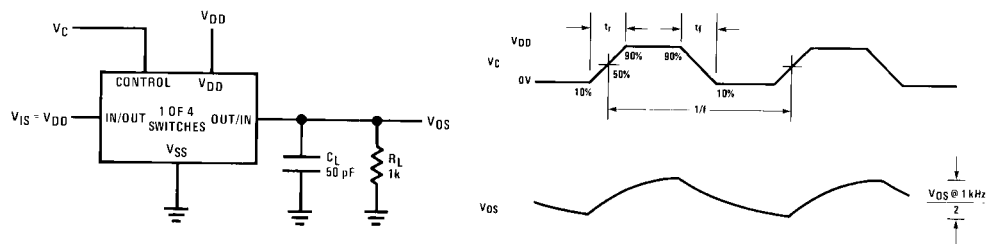


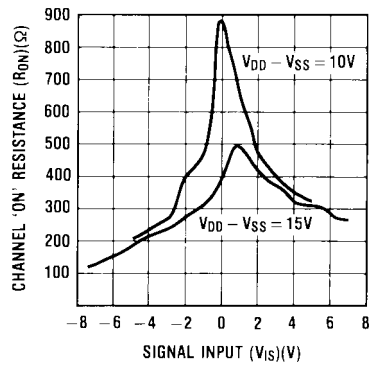
FIGURE 7. Maximum Control Input Frequency

TABLE 1. CD4016B Switch Test Conditions for  $V_{IHC}$

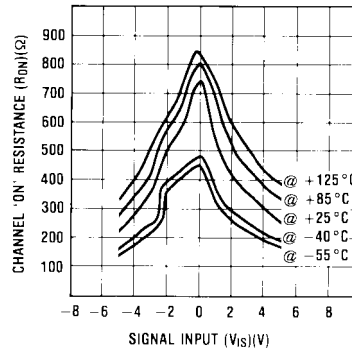
Temperature Range	$V_{DD}$	Switch Input				Switch Output	
		$V_{IS}$	$I_{IS}$ (mA)			$V_{OS}$ (V)	
			-40°C	25°C	+85°C	Min	Max
COMMERCIAL	5	0	0.2	0.16	0.12	4.6	0.4
	5	5	-0.2	-0.16	-0.12		
	10	0	0.5	0.4	0.3	9.5	0.5
	10	10	-0.5	-0.4	-0.3		
	15	0	1.4	1.2	1.0	13.5	1.5
	15	15	-1.4	-1.2	-1.0		

Typical Performance Characteristics

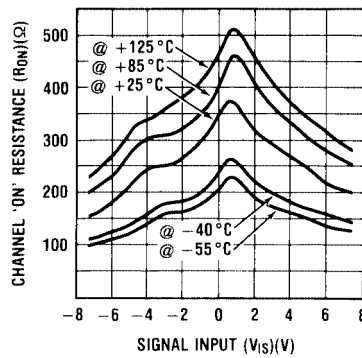
'ON' Resistance vs. Signal Voltage  $T_A = 25^\circ\text{C}$



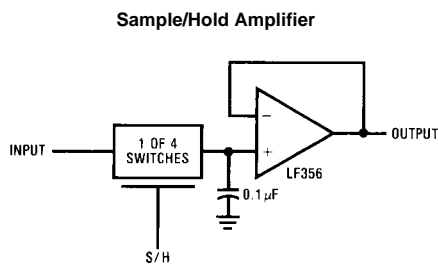
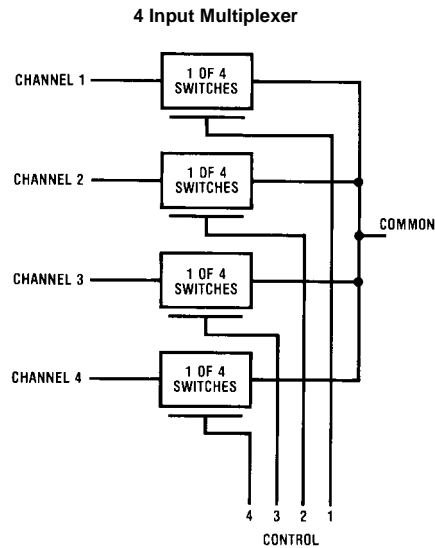
'ON' Resistance Temperature Variation for  $V_{DD} - V_{SS} = 10\text{V}$



'ON' Resistance Temperature Variation for  $V_{DD} - V_{SS} = 15\text{V}$



## Typical Applications

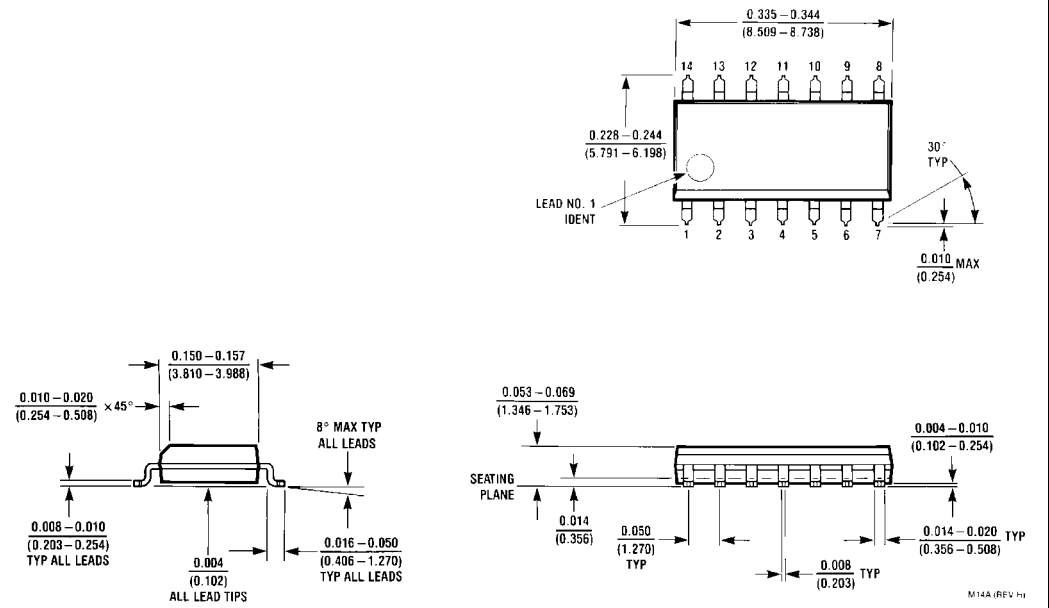


## Special Considerations

The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R<sub>ON</sub>" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages,  $\leq 5V$ , the CD4016B's On Resistance becomes

non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either  $V_{DD}$  or  $V_{SS}$ ; and that at 3V the voltages on the in/out pins should be at  $V_{DD}$  or  $V_{SS}$  for reliable operation.

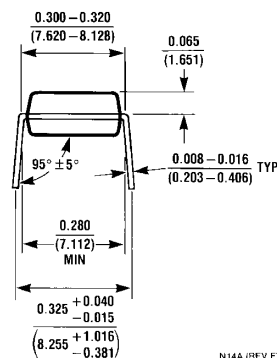
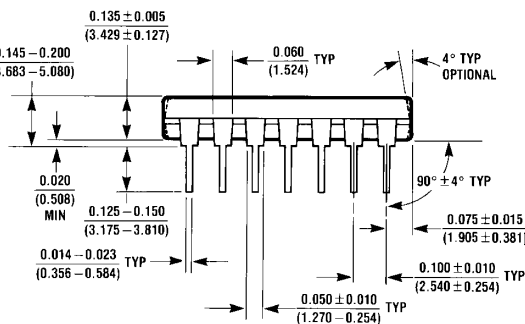
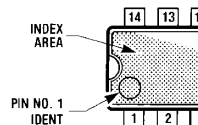
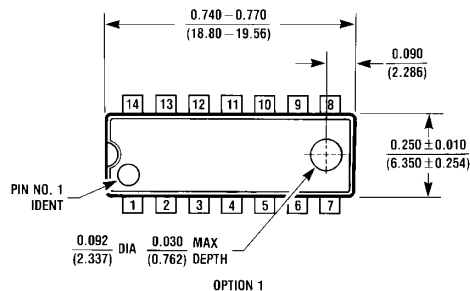
**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



N14A (REV F)

**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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