FAIRCHILD SEMICONDUCTOR™

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FC940L
Low Voltage 1 to 18 Clock Distribution Device with Selectable PECL or LVTTL Input

General Description

The FC940L is a 1 to 18 low voltage clock fanout buffer. The device allows for the selection of either differential PECL or LVTTL/CMOS input levels. The 18 outputs are compatible with LVCMOS or LVTTL technology and are capable of driving 50Ω series or parallel terminated lines. The device has a minimal propagation delay and features low part-to-part and pin-to-pin skews. The outputs of the device are designed to operate at either 2.5V or 3.3V V_{CC}. The output transistors have a 20Ω (30Ω) impedance at 3.3V (2.5V) V_{CC}. The input and core circuitry operate at 3.3V.

The FC940L is fabricated in a high performance BiCMOS Process.

Features

- Selectable Differential PECL or LVTTL/CMOS inputs
- 2.5V/3.3V output V_{CC} supply operation
- Typical propagation delays 2.5 ns
- Part-to-Part skew < 900 ps
- Typical Pin-to-Pin skew 200 ps
- Ability to drive 50Ω series or parallel terminated transmission lines
- Latchup performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V
- Pin compatible to MPC940L
- 32 pin TQFP package

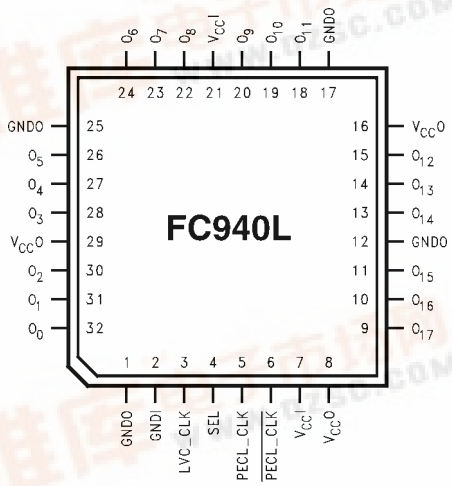
Ordering Code:

Order Number	Package Number	Package Description
FC940LVB	VBE32A	32-Lead Thin Quad Flat Package, JEDEC MO-136, 7mm Square

Device also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignment for TQFP



Pin Descriptions

Pin Names	Description
PECL_CLK, $\overline{\text{PECL\_CLK}}$	Differential PECL Input
LVC_CLK	LVTTL/CMOS Clock Input
SEL	Input Selection Pin
O[0:17]	Low Voltage CMOS Outputs

Truth Table

Inputs			Outputs
PECL_CLK	LVC_CLK	SEL	O_0–O_{17}
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

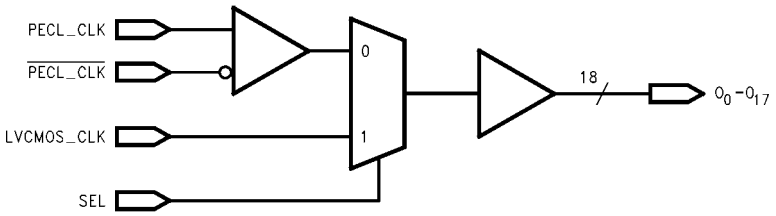
Functional Description

The FC940L is a 1 to 18 Clock distribution fanout buffer. The devices accept either a differential PECL or LVCMOS/LVTTL input signal and generates 18 LVCMOS output signals. The SEL signal selects the differential PECL CLK input signals when held at a logic “L” and selects the LVCMOS CLK input signal when held at a logic “H”. The complete functional operation is shown in the Truth Table.

The output buffers support the ability to be powered by either a 2.5V or 3.3V V_{CC}. The internal core voltage is required to be a 3.3V.

The selectable input stage allows the device to be used in combination with either LVTTL/LVCMOS or LVPECL clock generation devices. The LVPECL inputs make this device ideal for use in large clock distribution systems where there are multiple levels of hierarchy.

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +4.6V
DC Input Voltage (V_I)	–0.5V to +4.6V
Output Voltage (V_O) (Note 2)	–0.5V to V_{CC} + 0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	–50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	–50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or Ground)	±100 mA
Storage Temperature Range (T_{STG})	–65°C to + 150°C
Ambient Temperature Under Bias (T_A)	0°C to + 70°C
Case Temperature Under Bias (T_C)	0°C to + 110°C

Recommended Operating Conditions

Power Supply Voltage (V_{CC})	
V_{CC}I	3.135V to 3.465V
V_{CC}O(Note 3)	2.375 to 3.465V
Input Voltage (V_{IN})	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Output Current in I_{OH}/I_{OL}	
V_{CC}O = 3.135V to 3.465V	±24 mA
V_{CC}O = 2.375V to 2.625V	±16 mA
Free Air Operating Temperature	0°C to +70°C
Input Edge Rate (Δt/ΔV)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.135V	< 10 ns/V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Absolute Maximum Rating must be observed.

Note 3: $V_{CC}O \leq V_{CC}1$

DC Electrical Characteristics (V_{CC}I = 3.3 ± 0.165V, V_{CC}O = 3.3 ± 0.165V)

Symbol	Parameter		Conditions	V_{CC}I	V_{CC}O	T_A = 0°C to +70°C		Units
						Min	Max	
V_{IH}	High Level Input Voltage	PECLK_CLK		3.135–3.465	3.135–3.465	2.135	2.42	V
		OTHER		3.135–3.465	3.135–3.465	2.00		V
V_{IL}	Low Level Input Voltage	PECLK_CLK		3.135–3.465	3.135–3.465	1.49	1.825	V
		OTHER		3.135–3.465	3.135–3.465		0.8	V
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK		3.135–3.465	3.135–3.465	300	1000	mV
VCMR	Common Mode Range (Note 4)			3.135–3.465	3.135–3.465	V_{CC}–1.6	V_{CC}–0.8	V
V_{OH}	High Level Output Voltage		I_{OH} = –100 µA	3.135–3.465	3.135–3.465	V_{CC}–0.2		V
			I_{OH} = –24 mA	3.135	3.135	2.5		V
V_{OL}	Low Level Output Voltage		I_{OL} = 100 µA	3.135–3.465	3.465		0.2	V
			I_{OL} = 24 mA	3.135	3.135		0.5	V
I_{IN}	Input Current	PECL_CLK		3.135–3.465	3.135–3.465		100	µA
		LVC_CLK		3.135–3.465	3.135–3.465		100	µA
I_{CC}	Quiescent Supply Current (I_{CCI} + I_{CCO})		All Outputs Low (I_{CCL})	3.465	3.465		240	mA
			All Outputs High (I_{CCH})	3.465	3.465		225	mA

Note 4: VCMR is the difference between V_{CC}I and the most positive side of the differential Input signal. Normal operation is obtained when the "high" input is within the VCMR Range and the inputs swing lies within the V_{PP} specification. See figure 6.

DC Electrical Characteristics ($V_{CC}I = 3.3V \pm 0.165V$, $V_{CC}O = 2.5V \pm 0.125V$)

Symbol	Parameter		Conditions	$V_{CC}I$	$V_{CC}O$	$T_A = 0°C$ to $+70°C$		Units
						Min	Max	
V_{IH}	High Level Input Voltage	PECLK_CLK		3.135–3.465	2.375–2.625	2.135	2.42	V
		OTHER		3.135–3.465	2.375–2.625	2.0		V
V_{IL}	Low Level Input Voltage	PECLK_CLK		3.135–3.465	2.375–2.625	1.49	1.825	V
		OTHER		3.135–3.465	2.375–2.625		0.8	V
V_{PP}	Peak-to-Peak Input Voltage			3.135–3.465	2.375–2.625	300	1000	mV
VCMR	Common Mode Range (Note 4)			3.135–3.465	2.375–2.625	V_{CC}–1.6	V_{CC}–0.8	V
V_{OH}	High Level Output Voltage		$I_{OH} = -100\ \mu A$	3.135–3.405	2.375–2.625	V_{CC}–0.2		V
			$I_{OH} = -16$ mA	3.135	2.375	1.7		V
V_{OL}	Low Level Output Voltage		$I_{OL} = 100\ \mu A$	3.135–3.465	2.375–2.625		0.2	V
			$I_{OL} = 16$ mA	3.135	2.375		0.5	V
I_{IN}	Input Current	PECL_CLK		3.135–3.465	2.375–2.625		100	µA
		LVC_CLK		3.135–3.465	2.375–2.625		100	µA
I_{CC}	Quiescent Supply Current ($I_{CCI} + I_{CCO}$)		All Outputs Low (I_{CCL})	3.465	2.625		240	mA
			All Outputs High (I_{CCH})	3.465	2.625		225	mA

AC Electrical Characteristics ($V_{CC}I = 3.3V \pm 0.165V$, $T_A = 0°C$ to $+70°C$)

(Note 5)

Symbol	Parameter	$V_{CC}O = 3.3V \pm 0.165V$			$V_{CC}O = 2.5V \pm 0.125V$			Units
		Min	Typ	Max	Min	Typ	Max	
f_{max}	Clock Frequency	150			150			MHz
t_{PHL}	Propagation Delay							
t_{PLH}	PECL_CLK to O_n		2.5	3.5		2.5	3.7	ns
	LVC_CLK to O_n		2.9	3.8		2.9	4.0	
t_{PHL}	Propagation Delay			5.3			5.5	ns
t_{PLH}	SEL to O_n							
t_r	Rise and Fall Time							
t_f	$V_{CC}O = 3.3V$ (0.8V to 2V)		600					ps
	$V_{CC}O = 2.5V$ (0.7V to 1.6V)					600		
t_{OSLH}	Pin-to-Pin Output Skew		200			200		ps
t_{OSHL}	(Note 6)							
$t_{SK(PR)}$	Part-to-Part Skew (Note 7)			900			900	ps
t_{pwo}	Output Pulse Width (Note 8)	45		55	45		55	%

Note 5: AC Specifications are measured into a 50Ω Parallel terminated line. See Figure 1. Measurements are made with an input rise time of 1 ns/V.

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay between any two outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH t_{OSLH}).

Note 7: Part-to-Part Skew is defined as the variation in propagation delay between a specific output of device A and the same output of device B at the same V_{CC}, temperature, output loading and input signal conditions. This specification is valid where all outputs of the device are tied together. This specification is guaranteed by design and statistical process distribution.

Note 8: This specification assumes an input waveform with 50% duty cycle. The worst case duty cycle degradation will typically occur at f_{MAX}.

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	4	pF
C_{PD}	Power Dissipation Capacitance	V_I = 0V or V_{CC}, f= 10 MHz, V_{CC} = 3.3V	8	pF

AC Loading and Waveforms

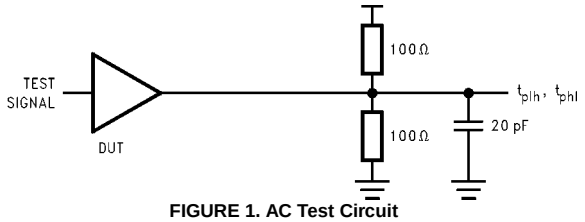


FIGURE 1. AC Test Circuit

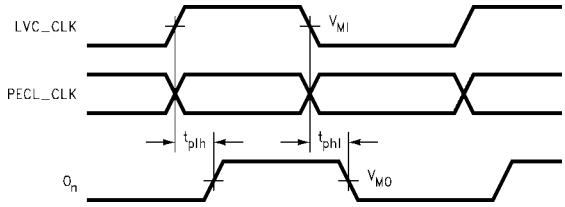


FIGURE 2. Waveform for Non-Inverting Output Signal

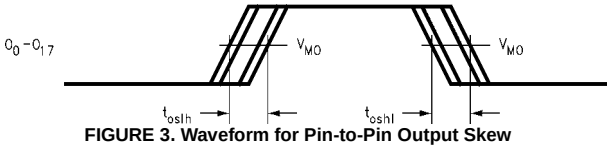


FIGURE 3. Waveform for Pin-to-Pin Output Skew

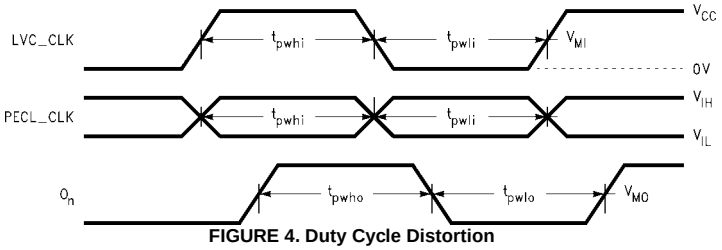


FIGURE 4. Duty Cycle Distortion
dpwh=(t_{pwho}-t_{pwhi}); dpwl=(t_{pwlo}-t_{pwli})

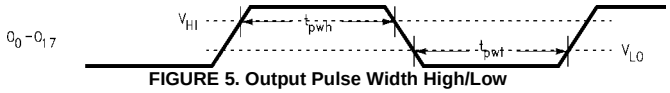


FIGURE 5. Output Pulse Width High/Low

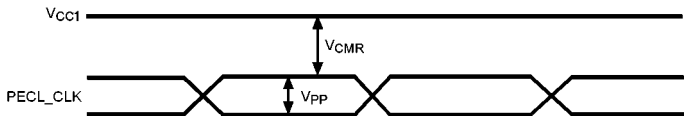
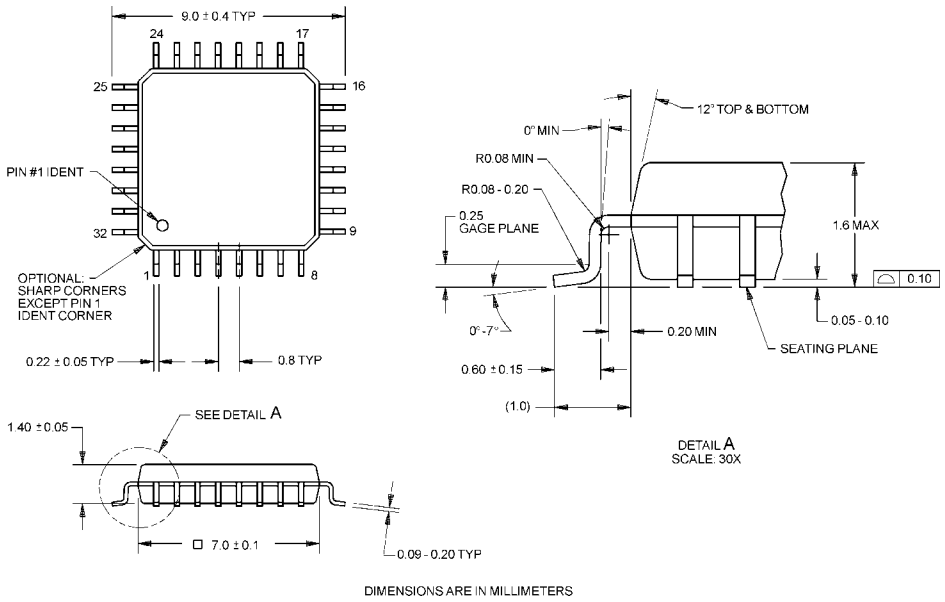


FIGURE 6. Differential Input Signals

Symbol	V_{MI}	V_{MO}	
	VCCI = 3.3V ± 0.165V	**V_{CC}O = 3.3V ± 0.165V**	**V_{CC}O = 2.5V ± 0.125V**
PECL_CLK	50% of Swing	1.5V	V_{CC}/2
LVC_CLK	1.5V	1.5V	VCC/2

Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

32-Lead Thin Quad Flat Package, JEDEC, M0-136, 7mm Square
Package Number VBE32A