

# International IOR Rectifier

Data Sheet No. PD60193

**IR21093(S)**

## HALF-BRIDGE DRIVER

### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with IN input
- Logic and power ground +/- 5V offset
- Internal 540ns dead-time
- Lower di/dt gate driver for better noise immunity

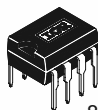
### Description

The IR21093(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

### Product Summary

$V_{\text{OFFSET}}$	600V max.
$I_{\text{O}+/-}$	120 mA / 250 mA
$V_{\text{OUT}}$	10 - 20V
$t_{\text{on/off (typ.)}}$	750 & 200 ns
Dead Time	540 ns

### Packages

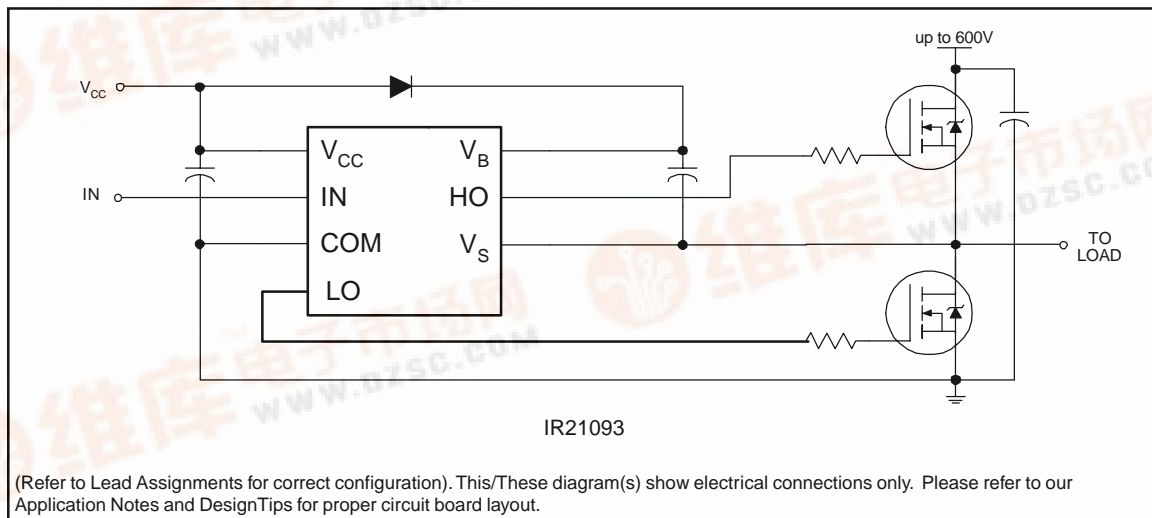


8-Lead PDIP



8-Lead SOIC

### Typical Connection



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## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating absolute voltage	-0.3	625	V
$V_S$	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
$V_{HO}$	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
$V_{CC}$	Low side and logic fixed supply voltage	-0.3	25	
$V_{LO}$	Low side output voltage	-0.3	$V_{CC} + 0.3$	
$V_{IN}$	Logic input voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$	
$dV_S/dt$	Allowable offset supply voltage transient	—	50	V/ns
$P_D$	Package power dissipation @ $T_A \leq +25^\circ\text{C}$	(8 Lead PDIP)	1.0	W
		(8 Lead SOIC)	0.625	
$R_{thJA}$	Thermal resistance, junction to ambient	(8 Lead PDIP)	125	$^\circ\text{C/W}$
		(8 Lead SOIC)	200	
$T_J$	Junction temperature	—	150	$^\circ\text{C}$
$T_S$	Storage temperature	-50	150	
$T_L$	Lead temperature (soldering, 10 seconds)	—	300	

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
$V_S$	High side floating supply offset voltage	Note 1	600	
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low side and logic fixed supply voltage	10	20	
$V_{LO}$	Low side output voltage	0	$V_{CC}$	
$V_{IN}$	Logic input voltage	$V_{SS}$	$V_{CC}$	
$T_A$	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for  $V_S$  of -5 to +600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V,  $C_L$  = 1000 pF, and  $T_A$  = 25°C, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	750	950	nsec	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	200	280		$V_S = 0V$ or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	70		
$t_r$	Turn-on rise time	—	150	220		$V_S = 0V$
$t_f$	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DTLO-HO) & HO turn-off to LO turn-on (DTHO-LO)	400	540	680		
MDT	Deadtime matching = DTLO - HO - DTHO-LO	—	0	60		

## Static Electrical Characteristics

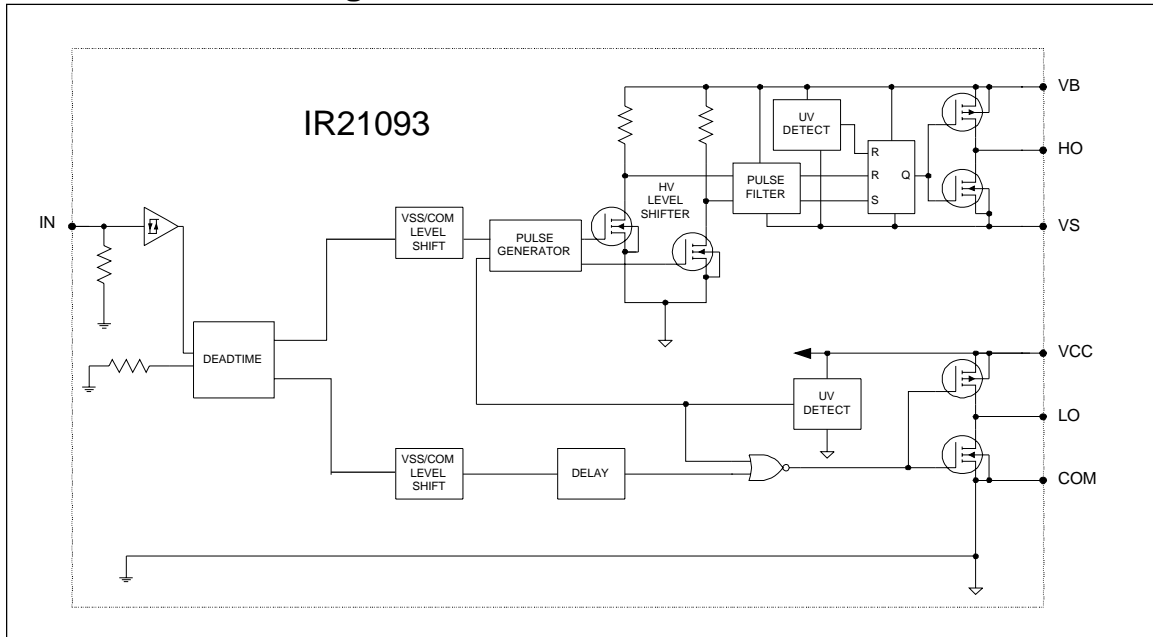
$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS}$ ) = 15V and  $T_A$  = 25°C unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to COM and are applicable to the respective input leads. The  $V_O$ ,  $I_O$  and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage for HO & logic "0" for LO	2.9	—	—	V	$V_{CC} = 10V$ to 20V
$V_{IL}$	Logic "0" input voltage for HO & logic "1" for LO	—	—	0.8		$V_{CC} = 10V$ to 20V
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20$ mA
$V_{OL}$	Low level output voltage, $V_O$	—	0.3	0.6		$I_O = 20$ mA
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu A$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	20	60	150	mA	$V_{IN} = 0V$ or 5V
$I_{QCC}$	Quiescent $V_{CC}$ supply current	0.4	1.0	1.6		$V_{IN} = 0V$ or 5V RDT = 0
$I_{IN+}$	Logic "1" input bias current	—	5	20	$\mu A$	IN = 5V, SD = 0V
$I_{IN-}$	Logic "0" input bias current	—	1	2		IN = 0V, SD = 5V
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$V_{CCUVH}$ $V_{BSUVH}$	Hysteresis	0.3	0.7	—		
$I_{O+}$	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$ , PW $\leq 10$ $\mu s$
$I_{O-}$	Output low short circuit pulsed current	250	350	—		$V_O = 15V$ , PW $\leq 10$ $\mu s$

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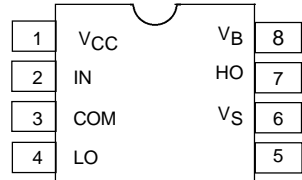
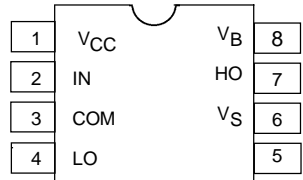
## Functional Block Diagrams



## Lead Definitions

Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM)
VB	High side floating supply
HO	High side gate drive output
VS	High side floating supply return
VCC	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

## Lead Assignments

 <p>8-Lead PDIP</p>	 <p>8-Lead SOIC</p>
<b>IR21093</b>	<b>IR21093S</b>

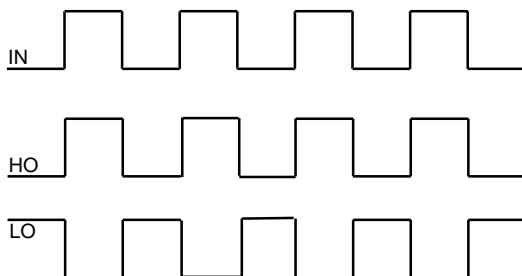


Figure 1. Input/Output Timing Diagram

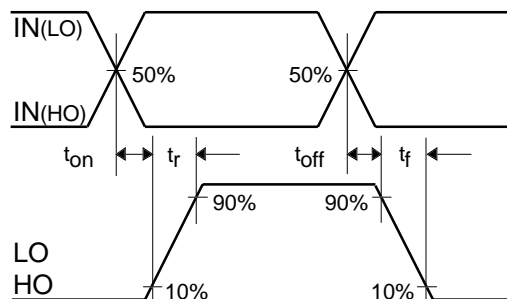


Figure 2. Switching Time Waveform Definitions

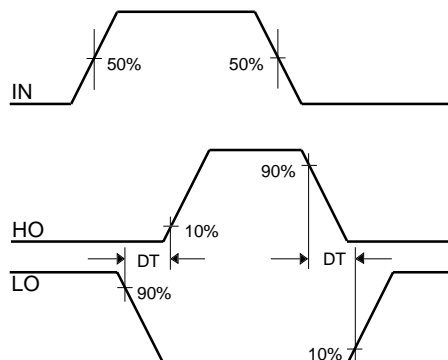


Figure 3. Deadtime Waveform Definitions

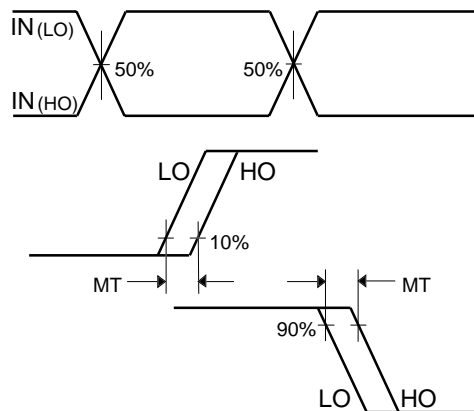


Figure 4. Delay Matching Waveform Definitions

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## Case Outlines

