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International
IOR Rectifier

PD-60022B

IR2130D
3-PHASE DRIVER

Features

- Hermetic
- Floatingchanneldesignedforbootstrap operation
  Fully operational to +400V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent half-bridge drivers
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET}	400V max.
I_O+/-	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	675 & 425 ns
Deadtime (typ.)	0.9 µs

Description

The IR2130D is a high voltage, high speed power MOSFET and IGBT driver with three independent high and low side referenced output channels. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5V CMOS or LSTTL outputs. A ground-referenced operational amplifier provides analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor.

An open drain $\overline{\text{FAULT}}$ signal indicates if an over-current or undervoltage shutdown has occurred. The output driverhgre a high pulse current buffer stage designed for minimum driver cross-con duction. Propagation delays are matched to simplify use at high frequencies. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operate up to 400 volts.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to Vso. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Parameter	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Absolute Voltage	-0.3	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	V_{SO} - 5	V_{SO} + 400	
$V_{HO1,2,3}$	High Side Output Voltage	$V_{S1,2,3}$ - 0.3	$V_{S1,2,3}$ + 0.3	
V_{CC}	Low Side Fixed Supply Voltage	-0.3	20	
V_{SO}	Low Side Driver Return	-5	V_{CC} + 0.3	
$V_{LO1,2,3}$	Low Side Output Voltage	V_{SO} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	-0.3	V_{CC} + 0.3	
V_{FLT}	Fault Output Voltage	-0.3	V_{CC} + 0.3	
V_{CAO}	Operational Amplifier Output Voltage	-0.3	V_{CC} + 0.3	
V_{CA}-	Operational amplifier Inverting Input Voltage	-0.3	V_{CC} + 0.3	
dVS/dt	Allowable Offset Supply Voltage Transient (Fig. 16)	—	50	V/nS
P_D	Package Power Dissipation @ TA< = 25°C (Fig. 19)	—	1.5	W
R_{thJA}	Thermal Resistance, Junction to Ambient	—	70	°C/W
T_j	Junction Temperature	-55	125	°C
T_S	Storage Temperatue	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	
	Weight	6.1 (typical)		g

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Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to V_{S0}. The V_S offset rating is tested with all supplies biased at 15V differential.

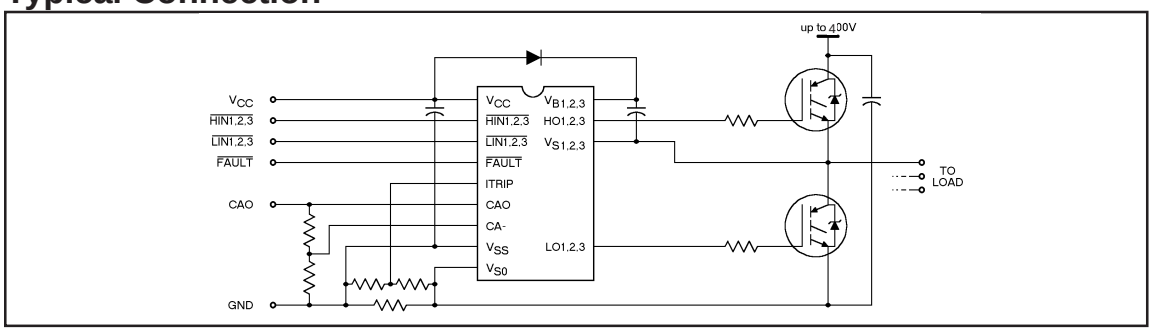
Symbol	Parameter	Min.	Max.	Units
$V_{B1,2,3}$	High Side Floating Supply Voltage	$V_{S1,2,3}$ + 10	$V_{S1,2,3}$ + 20	V
$V_{S1,2,3}$	High Side Floating Supply Offset Voltage	V_{SO} - 5	V_{SO} + 400	
$V_{HO1,2,3}$	High Side Output Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$	
V_{CC}	Low Side Fixed Supply Voltage	10	20	
V_{SS}	Logic Ground	-5	5	
$V_{LO1,2,3}$	Low Side Output Voltage	0	V_{CC}	
V_{IN}	Logic Input Voltage (HIN, LIN & SD)	V_{SS}	V_{SS} + 5	
V_{FLT}	Fault Output Voltage	V_{SS}	V_{CC}	
V_{CAO}	Operational Amplifier Output Voltage	V_{SS}	5	
V_{CA-}	Operational Amplifier Inverting Input Voltage	V_{SS}	5	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15V, $V_{S0,1,2,3}$ = V_{SS}, C_L = 1000 pF unless otherwise specified.

		Tj = 25°C			Tj = -55 to 125°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay (all six channels)	500	675	850	—	850	ns	CL= 1000pF $V_{S1,2,3}$ = 0 to 400 V V_{IN} = 0 & 5 V
t_r	Turn-On Rise Time (all six channels)	—	80	125	—	175		
t_{off}	Turn-Off Propagation Delay (all six channels)	300	425	550	—	600		
t_f	Turn-Off Fall Time (all six channels)	—	35	55	—	85		
DT	Deadtime (LS Turn-off to HS Turn-on & HS Turn-off to LS Turn-on)	0.4	0.9	1.3	0.25	1.5	µs	CL = 1000pF, V_{IN} = 0 & 5V
t_{itrip}	ITRIP to Output Shutdown Prop. Delay	400	660	920	—	1100	ns	CL = 1000pF, V_{IN}, V_{ITRIP} = 0 & 5V
t_{flt}	ITRIP to FAULT Indication Delay	335	590	845	—	1000	ns	
t_{fltclr}	LIN1, 2, 3 To FAULT Clear Time	5.5	10	12.5	—	—	µs	
$t_{flt,in}$	Input Filter Time (all six inputs)	—	310	—	—	—	ns	V_{IN} = 0 & 5V
t_{bl}	ITRIP Blanking Time	—	400	—	—	—	ns	V_{ITRIP} = 1V
SR+	Amplifier Slew Rate (+)	4.4	6.2	—	2.7	—	V/µs	
SR-	Amplifier Slew Rate (-)	2.4	3.2	—	1.5	—	V/µs	

Typical Connection



Static Electrical Characteristics

V_{BIAS} (V_{CC}, $V_{BS1, 2, 3}$) = 15V, $V_{SO1, 2, 3}$ = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1, 2, 3 & LIN1, 2, 3. The V_O and I_O parameters are referenced to $V_{SO1, 2, 3}$.

		Tj = 25°C			Tj=55-125°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Max.	Units	Test Conditions
I_{LK}	Offset Supply Leakage Currents	—	—	50	—	500	µA	$V_B = V_S$=400V
I_{QBS}	Quiescent V_{BS} Supply Current	—	15	30	—	45		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	3.0	4.0	—	6.0	mA	V_{IN} = 0V or 5V
I_{IN}^+	Logic “1” Input Bias Current(OUT= HI)	—	450	650	—	1050	µA	V_{IN} = 0V
I_{IN}^-	Logic “0” Input Bias Current(OUT=LO)	—	225	400	—	—		V_{IN} = 5V
I_{ITRIP}^+	“High” ITRIP Bias Current	—	75	150	—	—		ITRIP = 5V
I_{ITRIP}^-	“Low” ITRIP Bias Current	—	—	100	—	170	nA	ITRIP =0V
$V_{IN,IH}$	Logic “0” Input Voltage(OUT = LO)	—	—	—	2.2	—	V	
$V_{IN,IL}$	Logic “1” Input Voltage (OUT = HI)	—	—	—	—	0.8		
$V_{IT,TH}^+$	ITRIP Input Positive Going Threshold	400	490	580	350	580	mV	
V_{OS}	Amplifier Input Offset Voltage	—	—	30	—	—	mV	V_{SO} = CA- = 0.2V
$R_{on,FLT}$	FAULT- Low On Resistance	—	55	75	—	150	Ω	
I_{CA}^-	CA- Input Bias Current	—	0.5	4.0	—	4.0	nA	CA- = 2.5V
V_{CCUV}^+	V_{CC} Supply Undervoltage Positive Going Threshold	8.3	9.0	10.6	8.0	10.7	V	
V_{CCUV}^-	V_{CC} Supply Undervoltage Negative Going Threshold	8.0	8.7	10.5	7.7	10.5		
V_{BSUV}^+	V_{BS} Supply Undervoltage Positive Going Threshold	7.5	8.4	9.2	—	—	V	
V_{BSUV}^-	V_{BS} Supply Undervoltage Negative Going Threshold	7.1	8.0	8.8	—	—		
I_O^+	Output High Short Circuit Pulsed Current	200	250	—	—	—		V_{OUT} = V_{IN-} = 0V PW <= 10µS
I_O^-	Output Low Short Circuit Pulsed Current	420	500	—	—	—	mA	V_{OUT} =15, V_{IN-}=5V PW <= 10µS
$V_{OH,Amp}$	Amplifier High Level Output Voltage	5.0	5.2	5.4	4.9	5.6	V	CA- = 0V, VSO =1V
$V_{OL,Amp}$	Amplifier Low Level Output Voltage	—	2.5	20	—	20	mV	CA- = 1V, VSO =0V
$I_{SRC,Amp}$	Amplifier Output Source Current	2.3	4.0	—	1.5	—	mA	CA- = 0V, VSO =1V, CAO=4V
$I_{SNK,Amp}$	Amplifier Output Sink Current	1.0	2.1	—	0.5	—		CA- = 1V, VSO =0V,CAO=2V
CMRR	Amplifier Common Mode Rejection Ratio	60	80	—	—	—	dB	CA- =V_{SO} =0.1V & 5V
PSRR	Amplifier Power Supply Rejection Ratio	55	75	—	—	—		CA- = V_{SO} =0.2V VCC = 10V & 20V
V_{OH}	High Level Output Voltage	—	—	100	—	100	mV	V_{IN-} = 0V, IO = 0A
V_{OL}	Low Level Output Voltage	—	—	100	—	100		V_{IN-} = 5V, IO = 0A

Static Electrical Characteristics Continued

V_{BIAS} (V_{CC}, $V_{BS1, 2, 3}$) = 15V, $V_{SO1, 2, 3}$ = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six logic input leads: HIN1, 2, 3 & LIN1, 2, 3. The V_O and I_O parameters are referenced to $V_{SO1, 2, 3}$.

		Tj = 25°C			Tj = 55 to 125°C			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Max.	Units	Test Conditions
$I_{O+,Amp}$	Amplifier Output High Short Circuit Circuit	—	4.5	6.5	—	8.0		CA- = 0V, V_{SO} = 5V V_{CAO} = 0V
$I_{O-,Amp}$	Amplifier Output High Short Circuit Circuit	—	3.2	5.2	—	7.0		CA- = 5V, V_{SO} = 0V V_{CAO} = 5V

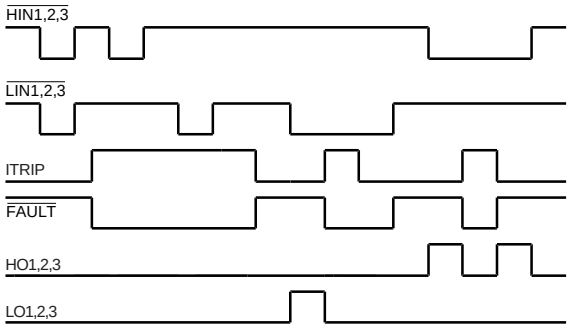


Figure 1. Input/Output Timing Diagram

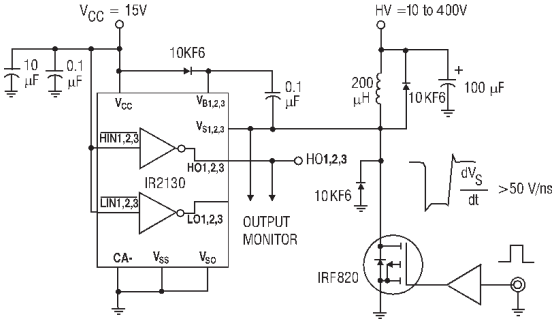


Figure 2. Floating Supply Voltage Transient Test Circuit

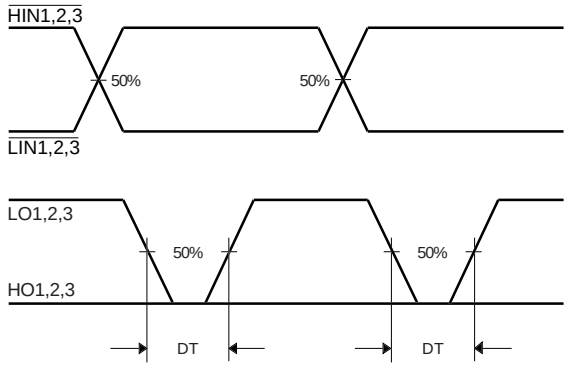


Figure 3. Deadtime Waveform Definitions

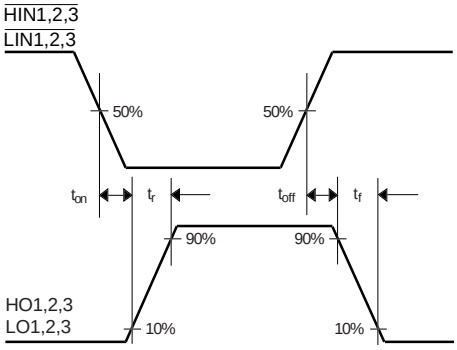


Figure 4. Input/Output Switching Time Waveform Definitions

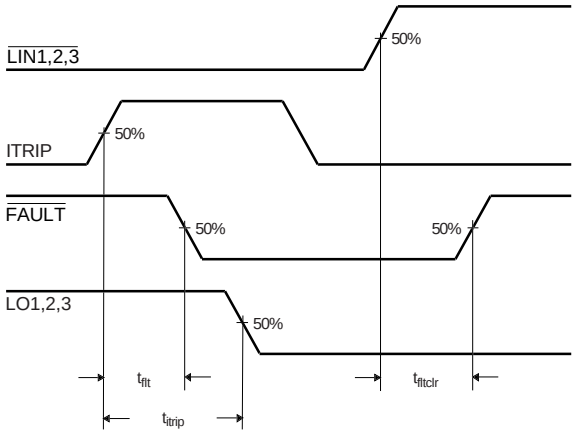


Figure 5. Overcurrent Shutdown Switching Time Waveform Definitions

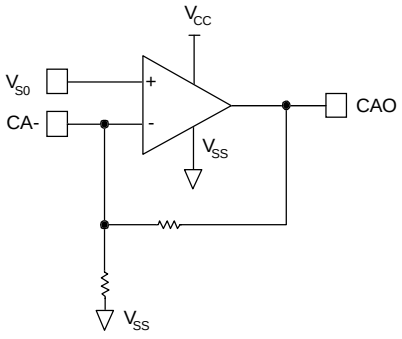


Figure 6. Diagnostic Feedback Operational Amplifier Circuit

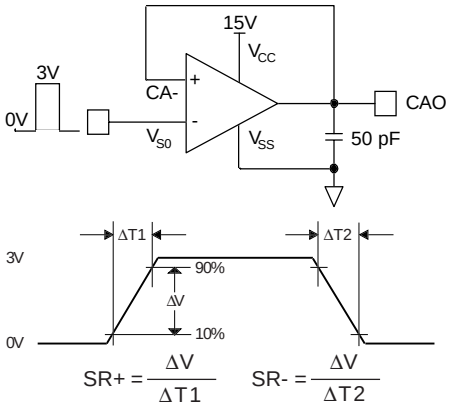


Figure 7. Operational Amplifier Slew Rate Measurement

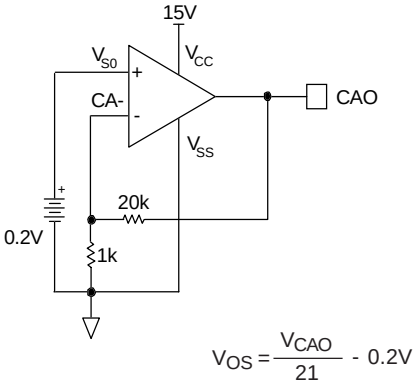
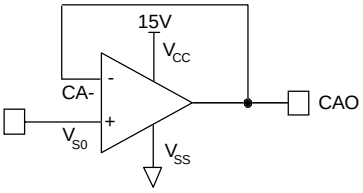


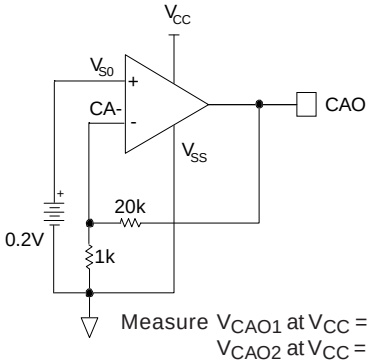
Figure 8. Operational Amplifier Input Offset Voltage Measurement



Measure V_{CAO1} at V_{S0} = 0.1V
V_{CAO2} at V_{S0} = 5V

$$CMRR = -20*LOG\left|\frac{(V_{CAO1}-0.1V) - (V_{CAO2}-5V)}{4.9V}\right| (dB)$$

Figure 9. Operational Amplifier Common Mode Rejection Ratio Measurements



Measure V_{CAO1} at V_{CC} = 10V
V_{CAO2} at V_{CC} = 20V

$$PSRR = -20*LOG\left|\frac{V_{CAO1} - V_{CAO2}}{(10V)\ (21)}\right|$$

Figure 10. Operational Amplifier Power Supply Rejection Ratio Measurements

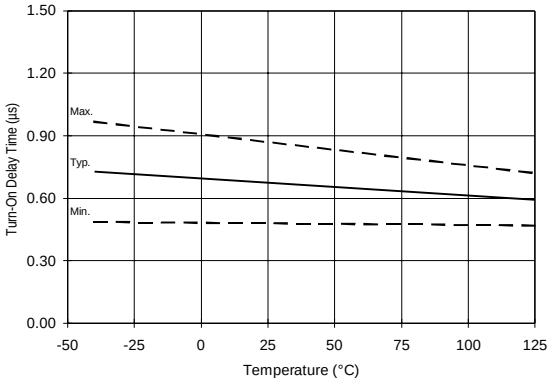


Figure 11A. Turn-On Time vs. Temperature

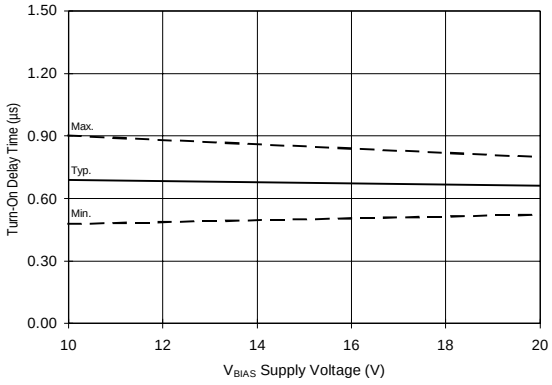


Figure 11B. Turn-On Time vs. Voltage

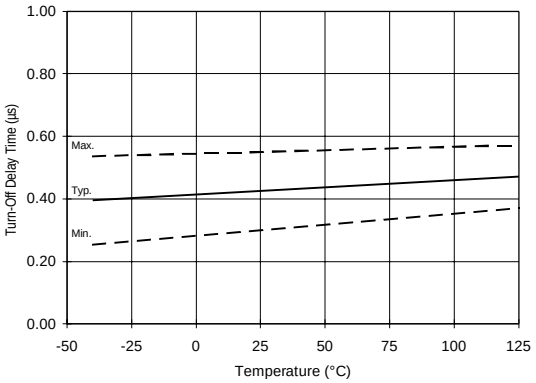


Figure 12A. Turn-Off Time vs. Temperature

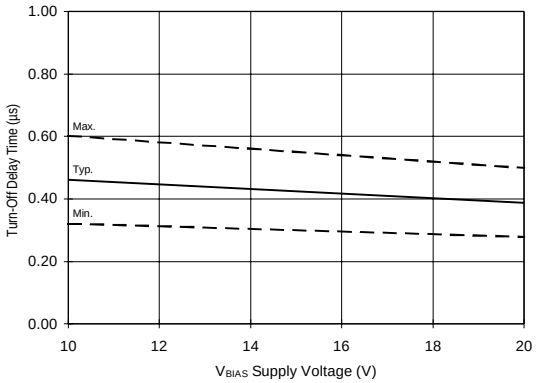


Figure 12B. Turn-Off Time vs. Voltage

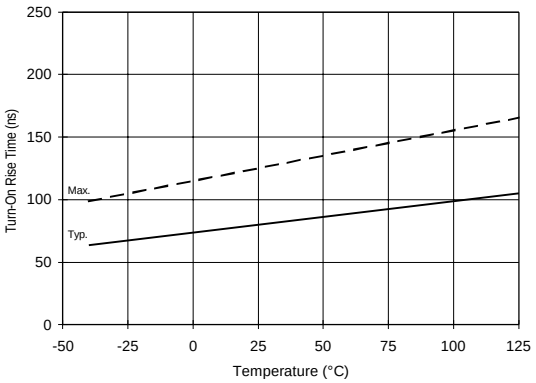


Figure 13A. Turn-On Rise Time vs. Temperature

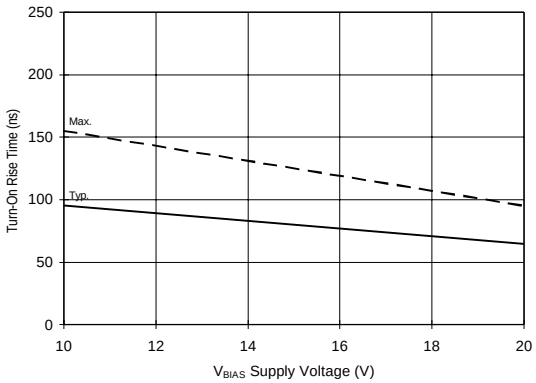


Figure 13B. Turn-On Rise Time vs. Voltage

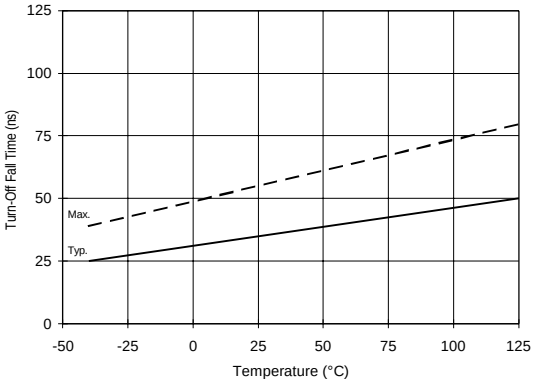


Figure 14A. Turn-Off Fall Time vs. Temperature

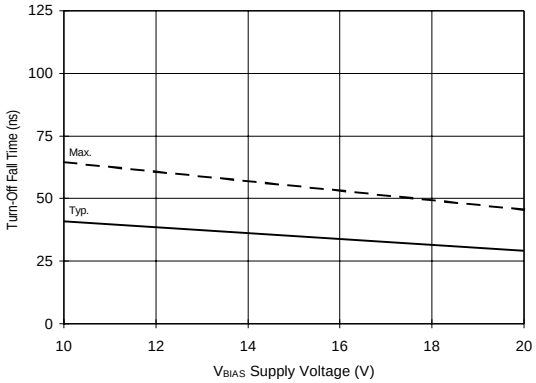


Figure 14B. Turn-Off Fall Time vs. Voltage

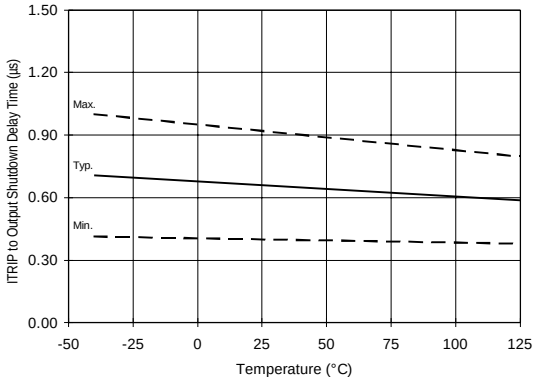


Figure 15A. ITRIP to Output Shutdown Time vs. Temperature

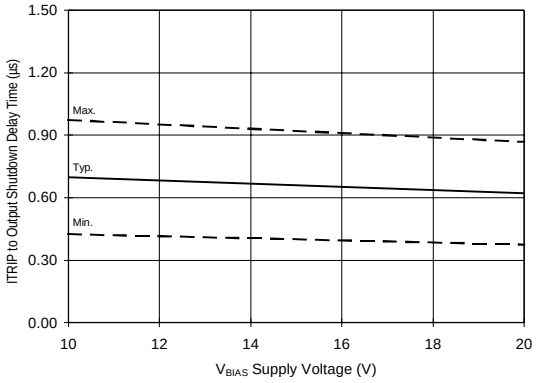


Figure 15B. ITRIP to Output Shutdown Time vs. Voltage

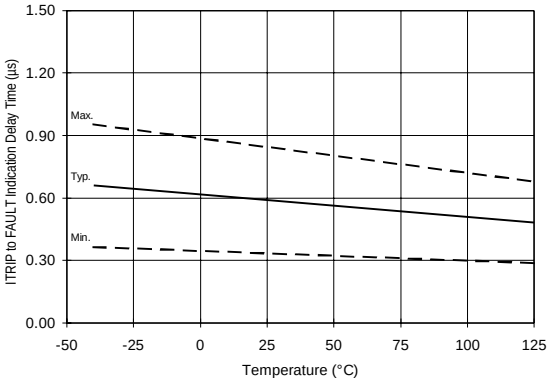


Figure 16A. ITRIP to **FAULT** Indication Time vs. Temperature

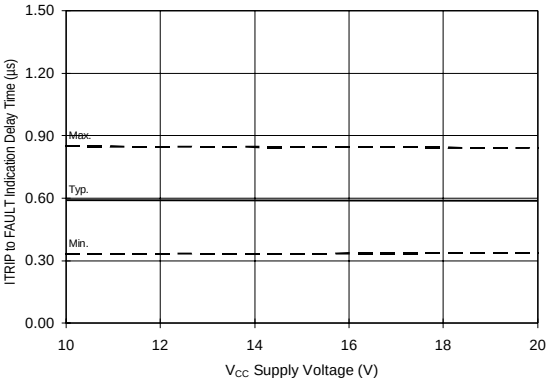


Figure 16B. ITRIP to **FAULT** Indication Time vs. Voltage

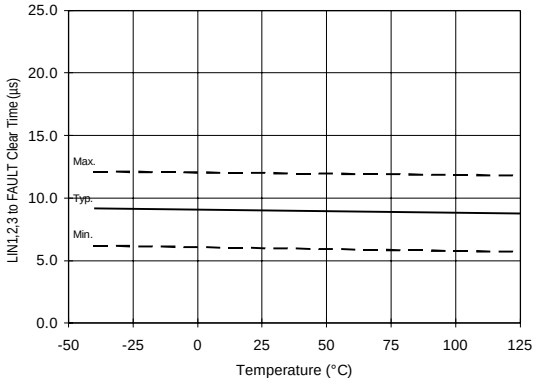


Figure 17A. **LIN1,2,3** to **FAULT** Clear Time vs. Temperature

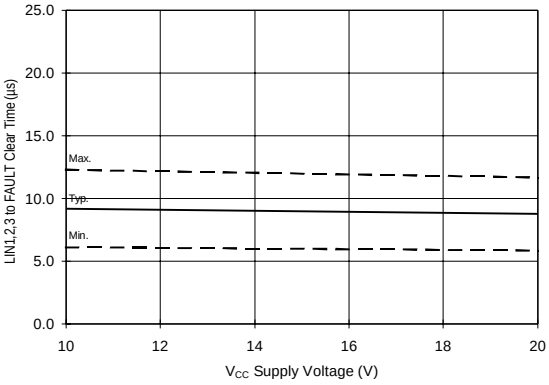


Figure 17B. **LIN1,2,3** to **FAULT** Clear Time vs. Voltage

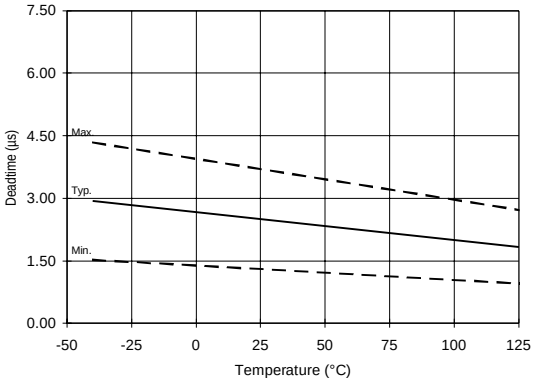


Figure 18A. Deadtime vs. Temperature

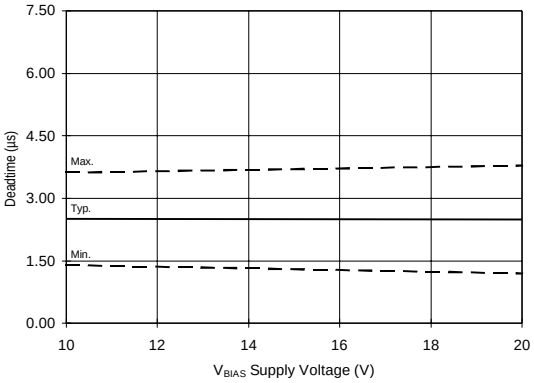


Figure 18B. Deadtime vs. Voltage

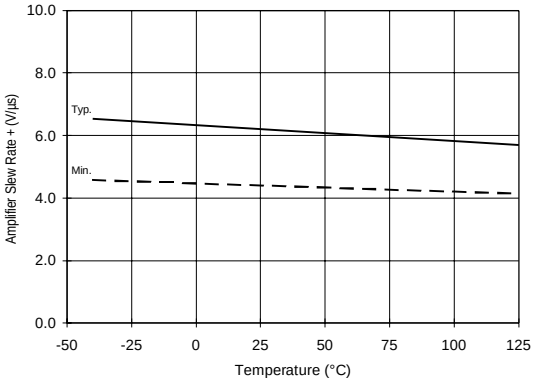


Figure 19A. Amplifier Slew Rate (+) vs. Temperature

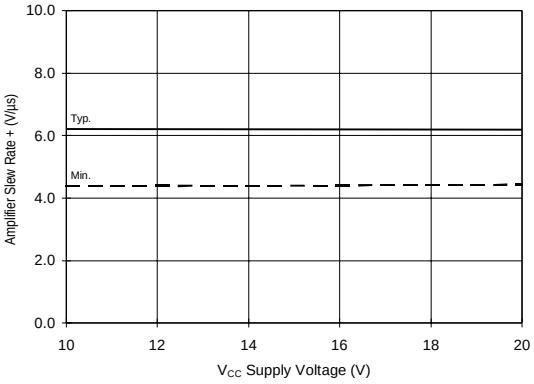


Figure 19B. Amplifier Slew Rate (+) vs. Voltage

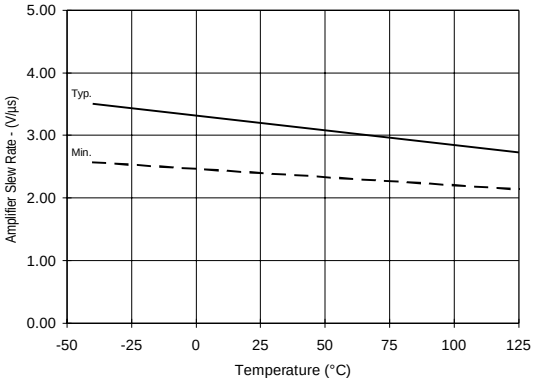


Figure 20A. Amplifier Slew Rate (-) vs. Temperature

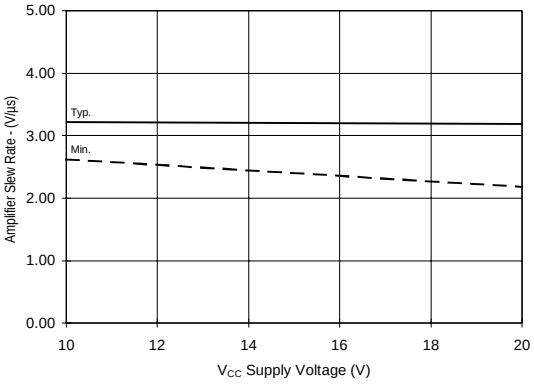


Figure 20B. Amplifier Slew Rate (-) vs. Voltage

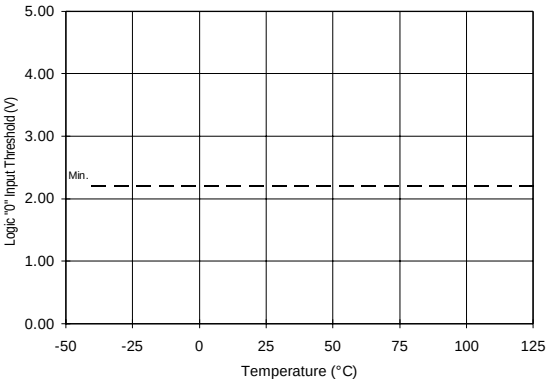


Figure 21A. Logic “0” Input Threshold vs. Temperature

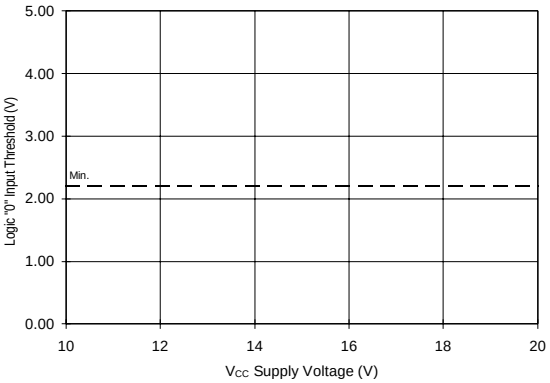


Figure 20B. Logic “0” Input Threshold vs. Voltage

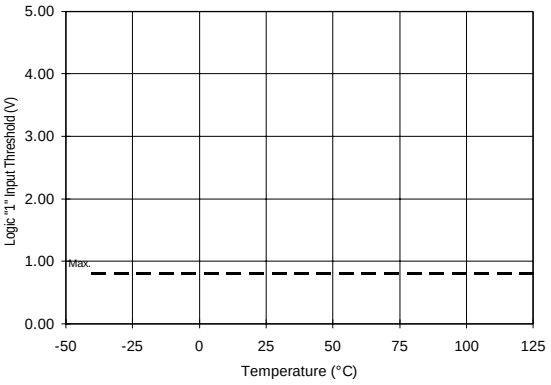


Figure 22A. Logic “1” Input Threshold vs. Temperature

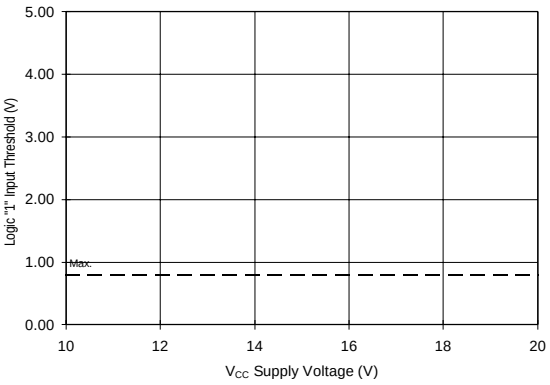


Figure 22B. Logic “1” Input Threshold vs. Voltage

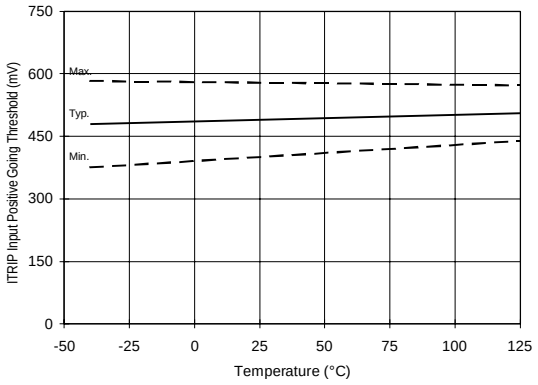


Figure 23A. ITRIP Input Positive Going Threshold vs. Temperature

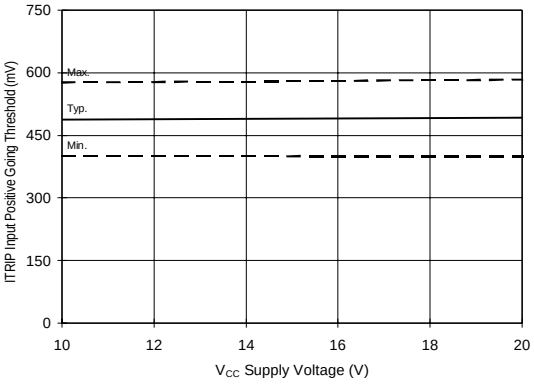


Figure 23B. ITRIP Input Positive Going Threshold vs. Voltage

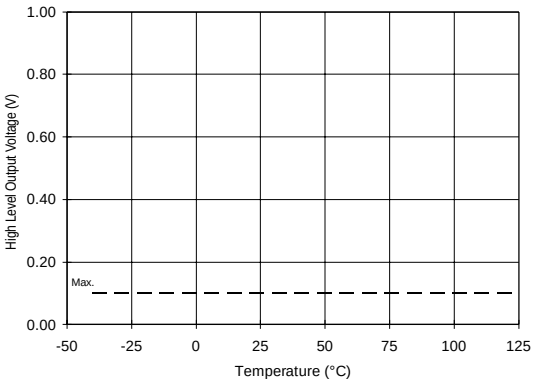


Figure 24A. High Level Output vs. Temperature

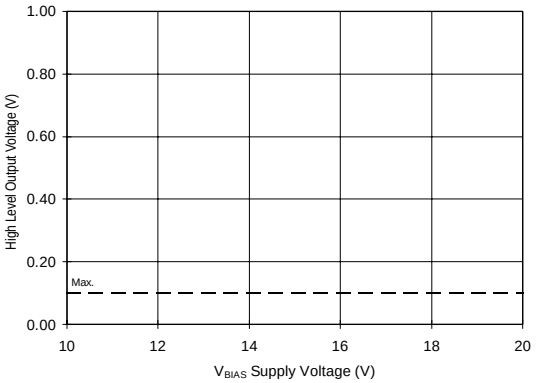


Figure 24B. High Level Output vs. Voltage

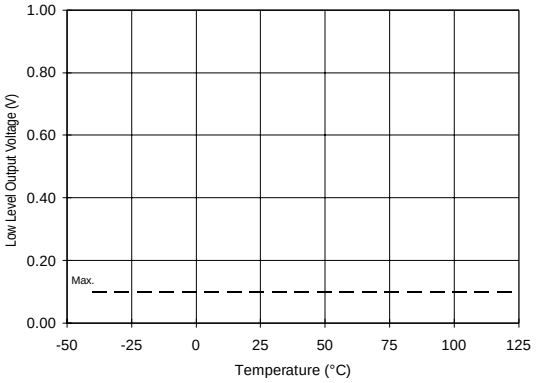


Figure 25A. Low Level Output vs. Temperature

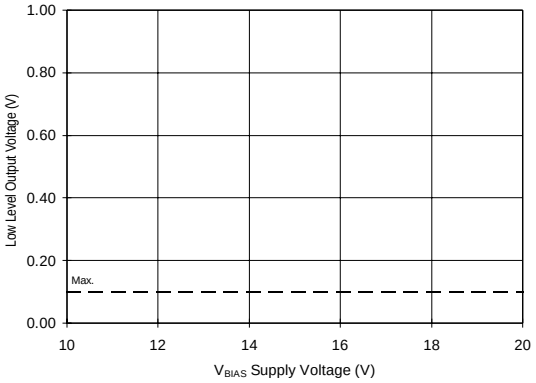


Figure 25B. Low Level Output vs. Voltage

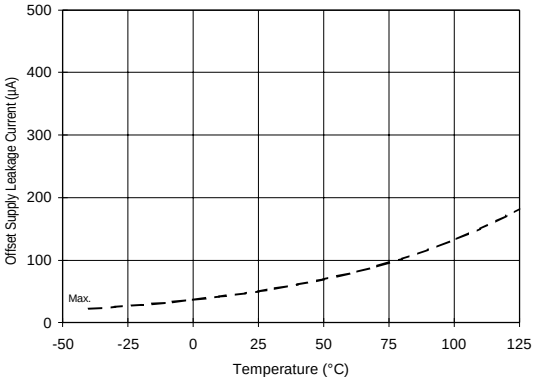


Figure 26A. Offset Supply Leakage Current vs. Temperature

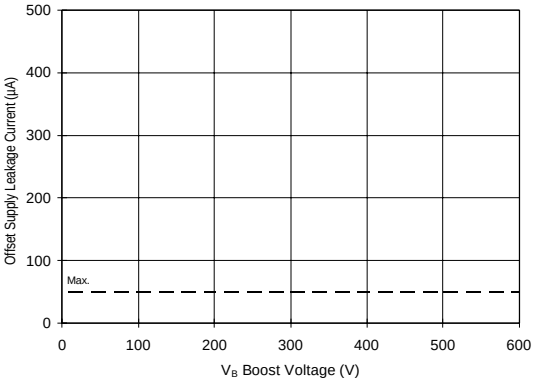


Figure 26B. Offset Supply Leakage Current vs. Voltage

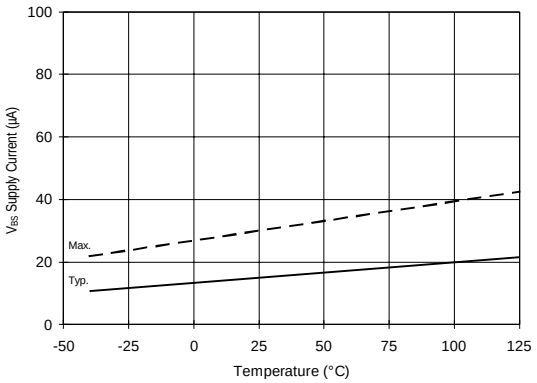


Figure 27A. V_{BS} Supply Current vs. Temperature

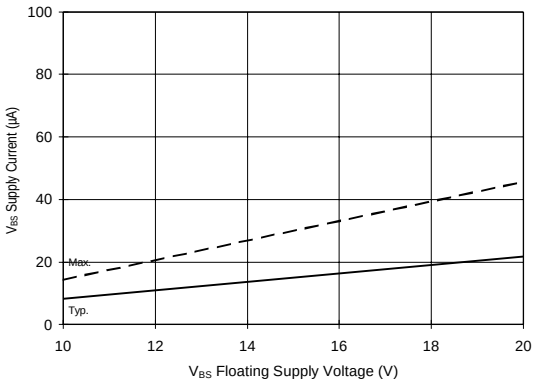


Figure 27B. V_{BS} Supply Current vs. Voltage

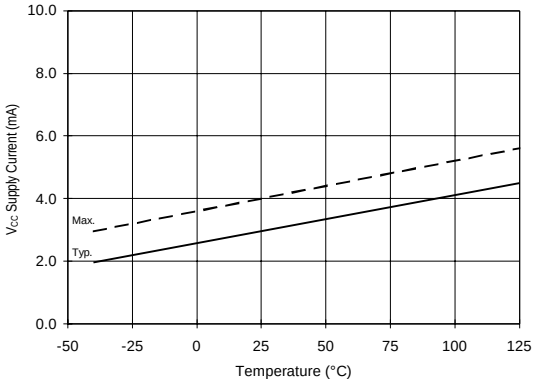


Figure 28A. V_{CC} Supply Current vs. Temperature

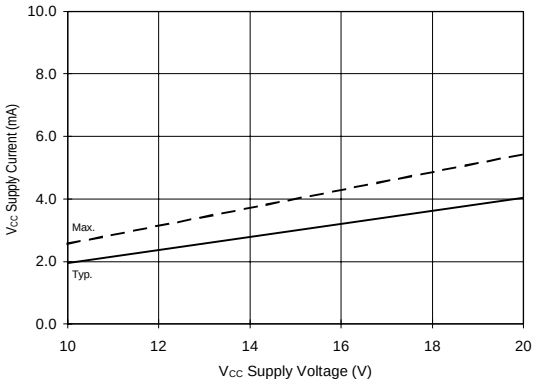


Figure 28B. V_{CC} Supply Current vs. Voltage

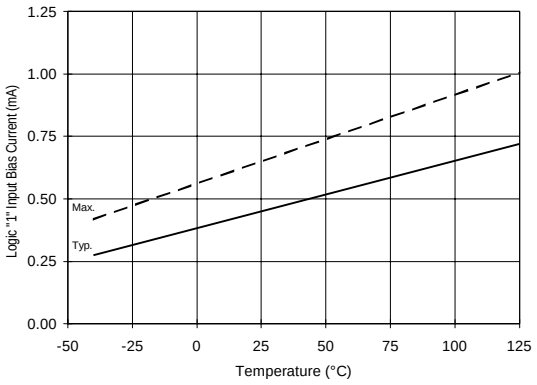


Figure 29A. Logic “1” Input Current vs. Temperature

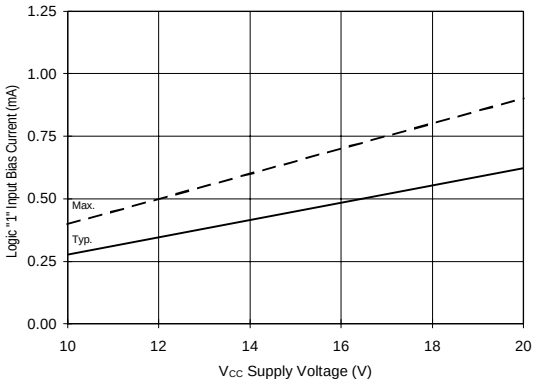


Figure 29A. Logic “1” Input Current vs. Voltage

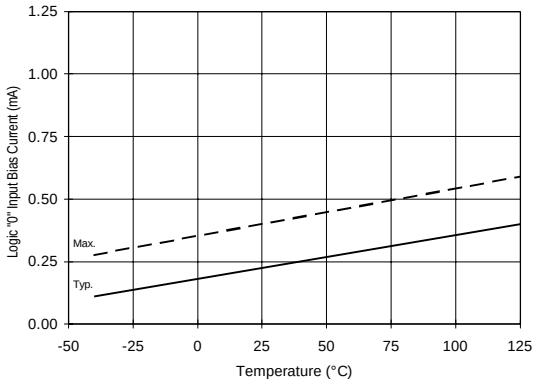


Figure 30A. Logic “0” Input Current vs. Temperature

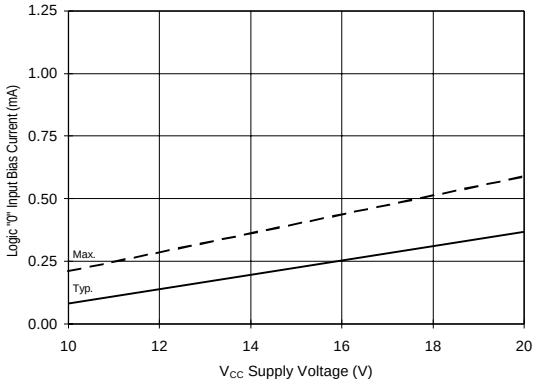


Figure 30B. Logic “0” Input Current vs. Voltage

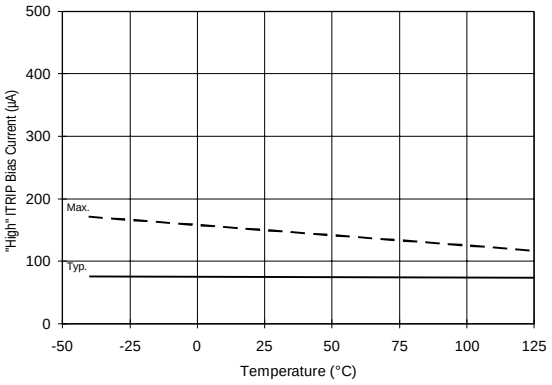


Figure 31A. “High” ITRIP Current vs. Temperature

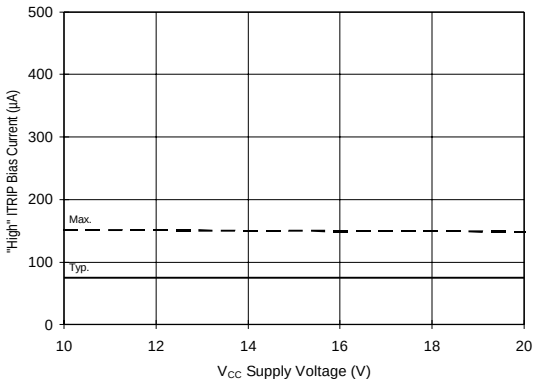


Figure 31B. “High” ITRIP Current vs. Voltage

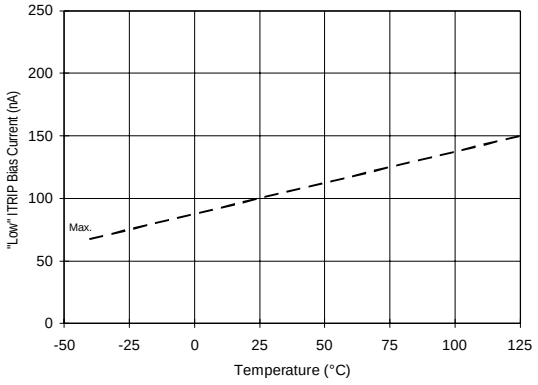


Figure 32A. “Low” ITRIP Current vs. Temperature

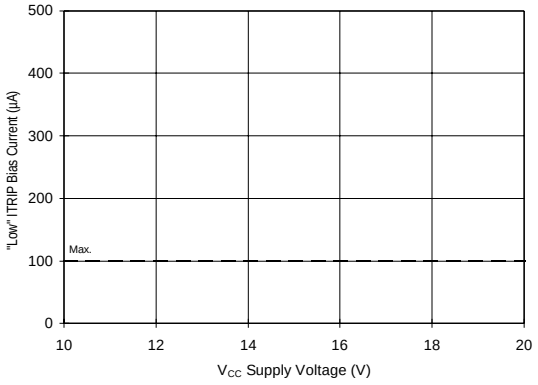


Figure 32B. “Low” ITRIP Current vs. Voltage

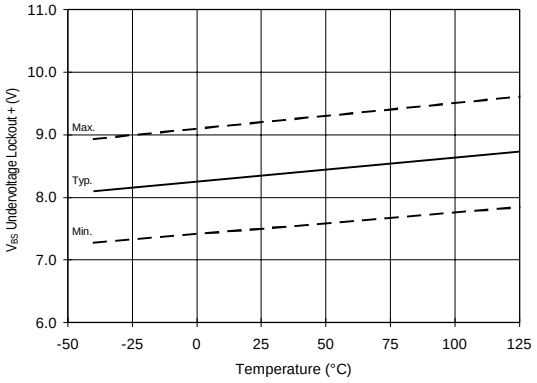


Figure 33. V_{BS} Undervoltage (+) vs. Temperature

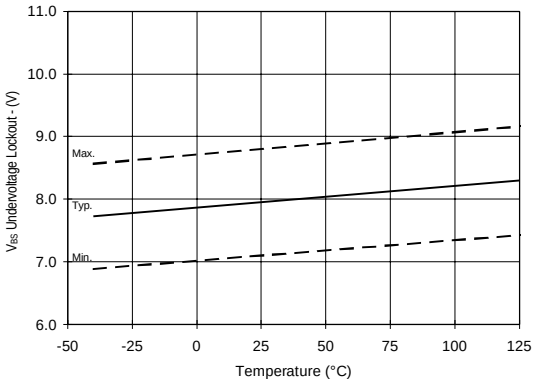


Figure 34. V_{BS} Undervoltage (-) vs. Temperature

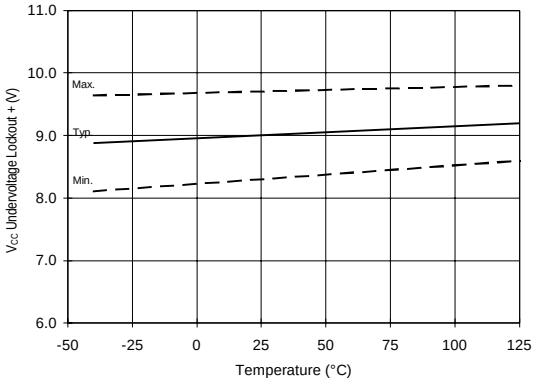


Figure 35. V_{CC} Undervoltage (+) vs. Temperature

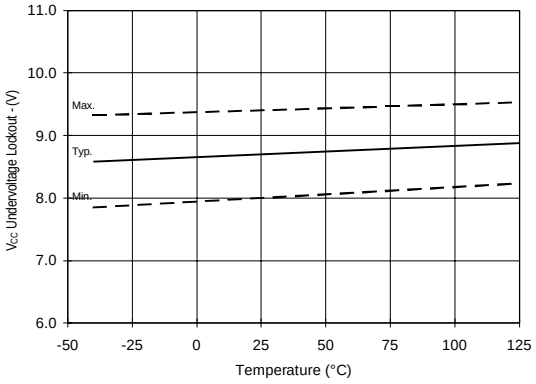


Figure 36. V_{CC} Undervoltage (-) vs. Temperature

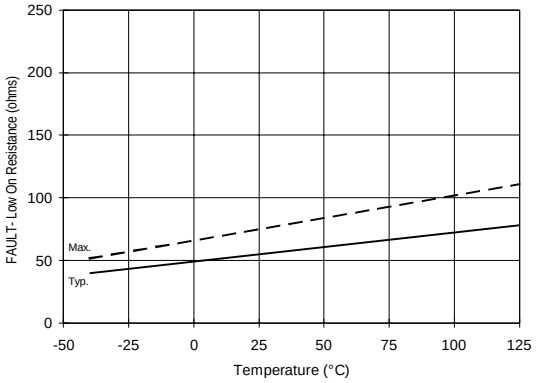


Figure 37A. **FAULT** Low On Resistance vs. Temperature

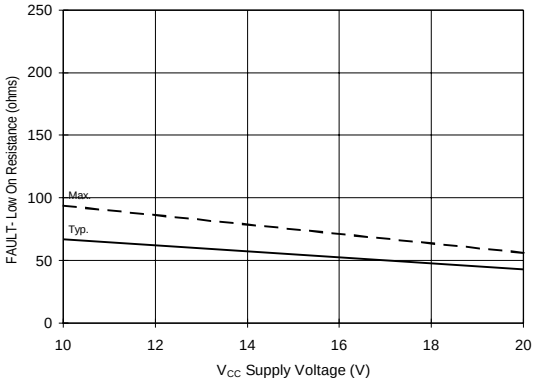


Figure 37B. **FAULT** Low On Resistance vs. Voltage

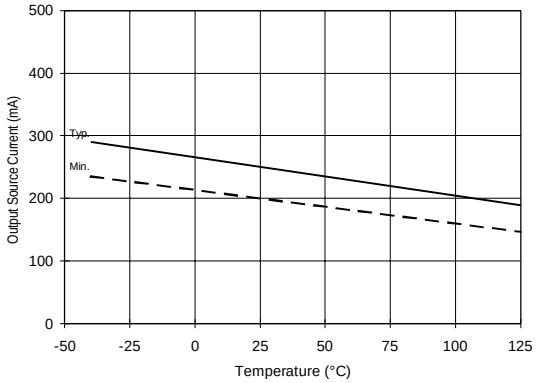


Figure 38A. Output Source Current vs. Temperature

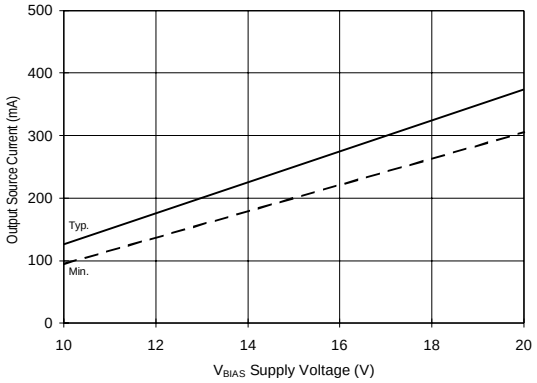


Figure 38B. Output Source Current vs. Voltage

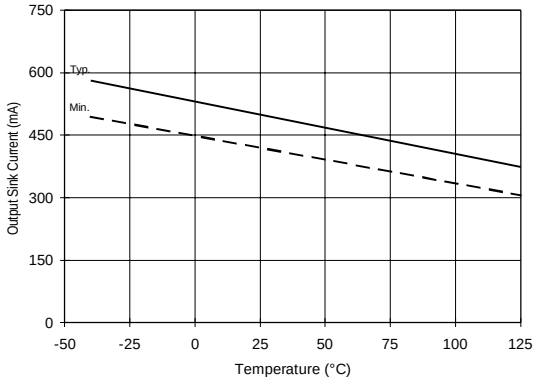


Figure 39A. Output Sink Current vs. Temperature

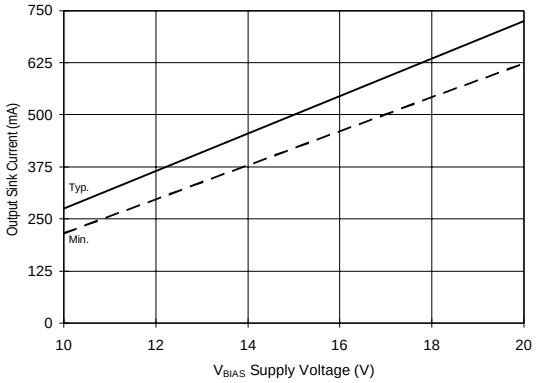


Figure 39B. Output Sink Current vs. Voltage

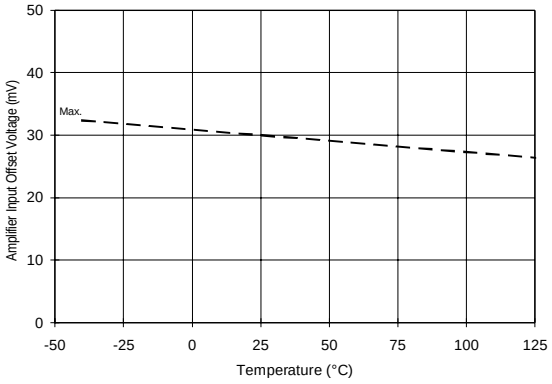


Figure 40A. Amplifier Input Offset vs. Temperature

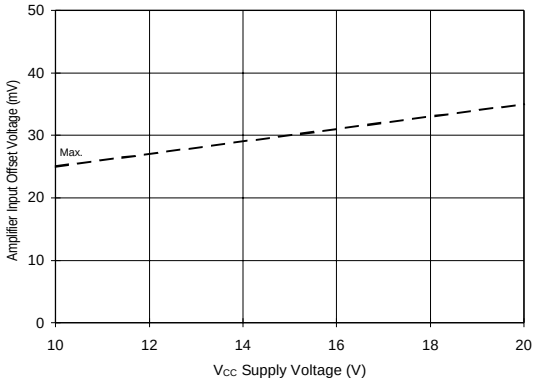


Figure 40B. Amplifier Input Offset vs. Voltage

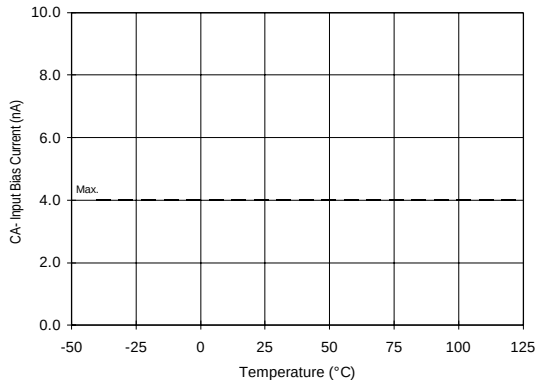


Figure 41A. CA- Input Current vs. Temperature

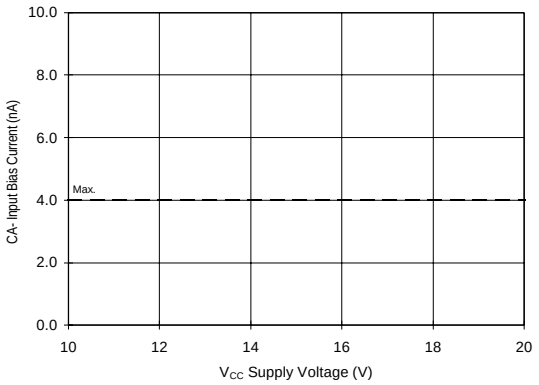


Figure 41B. CA- Input Current vs. Voltage

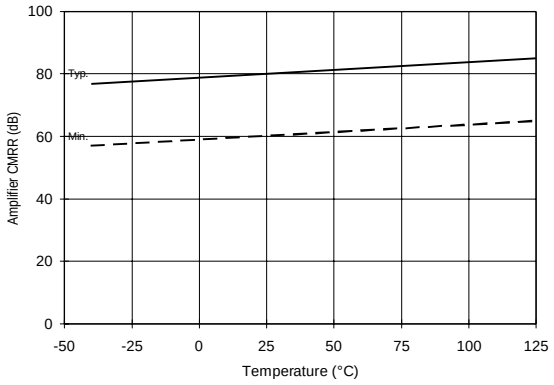


Figure 42A. Amplifier CMRR vs. Temperature

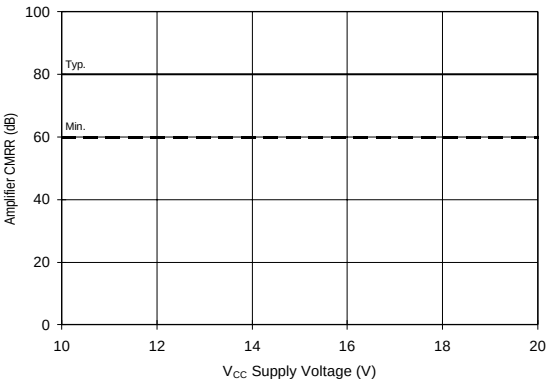


Figure 42B. Amplifier CMRR vs. Voltage

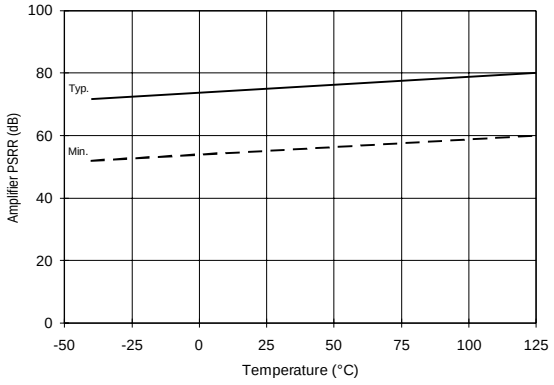


Figure 43A. Amplifier PSRR vs. Temperature

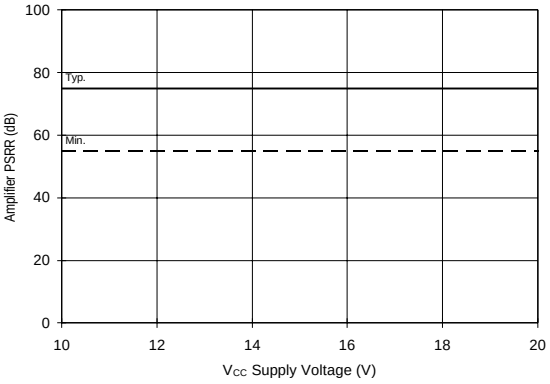


Figure 43B. Amplifier PSRR vs. Voltage

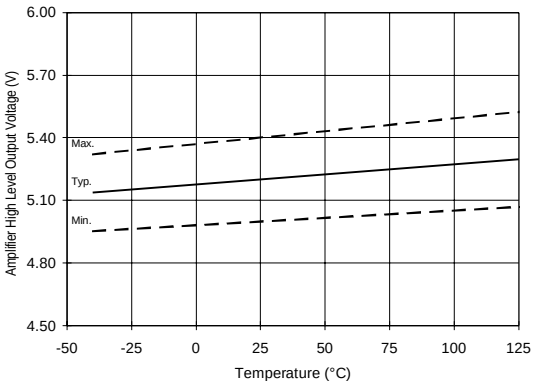


Figure 44A. Amplifier High Level Output vs. Temperature

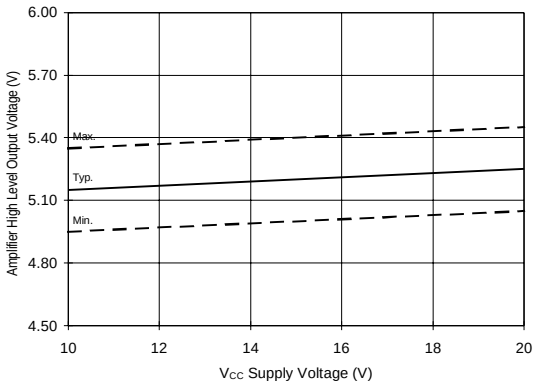


Figure 44B. Amplifier High Level Output vs. Voltage

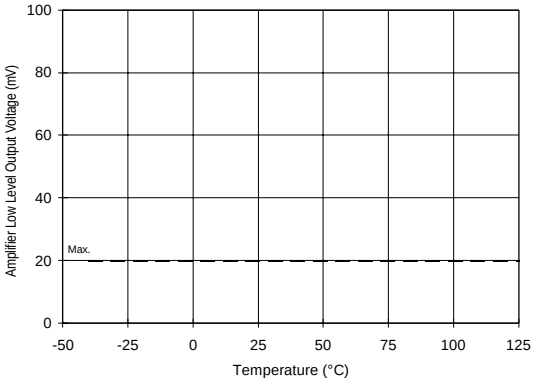


Figure 45A. Amplifier Low Level Output vs. Temperature

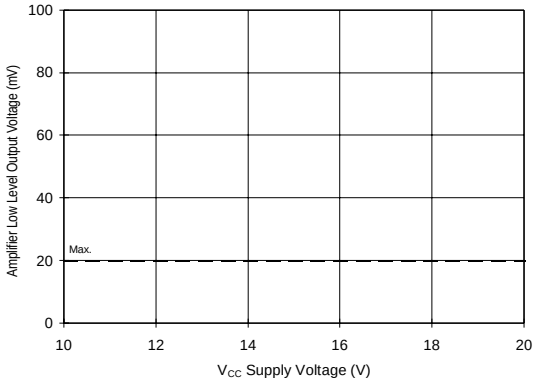


Figure 45B. Amplifier Low Level Output vs. Voltage

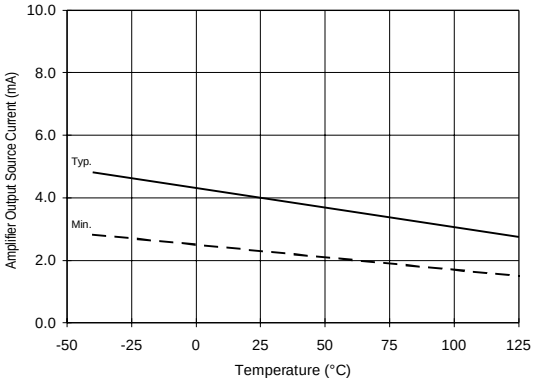


Figure 46A. Amplifier Output Source Current vs. Temperature

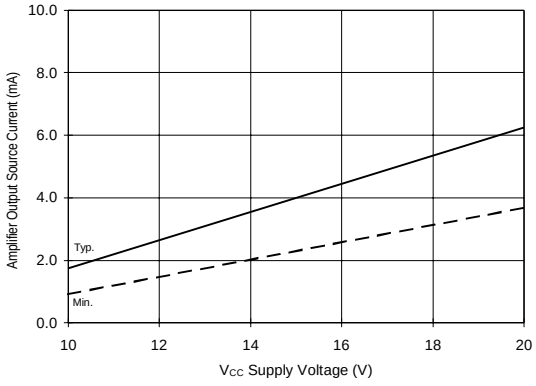


Figure 46B. Amplifier Output Source Current vs. Voltage

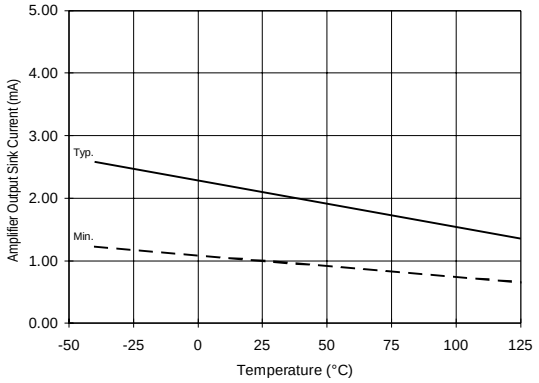


Figure 47A. Amplifier Output Sink Current vs. Temperature

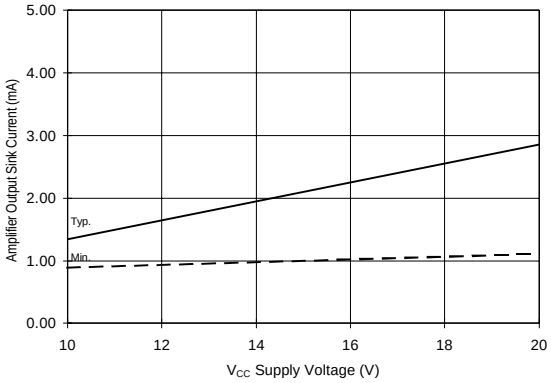


Figure 47B. Amplifier Output Sink Current vs. Voltage

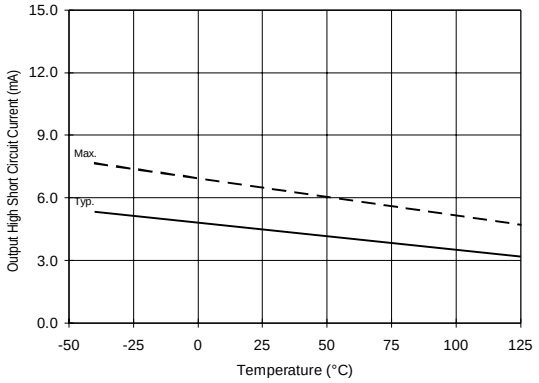


Figure 48A. Amplifier Output High Short Circuit Current vs. Temperature

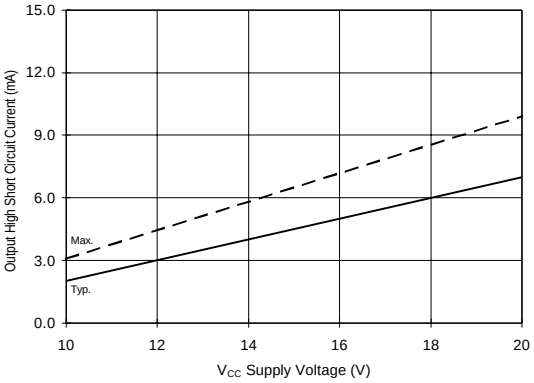


Figure 48B. Amplifier Output High Short Circuit Current vs. Voltage

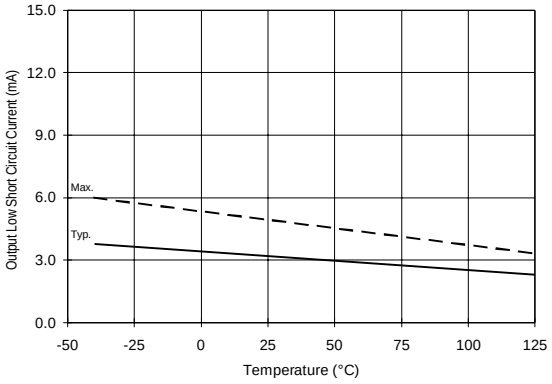


Figure 49A. Amplifier Output Low Short Circuit Current vs. Temperature

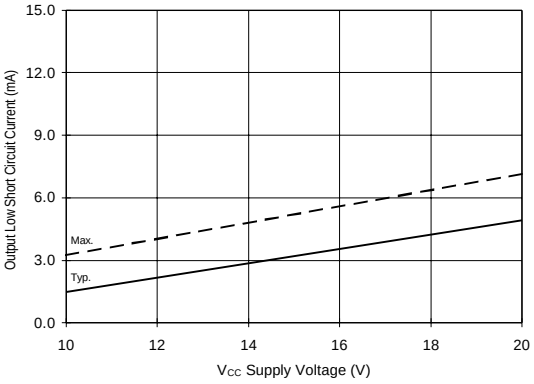


Figure 49B. Amplifier Output Low Short Circuit Current vs. Voltage

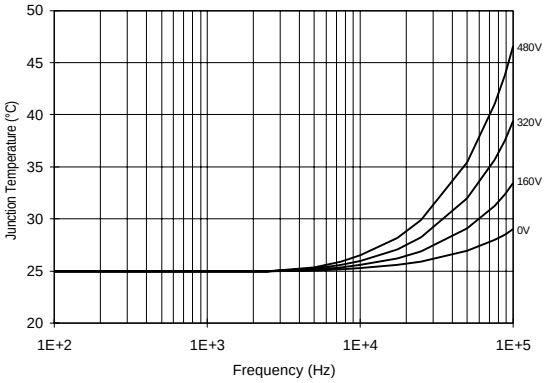


Figure 50. IR2130 T_J vs. Frequency (IRF820)
R_{GATE} = 33W, V_{CC} = 15V

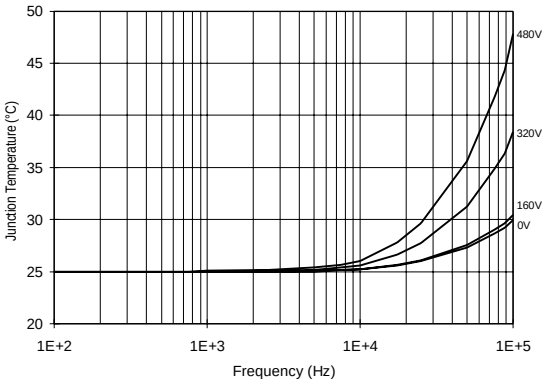


Figure 51. IR2130 T_J vs. Frequency (IRF830)
R_{GATE} = 20W, V_{CC} = 15V

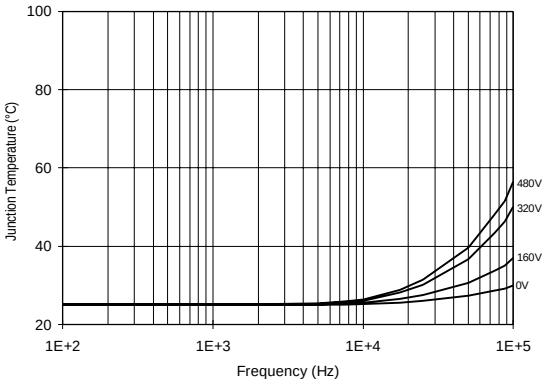


Figure 52. IR2130 T_J vs. Frequency (IRF840)
R_{GATE} = 15W, V_{CC} = 15V

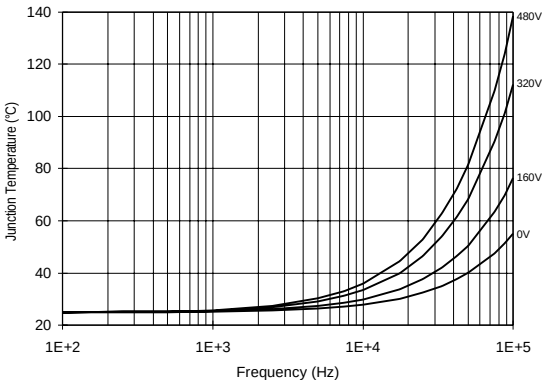


Figure 53. IR2130 T_J vs. Frequency (IRF450)
R_{GATE} = 10W, V_{CC} = 15V

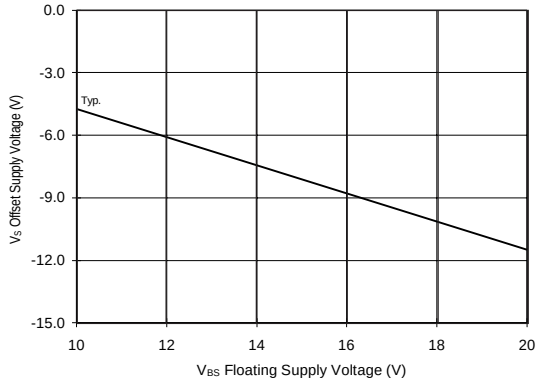
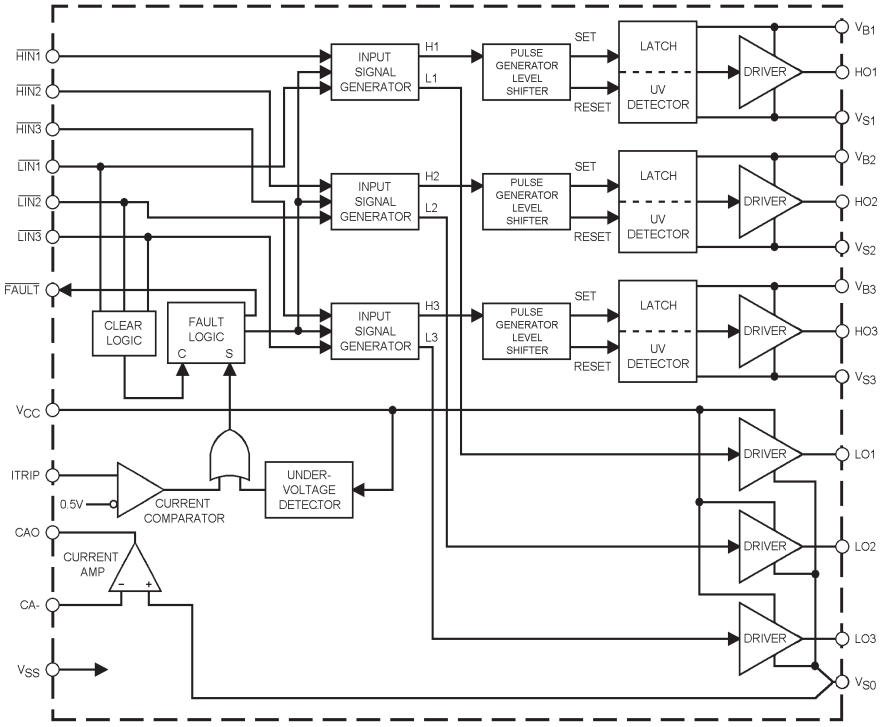


Figure 54. Maximum VS Negative Offset vs. V_{BS} Supply Voltage

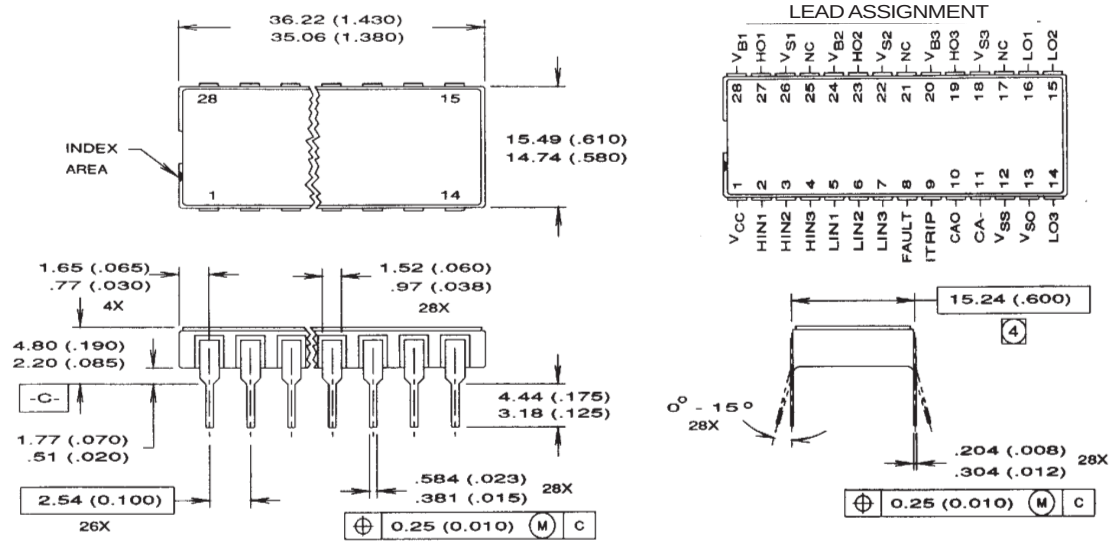
Functional Block Diagram



Lead Definitions

Lead Symbol	Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver output (LO1,2,3), out of phase
$\overline{FAULT}$	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic
V_{CC}	Low side and logic fixed supply
ITRIP	Input for over-current shutdown
CAO	Output of current amplifier
CA-	Negative input of current amplifier
V_{SS}	Logic ground
$V_{B1,2,3}$	High side floating supplies
HO1,2,3	High side gate drive outputs
$V_{S1,2,3}$	High side floating supply returns
LO1,2,3	Low side gate drive outputs
V_{S0}	Low side return and positive input of current amplifier

Case Outline and dimensions - MO038AB



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4 DIMENSION IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5 OUTLINE CONFORMS TO JEDEC OUTLINE MO-038AB.

International
IOR Rectifier

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Data and specifications subject to change without notice. 3/00