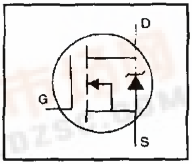
PD-9.1068

International
IOR Rectifier

IRF740LC

HEXFET® Power MOSFET

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V_{GS} Rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Extremely High Frequency Operation
- Repetitive Avalanche Rated



V_{DSS} = 400V

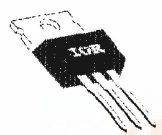
$R_{DS(on)}$ = 0.55Ω

I_D = 10A

Description

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	10	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	6.3	A
I_{DM}	Pulsed Drain Current ①	32	A
P_D @ T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ②	520	mJ
I_{AR}	Avalanche Current ①	10	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	°C
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

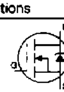
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	°C/W

Electrical Characteristics @ $T_J = 25°C$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	V_{GS}=0V, I_D= 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.76	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.55	Ω	V_{GS}=10V, I_D=6.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250μA
g_{fs}	Forward Transconductance	3.0	—	—	S	V_{DS}=50V, I_D=6.0A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS}=400V, V_{GS}=0V
		—	—	250		V_{DS}=320V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	39	nC	I_D=10A
Q_{gs}	Gate-to-Source Charge	—	—	10		V_{DS}=320V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD}=200V
t_r	Rise Time	—	31	—		I_D=10A
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		R_G=9.1Ω
t_f	Fall Time	—	20	—		R_D=20Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1100	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	190	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	18	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=10A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	380	570	ns	T_J=25°C, I_F=10A
Q_{rr}	Reverse Recovery Charge	—	2.8	4.2	μC	di/dt=100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=9.1mH

③ I_{SD}≤10A, di/dt≤120A/μs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 μs; duty cycle ≤2%.

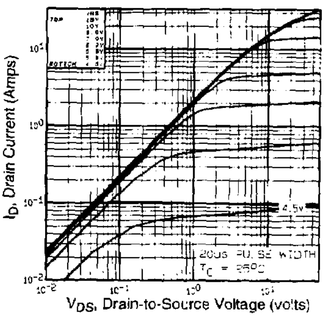


Fig 1. Typical Output Characteristics, T_C=25°C

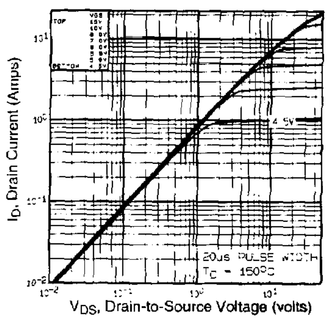


Fig 2. Typical Output Characteristics, T_C=150°C

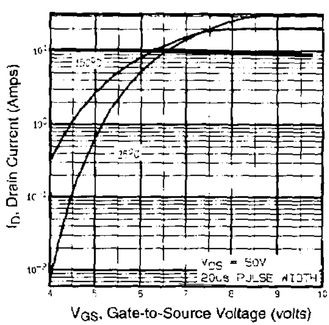


Fig 3. Typical Transfer Characteristics

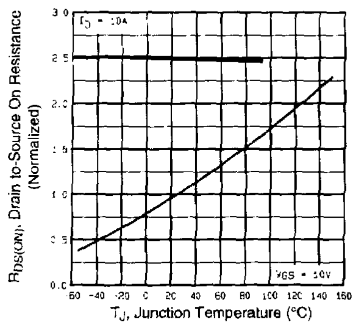


Fig 4. Normalized On-Resistance Vs. Temperature

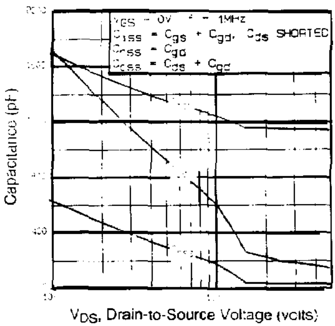


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

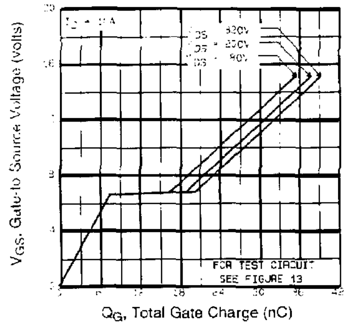


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

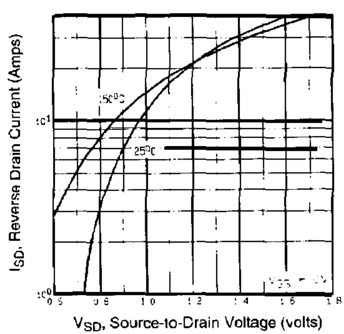


Fig 7. Typical Source-Drain Diode Forward Voltage

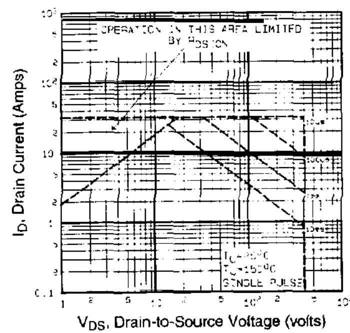


Fig 8. Maximum Safe Operating Area

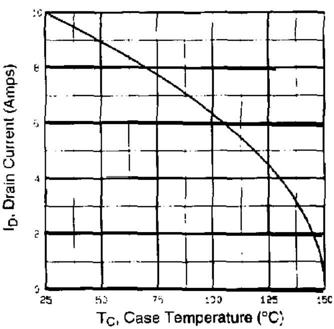


Fig 9. Maximum Drain Current Vs. Case Temperature

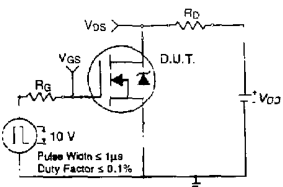


Fig 10a. Switching Time Test Circuit

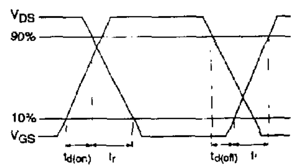


Fig 10b. Switching Time Waveforms

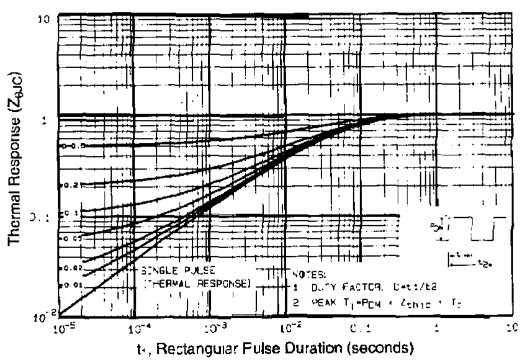


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

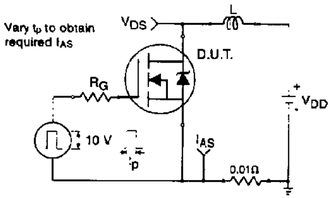


Fig 12a. Unclamped Inductive Test Circuit

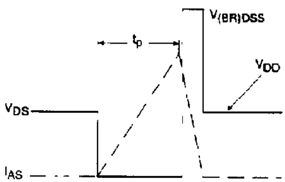


Fig 12b. Unclamped Inductive Waveforms

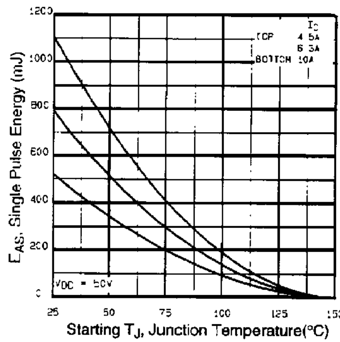


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

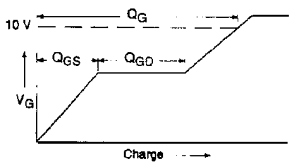


Fig 13a. Basic Gate Charge Waveform

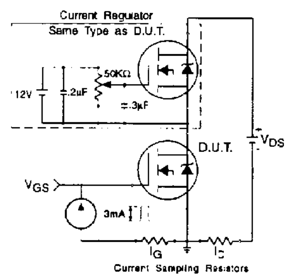


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit

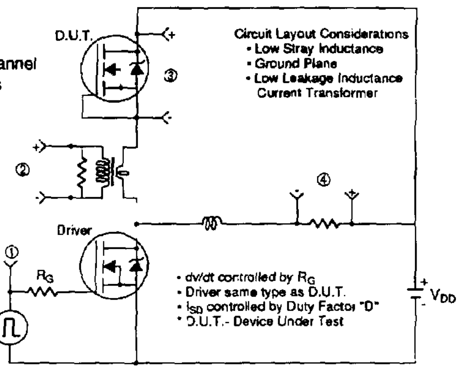
Appendix B: Package Outline Mechanical Drawing

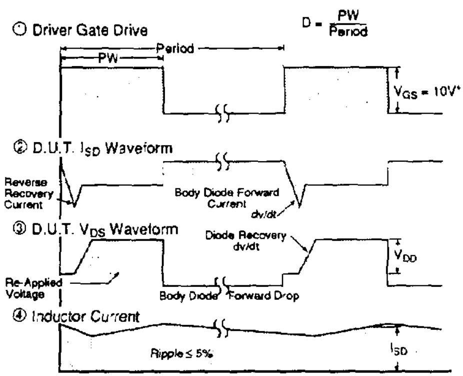
Appendix C: Part Marking Information

Appendix A

Peak Diode Recovery dv/dt Test Circuit

Fig 14. For N-Channel HEXFETs





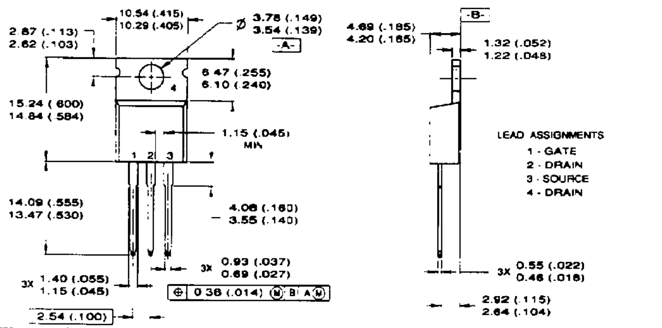
* V_{GS} = 5V for Logic Level Devices

Package Outline

Appendix B

TO-220AB Outline

Dimensions are shown in millimeters (inches)



NOTES

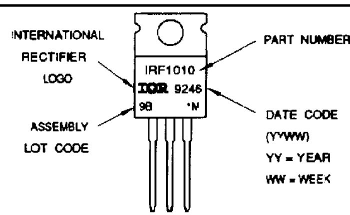
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220-AB.
4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

Appendix C

TO-220AB

EXAMPLE: THIS IS AN IRF1010 WITH ASSEMBLY LOT CODE 9B1M



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