

International Rectifier

POWER MOSFET

THRU-HOLE (TO-257AA)

Product Summary

Part Number	R _{ds(on)}	I _d	Eyelets
IRFY9240	0.51 Ω	-9.4A	Glass
IRFY9240M	0.51 Ω	-9.4A	Glass

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

Absolute Maximum Ratings

	Parameter	Units
I _d @ V _{GS} = -10V, T _C = 25°C	Continuous Drain Current	-9.4
I _d @ V _{GS} = -10V, T _C = 100°C	Continuous Drain Current	-6.0
I _{DM}	Pulsed Drain Current ①	-36
P _D @ T _C = 25°C	Max. Power Dissipation	100
	Linear Derating Factor	0.8
V _{GS}	Gate-to-Source Voltage	±20
E _A S	Single Pulse Avalanche Energy ②	700
I _{AR}	Avalanche Current ①	-9.4
E _{AR}	Repetitive Avalanche Energy ①	10
dv/dt	Peak Diode Recovery dv/dt ③	-5.5
T _J	Operating Junction	-55 to 150
T _{STG}	Storage Temperature Range	
	Lead Temperature	300(0.063in.(1.6mm)from case for 10 sec)
	Weight	3.3 (Typical)
		g

IRFY9240,IRFY9240M
200V, P-CHANNEL
HEXFET® MOSFET TECHNOLOGY



Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Glass Eyelets
- For Space Level Applications

Refer to Ceramic Version Part Numbers IRFY9240C, IRFY9240CM

Electrical Characteristics @ $T_j = 25^\circ\text{C}$ (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-200	—	—	V	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{I}_D = -1.0\text{mA}$
$\Delta \text{BV}_{\text{DSS}}/\Delta T_j$	Temperature Coefficient of Breakdown Voltage	—	-0.2	—	$\text{V}/^\circ\text{C}$	Reference to 25°C , $\text{I}_D = -1.0\text{mA}$
$\text{R}_{\text{DS}(\text{on})}$	Static Drain-to-Source On-State Resistance	—	—	0.51	Ω	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{I}_D = -6.0\text{A}$ ④
$\text{V}_{\text{GS}(\text{th})}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$\text{V}_{\text{DS}} = \text{V}_{\text{GS}}$, $\text{I}_D = -250\mu\text{A}$
g_{fs}	Forward Transconductance	4.0	—	—	$\text{S} (\text{r})$	$\text{V}_{\text{DS}} > -15\text{V}$, $\text{I}_{\text{DS}} = -6.0\text{A}$ ④
ID_{SS}	Zero Gate Voltage Drain Current	—	—	-25	μA	$\text{V}_{\text{DS}} = -160\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$
		—	—	-250		$\text{V}_{\text{DS}} = -160\text{V}$, $\text{V}_{\text{GS}} = 0\text{V}$, $T_j = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	$\text{V}_{\text{GS}} = -20\text{V}$
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		$\text{V}_{\text{GS}} = 20\text{V}$
Q_g	Total Gate Charge	—	—	60	nC	$\text{V}_{\text{GS}} = -10\text{V}$, $\text{I}_D = -9.4\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	15		$\text{V}_{\text{DS}} = -100\text{V}$
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	38		
$\text{t}_{\text{d}(\text{on})}$	Turn-On Delay Time	—	—	35	ns	$\text{V}_{\text{DD}} = -100\text{V}$, $\text{I}_D = -9.4\text{A}$, $\text{R}_G = 9.1\Omega$
t_r	Rise Time	—	—	85		
$\text{t}_{\text{d}(\text{off})}$	Turn-Off Delay Time	—	—	85		
t_f	Fall Time	—	—	65		
$\text{L}_{\text{S}} + \text{L}_{\text{D}}$	Total Inductance	—	6.8	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	1200	—	pF	$\text{V}_{\text{GS}} = 0\text{V}$, $\text{V}_{\text{DS}} = -25\text{V}$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	570	—		
C_{rss}	Reverse Transfer Capacitance	—	81	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-9.4	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-36		
V_{SD}	Diode Forward Voltage	—	—	-4.6	V	$T_j = 25^\circ\text{C}$, $\text{I}_S = -9.4\text{A}$, $\text{V}_{\text{GS}} = 0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	—	440	nS	$T_j = 25^\circ\text{C}$, $\text{I}_F = -9.4\text{A}$, $d\text{I}/dt \leq -100\text{A}/\mu\text{s}$
Q_{RR}	Reverse Recovery Charge	—	—	7.2	μC	$\text{V}_{\text{DD}} \leq -50\text{V}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $\text{L}_{\text{S}} + \text{L}_{\text{D}}$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	1.25	$^\circ\text{C}/\text{W}$	Typical socket mount
R_{thCS}	Case-to-sink	—	0.21	—		
R_{thJA}	Junction-to-Ambient	—	—	80		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page.

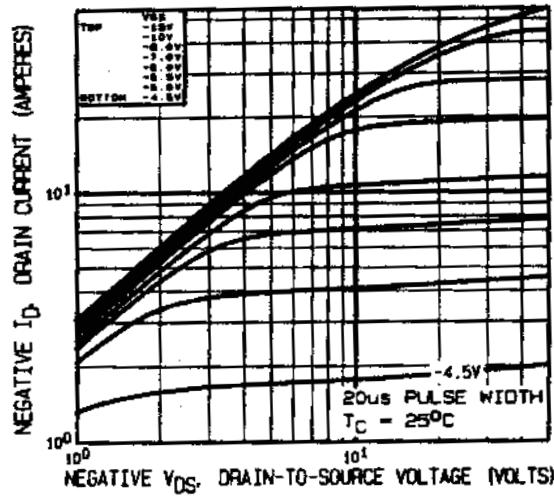


Fig 1. Typical Output Characteristics

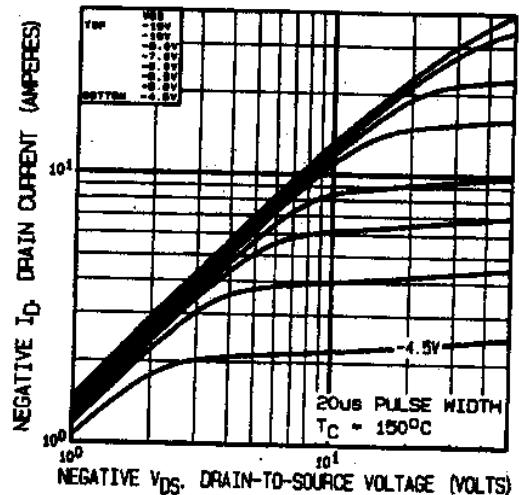


Fig 2. Typical Output Characteristics

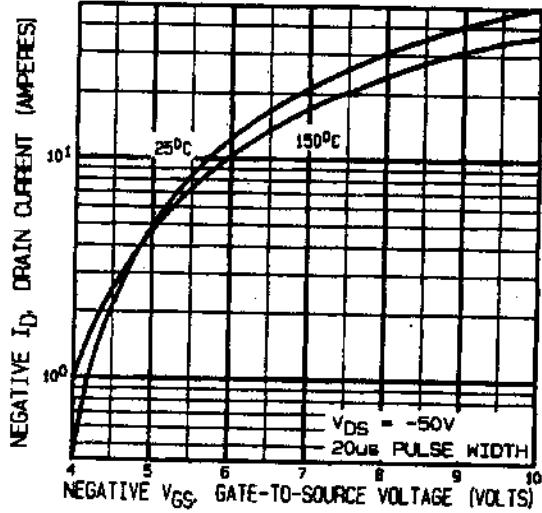


Fig 3. Typical Transfer Characteristics

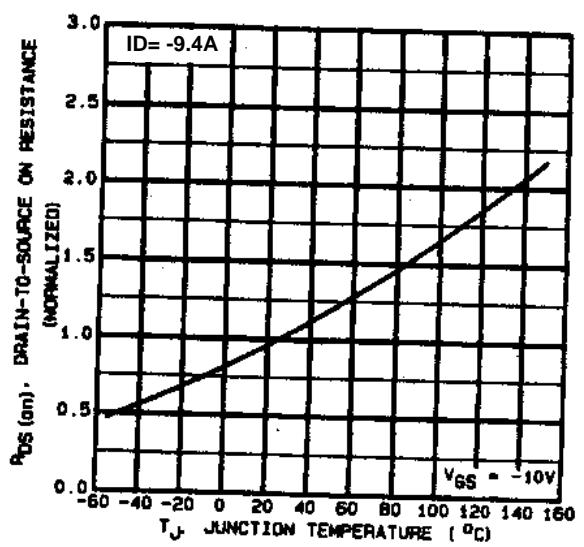


Fig 4. Normalized On-Resistance
Vs. Temperature

IRFY9240, IRFY9240M

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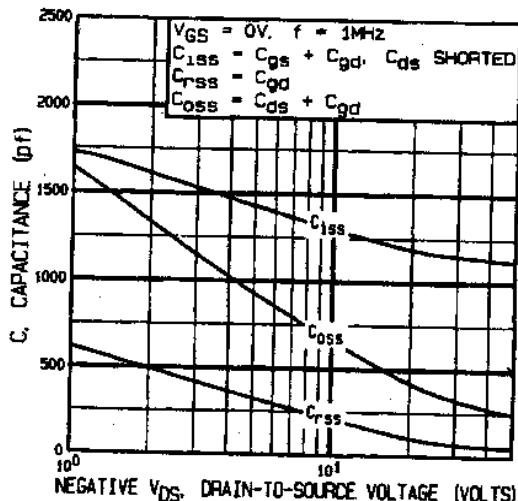


Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

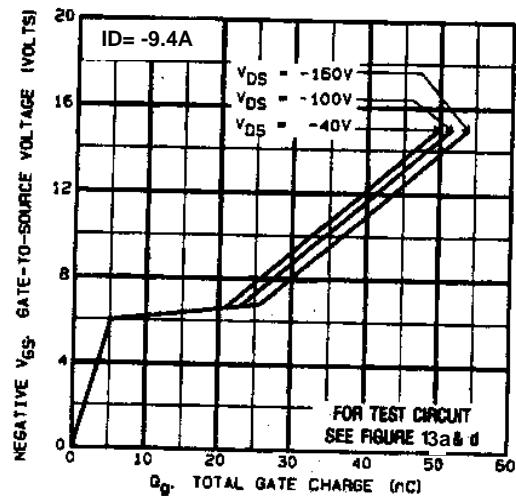


Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

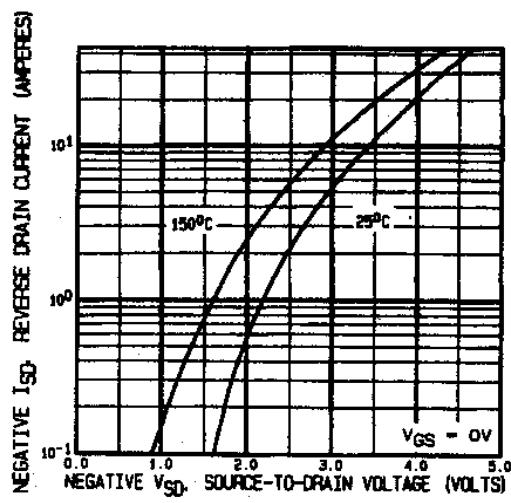


Fig 7. Typical Source-Drain Diode
Forward Voltage

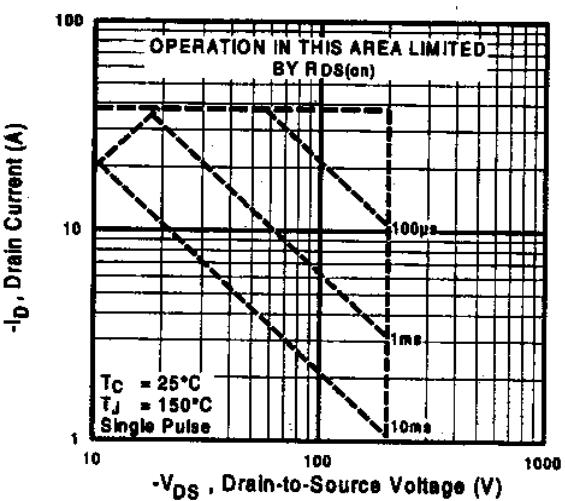


Fig 8. Maximum Safe Operating Area

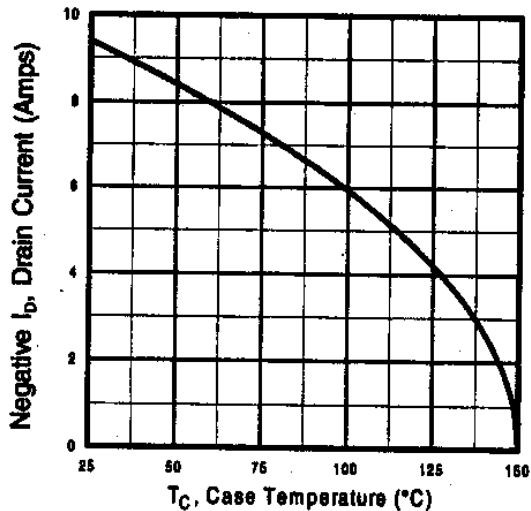


Fig 9. Maximum Drain Current Vs.
Case Temperature

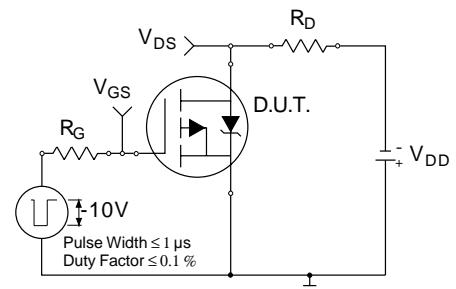


Fig 10a. Switching Time Test Circuit

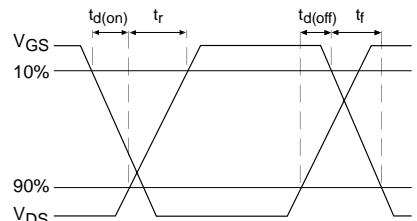


Fig 10b. Switching Time Waveforms

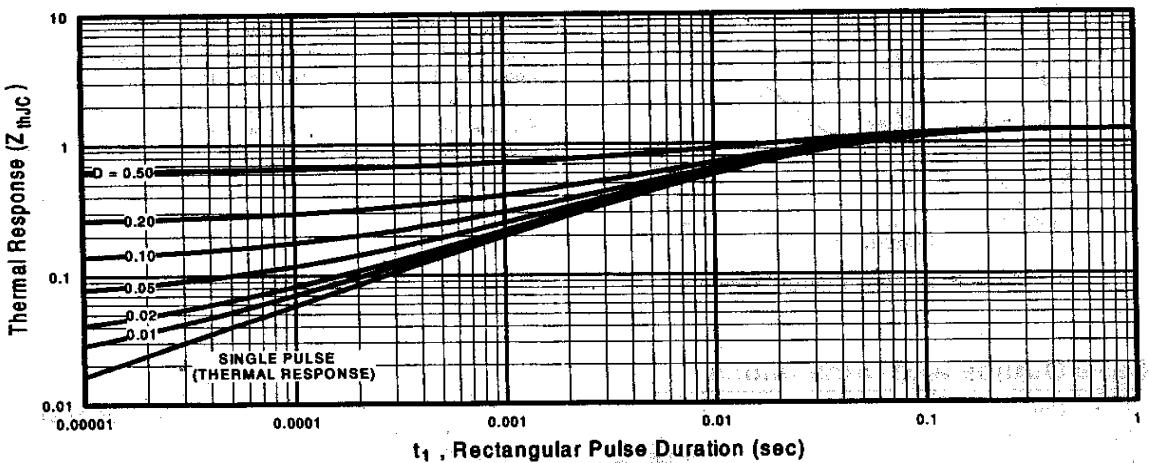


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

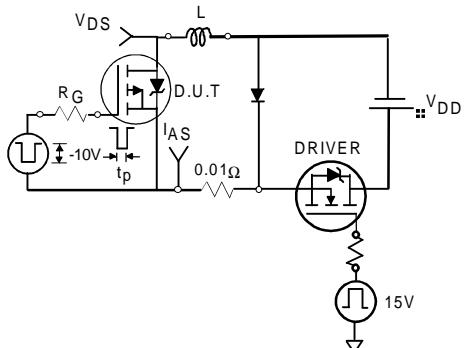


Fig 12a. Unclamped Inductive Test Circuit

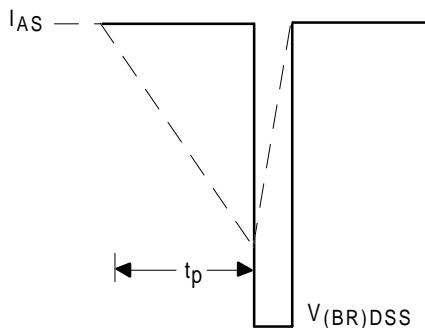


Fig 12b. Unclamped Inductive Waveforms

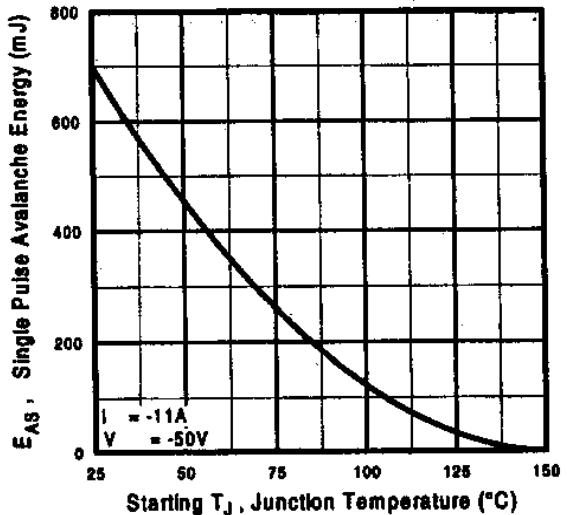


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

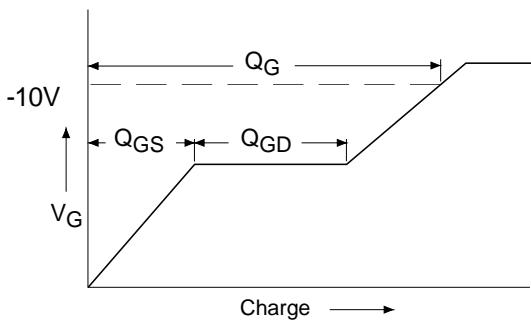


Fig 13a. Basic Gate Charge Waveform

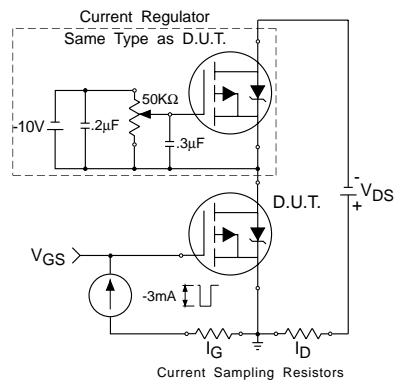
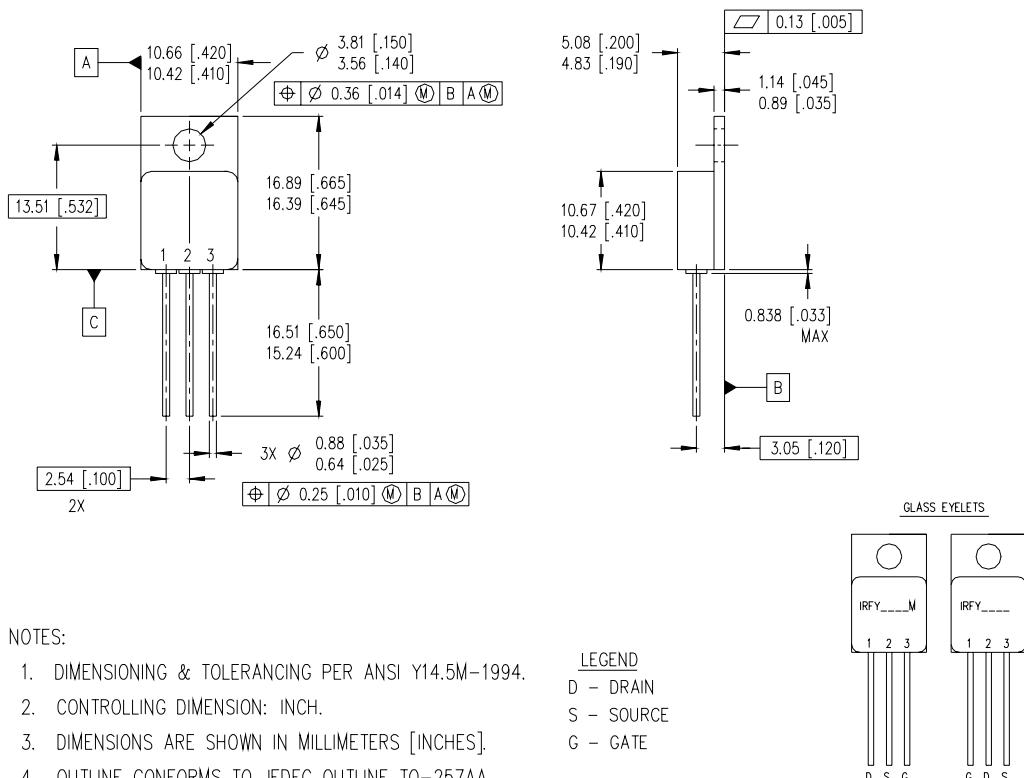


Fig 13b. Gate Charge Test Circuit

Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -50V$, starting $T_J = 25^\circ C$, $L = 15mH$
Peak $I_L = -9.4A$, $V_{GS} = -10V$
- ③ $|I_{SD}| \leq -9.4A$, $|di/dt| \leq -150A/\mu s$, $V_{DD} \leq -200V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions — TO-257AA



NOTES.

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA

LEGEND
D - DRAIN
S - SOURCE
G - GATE

International **ICR** Rectifier

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Data and specifications subject to change without notice. 04/01